Gowin LVDS7:1 LCD Driver Controller Reference Design

User Guide

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Revision History

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1 About This Guide

1.1 Purpose

This guide describes the LVDS7:1 LCD Driver Controller Reference Design. It mainly documents its functions and features, ports and timing, etc., and is designed to help users to quickly understand the features and usage of the Gowin LVDS7:1 LCD Driver Controller Reference Design.

1.2 Supported Products

The information presented in this guide applies to the following products:

GW2AR series of FPGA products: GW2AR-18

1.3 Related Documents

The latest user guides are available on the Gowin website. Refer to the related documents at www.gowinsemi.com:

GW2AR series of FPGA Products Data Sheet

1.4 Abbreviation and Terminology

The abbreviations and terminology used in this manual are as shown in Table 1-1.

Table 1-1: Abbreviations and Terminology

Abbreviations and Terminology	Full Name	Meaning
FPGA	Field Programmable Gate Array	Field Programmable Gate Array
LVDS	Low-Voltage Differential Signaling	Low-Voltage Differential Signaling
I/O	Input/Output	Input/Output
PLL	Phase Locked Loop	PLL

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information presented below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

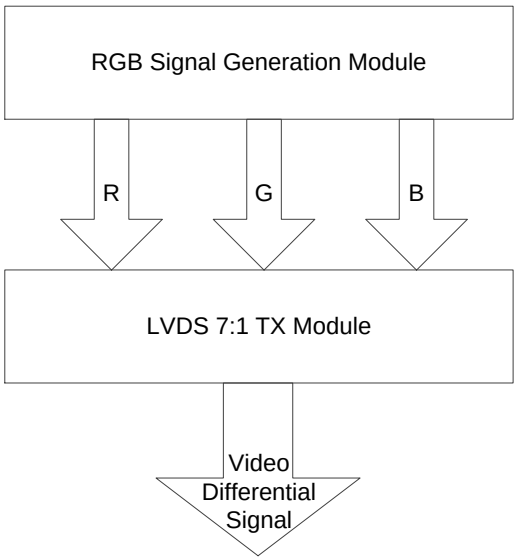
Tel: +86 755 8262 0391

2 Overview

2.1 Introduction

As a core block of the LCD driver circuit, the LCD driver controller provides the timing signals and displays data for the LCD system, which is the port between the company and LCD system. In the LVDS7:1 LCD Driver Controller Reference Design, the port adopts the LVDS I/O standard, and the RGB signal can be converted to the standard video difference signal. The structure diagram is shown in Figure 2-1.

Figure 2-1: LVDS7:1 LCD Driver Controller Schematic View



3 Features and Performance

3.1 Key Features

- Complies with LVDS port standard.
- Adopts low-voltage differential signaling.
- Supports high-speed, low-noise, long-distance, and high-accuracy transfer data.

3.2 Max. Frequency

The frequency of the LVDS7:1 LCD Driver Controller Reference Design timing port can be up to 800 Mbps.

3.3 Resource Utilization

The LVDS7:1 LCD Driver Controller can be realized via Verilog, which is applied to GW2A-18-LQFP144 FPGA. The resource utilization is shown in Table 3-1.

Table 3-1: Resource Utilization

Package Information	Speed Grade	Name	Resource Utilization
GW2AR-18-LQFP144	-8	LUT	85
		ALU	30
		PLL	1
		CLKDIV	1
		REG	46

4 Functional Description

4.1 Functions

The LVDS7:1 LCD Driver Controller Reference Design includes two modules:

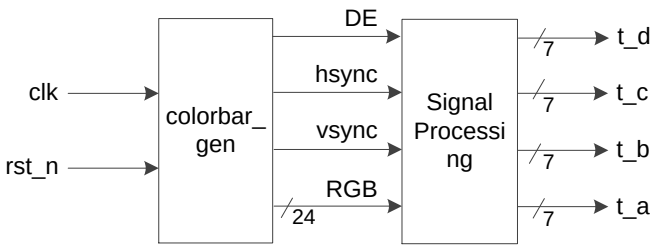
- RGB signal generation module
- LVDS 7:1 TX module

The RGB signal generation module mainly provides 24-bit RGB signal, line/field synchronizing signal and enable control signal; the LVDS 7:1 TX module converts the four-channel 7-bit LVDS signal to a four-channel series signal that can drive the LCD.

4.2 RGB Signal Generation Module

The RGB signal generation module provides a 24-bit RGB signal and line/field synchronizing signal and converts these signals to four-channel 7-bit LVDS signals. A functional diagram of the RGB signal generation module is presented in Figure 4-1.

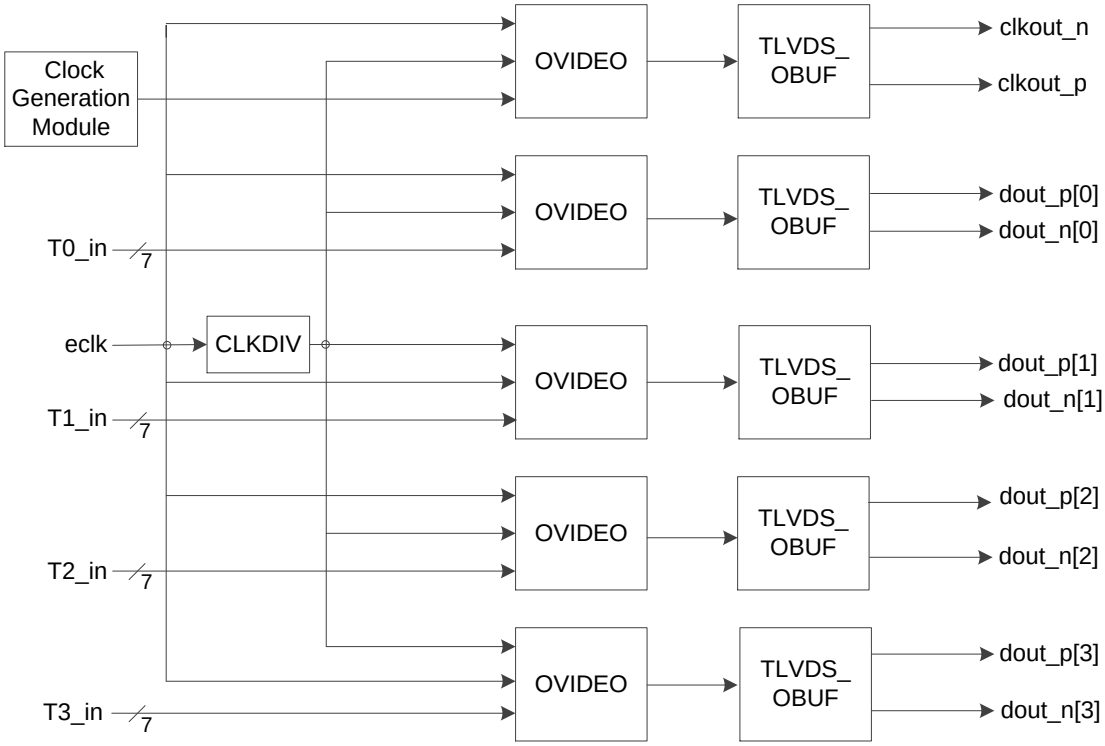
Figure 4-1: Functional Diagram of Signal Generation Module



4.3 LVDS 7:1 TX Module

The LVDS 7:1 TX module converts the four-channel 7-bit LVDS signal received from the RGB generation module to the four-channel series signal required to drive the LCD. The functional diagram is presented in Figure 4-2.

Figure 4-2: Functional Diagram of LVDS 7:1 TX Module

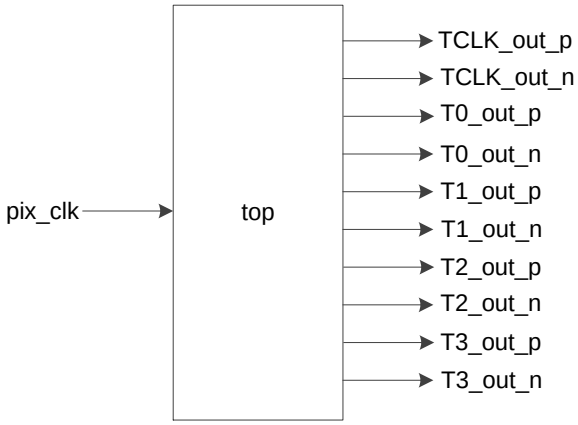


5 Description of Ports

5.1 LVDS7:1 Driver Controller View

The port diagram for the LVDS7:1 Driver Controller Reference Design is shown in Figure 5-1.

Figure 5-1: LVDS7:1 Driver Controller View



5.2 Port Signal

The port signals in the LVDS7:1 Driver Controller Reference Design are as shown in Table 5-1.

Table 5-1: Port Signals in the LVDS7:1 Driver Controller Reference Design

Port Name	Port Type	Description
pix_clk	input	Clocksignal
TCLK_out_p	output	Synchronous clock source CLK
TCLK_out_n	output	Synchronous clock source CLK
T0_out_p	output	Output serial data at port TX of 0-channel
T0_out_n	output	Output serial data at port TX of 0-channel

Port Name	Port Type	Description
T1_out_p	output	Output serial data at port TX of 1-channel
T1_out_n	output	Output serial data at port TX of 1-channel
T2_out_p	output	Output serial data at port TX of 2-channel
T2_out_n	output	Output serial data at port TX of 2-channel
T3_out_p	output	Output serial data at port TX of 3-channel
T3_out_n	output	Output serial data at port TX of 3-channel

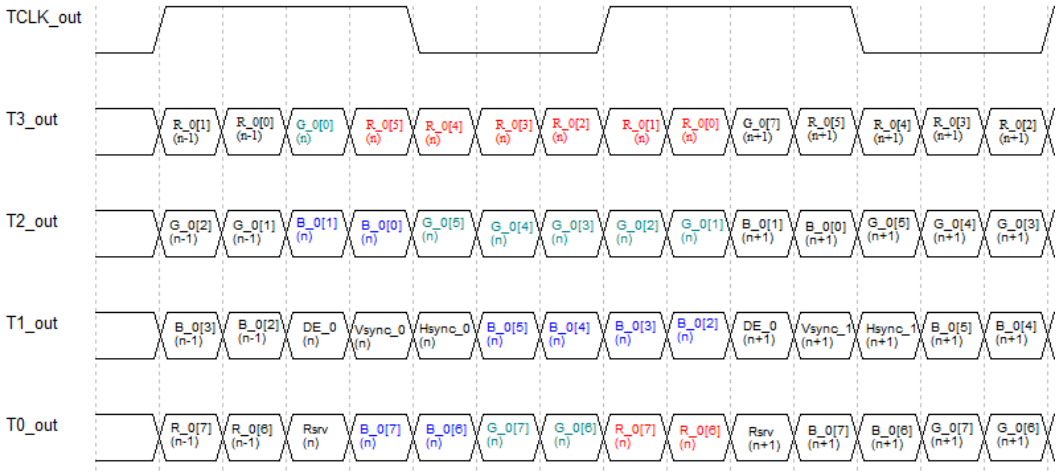
6 Timing Description

This chapter introduces the output signal timing of the LVDS7:1 Driver Controller Reference Design.

6.1 Timing Port Requirement

The LVDS7:1 Driver Controller Reference Design is used to produce an RGB signal. This is sent to the LCD after being converted to the standard video differential signal. The video differential signal includes one-channel (TCLK_out) and four-channel (T0_out, T1_out, T2_out and T3_out) forms. A pair of differential data lines can transmit 7-bit data. The signal timing is as shown in Figure 6-1.

Figure 6-1: LVDS7:1 Driver Port Timing



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