Gowin_EMPU_M1 Hardware Design
Reference Manual

IPUG531-1.6E, 06/12/2020
## Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Description</th>
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<tr>
<td>02/19/2019</td>
<td>1.0E</td>
<td>Initial version published.</td>
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<tr>
<td>07/18/2019</td>
<td>1.1E</td>
<td>MCU hardware design supports extended peripherals: CAN, Ethernet, SPI-Flash, RTC, DualTimer, TRNG, I2C, SPI, SD-Card.</td>
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</table>
| 08/18/2019 | 1.2E    | • MCU hardware design and software programming design support extended peripheral: DDR3 Memory;  
• Fixed known issues of ITCM, DTCM Size and IDE. |
| 09/27/2019 | 1.3E    | • MCU hardware design and software programming design support read, write and erasure of SPI-Flash;  
• MCU software programming design supports a continuous multi-byte read and write of I2C;  
• Fixed known issues of address mapping of AHB2 and APB2 extended interface in MCU software programming design;  
• Fixed known issues of continuous read and write of DDR3 Memory in MCU software programming design. |
| 01/16/2020 | 1.4E    | • MCU hardware design and software programming design supports PSRAM;  
• MCU compiling software GMD V1.0 updated;  
• RTOS reference design updated;  
• Hardware and software reference design of AHB2 and APB2 extension bus interface added. |
| 03/09/2020 | 1.5E    | • MCU hardware design supports the read and write of SD-Card;  
• Fixed known issues of the read and write of DDR3 in synthesis using Synplify Pro;  
• GW2A-18C/GW2AR-18C/GW2A-55C devices added. |
| 06/12/2020 | 1.6E    | • MCU supports for external instruction memory;  
• MCU supports for external data memory;  
• Extension of 6 AHB bus interfaces;  
• Extension of 16 APB bus interfaces;  
• GPIO supports multiple interface types;  
• I²C supports multiple interface types. |
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1 Hardware Architecture

1.1 System Architecture

Gowin_EMPU_M1 architecture consists of three levels, as shown in Figure 1-1.

- First level: Cortex-M1 core, ITCM, and DTCM;
- Second level: AHB bus, GPIO, CAN, Ethernet, DDR3 Memory, PSRAM, SPI-Flash, and AHB Master [1-6];
- Third level: APB bus, UART0, UART1, Timer0, Timer1, Watch Dog, RTC, TRNG, DualTimer, I2C Master, SPI Master, SD-Card, and APB Master [1-16].
1.2 System Feature

Gowin_EMPU_M1 includes two sub-systems:

- Cortex-M1 core sub-system
- AHB-Lite extension AHB bus and APB bus and peripheral interface sub-system

1.2.1 Cortex-M1 Core System

Processor Core

- ARM architecture v6-M Thumb supporting 16-bit Thumb and 32-bit Thumb2.
- Configurable extension operating system
- System exception handling
- Interrupt exception handling and normal thread model
- One stack pointer for normal operation system and two stack pointers for extension operation system
- Big/Little-endian format
  - Configurable Big/Little-endian format
  - Little-endian format for instructions and system control register
  - Little-endian format for debugging system

NVIC

- Number of external interrupts configured: 1, 8, 16, 32
- Four priority levels
- Saves processor status automatically during interrupts handling and recovers automatically at the end of interrupt processing

Debug System

- If debug system is disabled, Cortex-M1 does not support it;
- If debug system is enabled, Cortex-M1 supports it;
  - Full mode and reduced mode can be configured;
    - Full mode: Four BreakPoint Units and two Data Watchpoints
    - Reduced mode: Two BreakPoint Units and one Data Watchpoints
  - Configurable DAP ports.
    - JTAG/SW
    - JTAG
• SW

Memory

• ITCM: Instruction memory
  - Internal instruction memory or external instruction memory can be selected;
  - Internal instruction memory can be configured Size (1/2/4/8/16/32/64/128/256KB);
  - Internal instruction memory can be configured with initial values.

• DTCM: Data memory and configurable size.
  - Internal data memory or external data memory can be selected;
  - Internal data memory can be configured in size (1/2/4/8/16/32/64/128/256KB).

32 Bits Hardware Multiplier

• Normal mode
• Small mode

1.2.2 AHB-Lite Extension Sub-system

• AHB bus, GPIO, CAN, Ethernet, DDR3 Memory, PSRAM, SPI-Flash, and AHB Master [1-6];
• APB bus, UART0, UART1, Timer0, Timer1, Watch Dog, RTC, DualTimer, TRNG, I2C Master, SPI Master, SD-Card, APB Master [1-16].
### 1.3 System Ports

The Gowin_EMPU_M1 system port definitions are shown in Table 1-1.

<table>
<thead>
<tr>
<th>Name</th>
<th>I/O</th>
<th>Bit-Width</th>
<th>Description</th>
<th>Subordinate Module</th>
</tr>
</thead>
<tbody>
<tr>
<td>HCLK</td>
<td>in</td>
<td>1</td>
<td>system clock</td>
<td>-</td>
</tr>
<tr>
<td>hwRstn</td>
<td>in</td>
<td>1</td>
<td>system reset</td>
<td>-</td>
</tr>
<tr>
<td>LOCKUP</td>
<td>out</td>
<td>1</td>
<td>core Lockup state</td>
<td>-</td>
</tr>
<tr>
<td>HALTED</td>
<td>out</td>
<td>1</td>
<td>core Halt Debug state</td>
<td>Debug</td>
</tr>
<tr>
<td>JTAG_3</td>
<td>inout</td>
<td>1</td>
<td>TRST</td>
<td></td>
</tr>
<tr>
<td>JTAG_4</td>
<td>inout</td>
<td>1</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>JTAG_5</td>
<td>inout</td>
<td>1</td>
<td>TDI</td>
<td></td>
</tr>
<tr>
<td>JTAG_6</td>
<td>inout</td>
<td>1</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>JTAG_7</td>
<td>inout</td>
<td>1</td>
<td>TMS/SWDIO</td>
<td></td>
</tr>
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<td>JTAG_8</td>
<td>inout</td>
<td>1</td>
<td>GND</td>
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<td>JTAG_9</td>
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<td>1</td>
<td>TCK/SWDCLK</td>
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<td>JTAG_10</td>
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<td>1</td>
<td>GND</td>
<td></td>
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<td>JTAG_11</td>
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<td>RTCK</td>
<td>Debug</td>
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<td>JTAG_12</td>
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<td>1</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>JTAG_13</td>
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<td>TDO/SWO</td>
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<tr>
<td>JTAG_14</td>
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<td>1</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>JTAG_15</td>
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<td>1</td>
<td>RESET</td>
<td></td>
</tr>
<tr>
<td>JTAG_16</td>
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<td>GND</td>
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<td>NC</td>
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<td>JTAG_18</td>
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<td>GND</td>
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</tr>
<tr>
<td>GPIO</td>
<td>inout</td>
<td>[15:0]</td>
<td>GPIO input/output</td>
<td>GPIO I/O</td>
</tr>
<tr>
<td>GPIOIN</td>
<td>in</td>
<td>[15:0]</td>
<td>GPIO input</td>
<td>GPIO non-I/O</td>
</tr>
<tr>
<td>GPIOOUT</td>
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<td>GPIO output</td>
<td>UART0</td>
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<td>GPIOOUTEN</td>
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<td>GPIO output enable</td>
<td>UART1</td>
</tr>
<tr>
<td>UART0RXD</td>
<td>in</td>
<td>1</td>
<td>UART0 receiving</td>
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<tr>
<td>UART0TXD</td>
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<td>1</td>
<td>UART0 transmitting</td>
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</tr>
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<td>int</td>
<td>1</td>
<td>UART1 receiving</td>
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</table>
## Hardware Architecture

### 1.3 System Ports

<table>
<thead>
<tr>
<th>Name</th>
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<th>Bit-Width</th>
<th>Description</th>
<th>Subordinate Module</th>
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</tr>
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<td>TIMER0EXTIN</td>
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<td>1</td>
<td>Timer0 external interrupt</td>
<td>Timer0</td>
</tr>
<tr>
<td>TIMER1EXTIN</td>
<td>in</td>
<td>1</td>
<td>Timer1 external interrupt</td>
<td>Timer1</td>
</tr>
<tr>
<td>RTCSRCCLK</td>
<td>in</td>
<td>1</td>
<td>RTC clock source 32.768 KHz</td>
<td>RTC</td>
</tr>
<tr>
<td>SCL</td>
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<td>I2C I/O</td>
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<td>I2C non-I/O</td>
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<td>SDAOOUT</td>
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<td>serial data output</td>
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<td>Master device output / slave device input</td>
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<td>Master device input / slave device output</td>
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<td>SD-Card</td>
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<td>chip select signal</td>
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<td>data input</td>
<td></td>
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<td>CAN</td>
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<td>Name</td>
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<td>Description</td>
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<td>-----</td>
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<td>------------------------------</td>
<td>--------------------</td>
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</tr>
<tr>
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<td>1</td>
<td>RGMII transmitting control</td>
<td></td>
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<td>[3:0]</td>
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<td>RGMII receiving clock</td>
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</tr>
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<td>GMII_RXD</td>
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<td>[7:0]</td>
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</tr>
<tr>
<td>GMII_RX_ER</td>
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<td>1</td>
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<td>[7:0]</td>
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<tr>
<td>GMII_TX_EN</td>
<td>out</td>
<td>1</td>
<td>GMII transmitting enable</td>
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<td>GMII_TX_ER</td>
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<td>1</td>
<td>GMII transmitting error</td>
<td></td>
</tr>
<tr>
<td>MII_RX_CLK</td>
<td>in</td>
<td>1</td>
<td>MII receiving clock</td>
<td>Ethernet MII Interface</td>
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<tr>
<td>MII_RXD</td>
<td>in</td>
<td>[3:0]</td>
<td>MII receiving data</td>
<td></td>
</tr>
<tr>
<td>MII_RX_DV</td>
<td>in</td>
<td>1</td>
<td>MII receiving enable</td>
<td></td>
</tr>
<tr>
<td>MII_RX_ER</td>
<td>in</td>
<td>1</td>
<td>MII receiving error</td>
<td></td>
</tr>
<tr>
<td>MII_TX_CLK</td>
<td>in</td>
<td>1</td>
<td>MII transmitting clock</td>
<td></td>
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<tr>
<td>MII_TXD</td>
<td>out</td>
<td>[3:0]</td>
<td>MII transmitting data</td>
<td></td>
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<tr>
<td>MII_TX_EN</td>
<td>out</td>
<td>1</td>
<td>MII transmitting enable</td>
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</tr>
<tr>
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<td>out</td>
<td>1</td>
<td>MII transmitting error</td>
<td></td>
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<tr>
<td>MII_COL</td>
<td>in</td>
<td>1</td>
<td>MII conflict signal</td>
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<td>MII_CRS</td>
<td>in</td>
<td>1</td>
<td>MII carrier signal</td>
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<tr>
<td>MDC</td>
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<td>1</td>
<td>manage channel clock</td>
<td>Ethernet</td>
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Ethernet RGMII Interface

Ethernet GMII Interface

Ethernet MII Interface

Ethernet
<table>
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<tr>
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<th>I/O</th>
<th>Bit-Width</th>
<th>Description</th>
<th>Subordinate Module</th>
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<td>MDIO</td>
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<td>1</td>
<td>manage channel data</td>
<td></td>
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<td>DDR_CLK_I</td>
<td>in</td>
<td>1</td>
<td>50MHz clock input</td>
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<td>DDR_INIT_COMPLETE_O</td>
<td>out</td>
<td>1</td>
<td>initialize finish signal</td>
<td></td>
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<td>DDR_ADDR_O</td>
<td>out</td>
<td>[15:0]</td>
<td>Row address; Column address</td>
<td></td>
</tr>
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<td>DDR_BA_O</td>
<td>out</td>
<td>[2:0]</td>
<td>Bank address</td>
<td></td>
</tr>
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### 1.3 System Ports

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## 1.3 System Ports

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1.4 System Resources Statistics

The system resources statistics of Gowin_EMPU_M1 is shown in Table 1-2.

Table 1-2 System Resources Statistics

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<td>32</td>
<td>2</td>
</tr>
<tr>
<td>Cortex-M1 Default and All Peripherals</td>
<td></td>
<td>21029</td>
<td>12929</td>
<td>48</td>
<td>2</td>
</tr>
</tbody>
</table>
2 Software Design Flow

2.1 Hardware Environment

- DK-START-GW2A18 V2.0
  GW2A-LV18PG256C8/I7
- DK-START-GW1N9 V1.1
  GW1N-LV9LQ144C6/I5
- DK-START-GW2A55 V1.3
  GW2A-LV55PG484C8/I7
- DK-START-GW2AR18 V1.1
  GW2AR-LV18ELQ144PC6/I5

2.2 Software Environment

Gowin_V1.9.6 Beta and above

2.3 IP Core Generator

Gowin Software provides the IP Core Generator tool for configuring and generating Gowin_EMPU_M1 hardware designs.

For the IP Core Generator usage, please refer to SUG284, Gowin IP Core Generator User Guide.

2.4 Download Tool

Gowin software provides download tool "Programmer" for downloading hardware design bitstream files.

For instructions on how to use the download tool "Programmer", please refer to SUG502, Gowin Programmer User Guide.
2.5 Design Flow

Gowin_EMPU_M1 hardware design flow is as follows:

1. Use IP Core Generator tool to configure Cortex-M1, APB Bus peripherals, and AHB Bus peripherals, and generate Gowin_EMPU_M1 hardware design and import project;

2. Instantiate Gowin_EMPU_M1 Top Module, import user designs and connect user design with Gowin_EMPU_M1 Top Module;

3. Physical constraints and timing constraints;

4. Use the synthesis tool "Synplify Pro" or "GowinSynthesis";

5. Use Place & Route to generate the hardware design bitstream file.

6. Use download tool “Programmer” to download the hardware bitstream files to GW1N-9/GW1NR-9/GW2A-18/GW2A-18C/GW2AR-18/GW2AR-18C/GW2A-55/GW2A-55C.
3 Project Template

3.1 Creating Project

3.1.1 Create a New Project

Double click to open Gowin Software. Click "File > New… > FPGA Design Project" on the menu bar and create an FPGA Design project, as shown in Figure 3-1.

Figure 3-1 Create an FPGA Design Project
3.1.2 Set Project Name and Path

Enter the project name and select the project path, as shown in Figure 3-2.

Figure 3-2 Set Project Name and Path

3.1.3 Select Device

Select “Series”, “Device”, “Package”, “Speed” and “Part Number”, as shown in Figure 3-3.

Take development board reference design of DK-START-GW2A18 V2.0 in SDK for an instance, as shown below:

- **Series**: GW2A
- **Device**: GW2A-18
- **Package**: PBGA256
- **Speed**: C8/I7
- **Part Number**: GW2A-LV18PG256C8/I7
### 3.1.4 Complete Project Creating

As shown in Figure 3-4, new project creation is completed.

**Figure 3-4 Complete Project Creating**
3.2 Hardware Design

Use IP Core Generator tool to generate Gowin_EMPU_M1 hardware design.

Select "Tools > IP Core Generator" on the menu bar or click "IP Core Generator" to open IP Core Generator.

Select "Soft IP Core > Microprocessor System > Soft-Core-MCU > Gowin_EMPU_M1 1.6", as shown in Figure 3-5.

Figure 3-5 Select Gowin_EMPU_M1
Open Gowin_EMPU_M1. The system configuration of Gowin_EMPU_M1 includes Cortex-M1, APB Bus Peripheral and AHB Bus Peripherals, as shown in Figure 3-6.

Figure 3-6 System Architecture

3.2.1 Cortex-M1 Hardware Design

Cortex-M1 hardware design configuration is as shown in Table 3-1.

Table 3-1 Cortex-M1 Configuration Options

<table>
<thead>
<tr>
<th>Configuration Options</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of interrupts</td>
<td>Configure the number of external interrupts of Cortex-M1, can be selected 1, 8, 16, or 32. The default is 32.</td>
</tr>
<tr>
<td>OS Extension</td>
<td>Configure Cortex-M1 to support operation system or not, and support by default.</td>
</tr>
<tr>
<td>Configuration Options</td>
<td>Description</td>
</tr>
<tr>
<td>-----------------------</td>
<td>-------------</td>
</tr>
<tr>
<td>Small Multiplier</td>
<td>Configure small hardware multiplier, and normal by default.</td>
</tr>
<tr>
<td>Big Endian</td>
<td>Configure big endian format of data, and small endian format by default.</td>
</tr>
<tr>
<td>Enable Debug</td>
<td>Enable Cortex-M1 Debug, and enable Debug by default.</td>
</tr>
<tr>
<td>Debug Port Select</td>
<td>Configure debugger interface and can be selected as JTAG, Serial Wire, or JTAG and Serial Wire, and JTAG and Serial Wire by default.</td>
</tr>
<tr>
<td>Small Debug</td>
<td>Configure small debugger, and Full by default.</td>
</tr>
<tr>
<td>ITCM Select</td>
<td>Select internal or external instruction memory. The default is internal instruction memory.</td>
</tr>
<tr>
<td>ITCM Size</td>
<td>Configure Internal instruction memory Size and can be selected as 1/2/4/8/16/32/64/128/256KB.</td>
</tr>
<tr>
<td></td>
<td>- The max. size for GW1N-9/GW1NR-9/GW1N-9C/GW1NR-9C is 32KB, and 16KB by default;</td>
</tr>
<tr>
<td></td>
<td>- The max. size for GW2A-18/GW2A-18C/GW2AR-18/GW2AR-18C/GW2ANR-18C is 64KB, and 32KB by default;</td>
</tr>
<tr>
<td></td>
<td>- The max. size for GW2A-55/GW2A-55C is 256KB, and 64KB by default.</td>
</tr>
<tr>
<td>Initialize ITCM</td>
<td>Enable ITCM Initialization, and disabled by default.</td>
</tr>
<tr>
<td>ITCM Initialization Path</td>
<td>ITCM Initialization file path.</td>
</tr>
<tr>
<td>DTCM Select</td>
<td>Select internal or external data memory. The default is internal data memory.</td>
</tr>
<tr>
<td>DTCM Size</td>
<td>Configure the internal data memory Size and can be selected as 1/2/4/8/16/32/64/128/256KB.</td>
</tr>
<tr>
<td></td>
<td>- The max. size for GW1N-9/GW1NR-9/GW1N-9C/GW1NR-9C is 32KB, and 16KB by default;</td>
</tr>
<tr>
<td></td>
<td>- The max. size for GW2A-18/GW2A-18C/GW2AR-18/GW2AR-18C/GW2ANR-18C series is 64KB, and 32KB by default;</td>
</tr>
<tr>
<td></td>
<td>- The max. size for GW2A-55/GW2A-55C is 256KB, and 64KB by default.</td>
</tr>
</tbody>
</table>
Double click Cortex-M1 to open the Cortex-M1 configuration options, as shown in Figure 3-7. This includes common configuration, debug configuration, and memory configuration.

Figure 3-7 Cortex-M1 Configuration Options
Common

Select "Common" option, as shown in Figure 3-8, users can configure number of interrupts, OS extension, multiplier mode, and data storage mode.

Figure 3-8 Cortex-M1 Common Configuration

- **Number of Interrupts**
  Users can configure 1, 8, 16, or 32 external interrupts. The default is 32.

- **OS Extension**
  If it is selected, Cortex-M1 supports operation system extension, which is supported by default.

- **Small Multiplier**
  If it is selected, Cortex-M1 supports Small multiplier; if not, Cortex-M1 supports Normal multiplier. The default is Normal multiplier.

- **Big Endian**
  If it is selected, Cortex-M1 supports big endian format; if not, Cortex-M1 supports small endian format. The default is small endian format.
Debug

Select "Debug" option, as shown in Figure 3-9, users can configure enable/disable debug, debug ports, and debug mode.

Figure 3-9 Cortex-M1 Debug Configuration

- Enable Debug
  If Enable Debug is selected, Cortex-M1 supports debugging; if not, Cortex-M1 does not support debugging. The default is Enable Debug.

- Debug Port Select
  Users can select JTAG, Serial Wire, or JTAG and Serial Wire. The default is JTAG and Serial Wire.

- Debug Mode Configuration
  If Small Debug is selected, Cortex-M1 supports small mode debug; if not, Cortex-M1 supports Full mode debug. The default is Full mode debug.
Memory

Select "Memory" option as shown in Figure 3-10. Users can configure ITCM and DTCM.

Figure 3-10 Cortex-M1 Memory Configuration

- **ITCM Select Configuration**
  - Internal Instruction Memory or External Instruction Memory can be selected;
  - The default is Internal Instruction Memory;
  - Internal Instruction Memory: on-chip Block RAM hardware storage resource, starting address 0x00000000;
  - External Instruction Memory: such as DDR3/Flash, starting address 0x00000000.

- **ITCM Size Configuration**
  - Prerequisite: Internal Instruction Memory has been selected;
  - 1KB, 2KB, 4KB, 8KB, 16KB, 32KB, 64KB, 128KB, or 256KB can be selected;
- The max. ITCM size for GW1N-9/GW1NR-9/GW1N-9C/GW1NR-9C is 32KB. The default is 16KB;
- The max. ITCM size for GW2A-18/GW2A-18C/GW2AR-18/GW2AR-18C/GW2ANR-18C series is 64KB. The default is 32KB;
- The max. ITCM size for GW2A-55/GW2A-55C is 256KB. The default is 64KB.

**ITCM Initialization Configuration**
- Prerequisite: Internal Instruction Memory has been selected;
- If Initialization ITCM is selected, ITCM initialization is supported. Click the button after the textbox to import ITCM initialization file path;
- If you select Off-chip SPI-Flash downloading and startup, import different bootload file paths according to ITCM sizes.

*Note!*
ITCM Initialization Path can not include file path named after numbers.

**DTCM Select Configuration**
- Internal data Memory or External data Memory can be selected;
- The default is Internal data Memory;
- Internal data Memory: on-chip Block RAM hardware storage resource, starting address 0x20000000;
- External Instruction Memory: such as DDR3, starting address 0x20100000.

**DTCM Size Configuration**
- Prerequisite: Internal Data Memory has been selected;
- 1KB, 2KB, 4KB, 8KB, 16KB, 32KB, 64KB, 128KB, or 256KB can be selected;
- The max. DTCM size for GW1N-9/GW1NR-9/GW1N-9C/GW1NR-9C is 32KB. The default is 16KB;
- The max. DTCM size for GW2A-18/GW2A-18C/GW2AR-18/GW2AR-18C/GW2ANR-18C is 64KB. The default is 32KB;
- The max. DTCM size for GW2A-55/GW2A-55C is 256KB. The default is 64KB.

**Limitations of ITCM and DTCM Size Configuration**
- Prerequisites: Internal Instruction Memory and Internal Data
Memory have been selected;
- For GW1N-9/GW1NR-9/GW1N-9C/GW1NR-9C, ITCM or DTCM can be configured up to 32KB. If ITCM or DTCM has been configured to 32KB, the other can only be configured up to 16KB;
- For GW2A-18/GW2A-18C/GW2AR-18/GW2AR-18C/ GW2ANR-18C, ITCM or DTCM can be configured up to 64KB. If ITCM or DTCM has been configured to 64KB, the other can only be configured up to 16KB;
- For GW2A-55/GW2A-55C, ITCM or DTCM can be configured up to 256KB. If ITCM or DTCM has been configured to 256KB, the other can only be configured up to 16KB.

3.2.2 AHB-Lite Extension Hardware Design

AHB-Lite Extension configuration options are described in Table 3-2.

Table 3-2 AHB-Lite Extension Configuration Options

<table>
<thead>
<tr>
<th>Configuration Options</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Enable GPIO</td>
<td>Enable GPIO, off by default.</td>
</tr>
<tr>
<td>Enable GPIO I/O</td>
<td>Enable GPIO inout port type, enable by default.</td>
</tr>
<tr>
<td>Enable CAN</td>
<td>Enable CAN, off by default.</td>
</tr>
<tr>
<td>Buffer Depth</td>
<td>CAN select Buffer Depth. The default value is 256.</td>
</tr>
<tr>
<td>Enable Ethernet</td>
<td>Enable Ethernet, off by default.</td>
</tr>
<tr>
<td>Interface</td>
<td>Ethernet selects Interface (RGMII/GMII/MII). The default is RGMII.</td>
</tr>
<tr>
<td>RGMII Input Delay</td>
<td>RGMII input delay. The default value is 100.</td>
</tr>
<tr>
<td>MIIM Clock Divider</td>
<td>MIIM clock divider. The default value is 20.</td>
</tr>
<tr>
<td>Enable DDR3</td>
<td>Enable DDR3 Memory, off by default.</td>
</tr>
<tr>
<td>Enable PSRAM</td>
<td>Enable PSRAM, off by default.</td>
</tr>
<tr>
<td>Enable SPI-Flash</td>
<td>Enable SPI-Flash downloading and read, write, erasure of Memory, off by default.</td>
</tr>
<tr>
<td>Enable AHB Master [1]</td>
<td>Enable AHB Master [1], off by default.</td>
</tr>
</tbody>
</table>
## Configuration Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Enable UART0</td>
<td>Enable serial port0, off by default.</td>
</tr>
<tr>
<td>Enable UART1</td>
<td>Enable serial port1, off by default.</td>
</tr>
<tr>
<td>Enable Timer0</td>
<td>Enable Timer0, off by default.</td>
</tr>
<tr>
<td>Enable Timer1</td>
<td>Enable Timer1, off by default.</td>
</tr>
<tr>
<td>Enable WatchDog</td>
<td>Enable Watchdog, off by default.</td>
</tr>
<tr>
<td>Enable RTC</td>
<td>Enable RTC, off by default.</td>
</tr>
<tr>
<td>Enable TRNG</td>
<td>Enable TRNG, off by default.</td>
</tr>
<tr>
<td>Enable DualTimer</td>
<td>Enable DualTimer, off by default.</td>
</tr>
<tr>
<td>Enable I2C</td>
<td>Enable I2C, off by default.</td>
</tr>
<tr>
<td>Enable I2C I/O</td>
<td>Enable I2C inoutport type, enable by default.</td>
</tr>
<tr>
<td>Enable SPI</td>
<td>Enable SPI, off by default</td>
</tr>
<tr>
<td>Enable SD-Card</td>
<td>Enable SD-Card, off by default</td>
</tr>
<tr>
<td>Enable APB Master [1]</td>
<td>Enable APB Master [1], off by default.</td>
</tr>
<tr>
<td>Enable APB Master [8]</td>
<td>Enable APB Master [8], off by default.</td>
</tr>
<tr>
<td>Enable APB Master [9]</td>
<td>Enable APB Master [9], off by default.</td>
</tr>
<tr>
<td>Enable APB Master [10]</td>
<td>Enable APB Master [10], off by default.</td>
</tr>
<tr>
<td>Enable APB Master [12]</td>
<td>Enable APB Master [12], off by default.</td>
</tr>
<tr>
<td>Enable APB Master [16]</td>
<td>Enable APB Master [16], off by default.</td>
</tr>
</tbody>
</table>
**GPIO Configuration**

- Double click to open GPIO to configure GPIO, as shown in Figure 3-11.
- If Enable GPIO is selected, Gowin_EMPU_M1 supports GPIO, off by default.
- If Enable GPIO has been selected, GPIO port type can be configured.
- If Enable GPIO I/O is selected, GPIO supports “inout” input/output port types by default.

**Figure 3-11 GPIO Configuration**
CAN Configuration

Double click to open CAN, as shown in Figure 3-12;
- If Enable CAN is selected, Gowin_EMPU_M1 supports CAN, off by default;
- If Enable CAN has been selected, Buffer Depth can be configured;
- Select and configure Buffer Depth. The default value is 256.

Figure 3-12 CAN Configuration

Ethernet Configuration

Double click to open Ethernet, as shown in Figure 3-13;
- If Enable Ethernet is selected, Gowin_EMPU_M1 supports Ethernet, off by default;
- If Enable Ethernet has been selected, Interface, RGMII Input Delay, and MIIM Clock Divider can be configured;
  - Select Interface, RGMII, GMII, MII, or GMII/MII can be configured. The default is RGMII;
  - If you select RGMII, RGMII Input Delay can be configured. The default value is 100;
- If you select MIIM Clock Divider, MIIM Clock Divider can be configured;

- If you select RGMII or GMII, 125MHz clock input must be provided to GTX_CLK. The default value is 20.

Figure 3-13 Ethernet Configuration
**DDR3 Configuration**

Double-click to open DDR3 to configure DDR3, as shown in Figure 3-14;

- If select Enable DDR3, Gowin_EMPU_M1 supports DDR3, off by default;
- The frequency of DDR3 clock is 150MHz;
- 50MHz clock must be provided to DDR3 port “DDR_CLK_I”.

Figure 3-14 DDR3 Configuration
SPI-Flash Configuration

SPI-Flash supports downloading and read, write and erasure of Memory;

Double click to open SPI-Flash, as shown in Figure 3-15;

- If Enable SPI-Flash is selected, Gowin_EMPU_M1 supports SPI-Flash, off by default;
- If Gowin_EMPU_M1 uses off-chip SPI-Flash downloading and startup, Enable SPI-Flash must be selected.

Figure 3-15 SPI-Flash Configuration

AHB Master [1-6] Configuration

Double click to open AHB Master [1-6]. AHB Master [1-6] user AHB bus expansion interface can be configured, as shown in Figure 3-16;

- If Enable AHB Master [1] is selected, Gowin_EMPU_M1 supports the AHB Master [1] user AHB bus expansion interface, where users can expand AHB external devices, off by default.
- If Enable AHB Master [2] is selected, Gowin_EMPU_M1 supports the AHB Master [2] user AHB bus expansion interface, where users can
expand AHB external devices, off by default.

- If Enable AHB Master [3] is selected, Gowin_EMPU_M1 supports the AHB Master [3] user AHB bus expansion interface, where users can expand AHB external devices, off by default.
- If Enable AHB Master [4] is selected, Gowin_EMPU_M1 supports the AHB Master [4] user AHB bus expansion interface, where users can expand AHB external devices, off by default.
- If Enable AHB Master [5] is selected, Gowin_EMPU_M1 supports the AHB Master [5] user AHB bus expansion interface, where users can expand AHB external devices, off by default.
- If Enable AHB Master [6] is selected, Gowin_EMPU_M1 supports the AHB Master [6] user AHB bus expansion interface, where users can expand AHB external devices, off by default.

Figure 3-16 AHB Master [1-6] Configuration
The starting address and address space definitions for the AHB Master [1-6] user AHB bus extension interface are shown in Table 3-3.

Table 3-3 AHB Master [1-6] Address Definition

<table>
<thead>
<tr>
<th>AHB Bus Interface</th>
<th>Starting Address</th>
<th>Size (MB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AHB Master [1]</td>
<td>0x80000000</td>
<td>16</td>
</tr>
<tr>
<td>AHB Master [2]</td>
<td>0x81000000</td>
<td>16</td>
</tr>
<tr>
<td>AHB Master [3]</td>
<td>0x86000000</td>
<td>16</td>
</tr>
<tr>
<td>AHB Master [4]</td>
<td>0x89000000</td>
<td>16</td>
</tr>
<tr>
<td>AHB Master [5]</td>
<td>0x8A000000</td>
<td>16</td>
</tr>
<tr>
<td>AHB Master [6]</td>
<td>0x8B000000</td>
<td>16</td>
</tr>
</tbody>
</table>

UART Configuration

Double click UART0 or UART1, as shown in Figure 3-17;

- If Enable UART0 is selected, Gowin_EMPU_M1 supports UART0, off by default;
- If Enable UART1 is selected, Gowin_EMPU_M1 supports UART1, off by default.

Figure 3-17 UART Configuration
Timer Configuration

Double click to open Timer0 or Timer1, as shown in Figure 3-18;

- If Enable Timer0 is selected, Gowin_EMPU_M1 supports Timer0, off by default;
- If Enable Timer1 is selected, Gowin_EMPU_M1 supports Timer1, off by default.

Figure 3-18 Timer Configuration
WatchDog Configuration

Double click to open WatchDog, as shown in Figure 3-19;

If Enable WatchDog is selected, Gowin_EMPU_M1 supports WatchDog, off by default.

Figure 3-19 WatchDog Configuration
RTC Configuration

Double click to open RTC, as shown in Figure 3-20;

If Enable RTC is selected, Gowin_EMPU_M1 supports RTC, off by default.

Figure 3-20 RTC Configuration
DualTimer Configuration

Double click to open DualTimer, as shown in Figure 3-21;

If Enable DualTimer is selected, Gowin_EMPU_M1 supports DualTimer, off by default.

Figure 3-21 DualTimer Configuration
TRNG Configuration

Double click to open TRNG, as shown in Figure 3-22;

If Enable TRNG is selected, Gowin_EMPU_M1 supports TRNG, off by default.

Figure 3-22 TRNG Configuration

The Cortex-M1 core of Gowin_EMPU_M1 interacts with TRNG block through APB bus. The TRNG block is a fully verified block which can implement true random number generator.
I2C Configuration

Double click to open I2C Master, as shown in Figure 3-23;

- If Enable I2C is selected, Gowin_EMPU_M1 supports I2C, off by default.
- If Enable I2C has been selected, I2C Master port type can be configured.
- If Enable I2C I/O is selected, I2C Master supports “inout” input/output port type, support by default.

Figure 3-23 I2C Configuration
SPI Configuration

Double click to open SPI Master, as shown in Figure 3-24;

If Enable SPI is selected, Gowin_EMPU_M1 supports SPI, off by default.

Figure 3-24 SPI Configuration
SD-Card Configuration

Double click to open SD-Card, as shown in Figure 3-25;

- If Enable SD-Card is selected, Gowin_EMPU_M1 supports SD-Card, off by default;
- SD_SPICLK of SD-Card requires 30MHz clock input.

Figure 3-25 SD-Card Configuration
APB Master [1-16] Configuration

Double click to open APB Master [1-16]. APB Master [1-16] can be configured as shown in Figure 3-26;

- If Enable APB Master [1] is selected, Gowin_EMPU_M1 supports the APB Master [1] user APB bus expansion interface, where users can expand AHB external devices, off by default.
- If Enable APB Master [2] is selected, Gowin_EMPU_M1 supports the APB Master [2] user APB bus expansion interface, where users can expand AHB external devices, off by default.
- If Enable APB Master [3] is selected, Gowin_EMPU_M1 supports the APB Master [3] user APB bus expansion interface, where users can expand AHB external devices, off by default.
- If Enable APB Master [4] is selected, Gowin_EMPU_M1 supports the APB Master [4] user APB bus expansion interface, where users can expand AHB external devices, off by default.
- If Enable APB Master [5] is selected, Gowin_EMPU_M1 supports the APB Master [5] user APB bus expansion interface, where users can expand AHB external devices, off by default.
- If Enable APB Master [6] is selected, Gowin_EMPU_M1 supports the APB Master [6] user APB bus expansion interface, where users can expand AHB external devices, off by default.
- If Enable APB Master [7] is selected, Gowin_EMPU_M1 supports the APB Master [7] user APB bus expansion interface, where users can expand AHB external devices, off by default.
- If Enable APB Master [8] is selected, Gowin_EMPU_M1 supports the APB Master [8] user APB bus expansion interface, where users can expand AHB external devices, off by default.
- If Enable APB Master [9] is selected, Gowin_EMPU_M1 supports the APB Master [9] user APB bus expansion interface, where users can expand AHB external devices, off by default.
- If Enable APB Master [10] is selected, Gowin_EMPU_M1 supports the APB Master [10] user APB bus expansion interface, where users can expand AHB external devices, off by default.
- If Enable APB Master [12] is selected, Gowin_EMPU_M1 supports the APB Master [12] user APB bus expansion interface, where users can expand AHB external devices, off by default.
- If Enable APB Master [13] is selected, Gowin_EMPU_M1 supports the APB Master [13] user APB bus expansion interface, where users can
expand AHB external devices, off by default.

- If Enable APB Master [14] is selected, Gowin_EMPU_M1 supports the APB Master [14] user APB bus expansion interface, where users can expand AHB external devices, off by default.
- If Enable APB Master [15] is selected, Gowin_EMPU_M1 supports the APB Master [15] user APB bus expansion interface, where users can expand AHB external devices, off by default.
- If Enable APB Master [16] is selected, Gowin_EMPU_M1 supports the APB Master [16] user APB bus expansion interface, where users can expand AHB external devices, off by default.

Figure 3-26 APB Master [1-16] Configuration
The starting address and address space definitions for the APB Master [1-6] user AHB bus extension interface are shown in Table 3-4.

Table 3-4 APB Master [1-6] Address Definition

<table>
<thead>
<tr>
<th>APB Bus Interface</th>
<th>Starting Address</th>
<th>Size (MB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>APB Master [1]</td>
<td>0x60000000</td>
<td>1</td>
</tr>
<tr>
<td>APB Master [2]</td>
<td>0x60100000</td>
<td>1</td>
</tr>
<tr>
<td>APB Master [3]</td>
<td>0x60200000</td>
<td>1</td>
</tr>
<tr>
<td>APB Master [4]</td>
<td>0x60300000</td>
<td>1</td>
</tr>
<tr>
<td>APB Master [5]</td>
<td>0x60400000</td>
<td>1</td>
</tr>
<tr>
<td>APB Master [6]</td>
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</tbody>
</table>
PSRAM

Double click to open PSRAM as shown in Figure 3-27;
- If Enable PSRAM is selected, Gowin_EMPU_M1 supports PSRAM, off by default;
- The following devices support Gowin_EMPU_M1 PSRAM.
  - GW2AR-LV18QN88PES
  - GW2AR-LV18QN88PC8/I7
  - GW2AR-LV18QN88PC7/I6
  - GW2AR-LV18EQ144PES
  - GW2AR-LV18EQ144PC8/I7
  - GW2AR-LV18EQ144PC7/I6
  - GW2AR-LV18EQ144PC9/I8

Figure 3-27 PSRAM Configuration
3.3 User Design

- After the configuration of Gowin_EMPU_M1, users can generate Gowin_EMPU_M1 hardware design;
- Instantiate Gowin_EMPU_M1 Top Module;
- Import user designs and connect Gowin_EMPU_M1 Top Module and user design to form a complete RTL design.

3.4 Constraint

After the user RTL design is completed, physical constraints can be
generated according to the used development board and the output IO.

Timing constraints file can be generated according to timing requirements.

For further details about how to generate physical constraints, please refer to SUG101, Gowin Design Constraints Guide.

3.5 Configuration

3.5.1 Synthesis Option Configuration

Synthesis option configuration is shown in Figure 3-29.

- Select the synthesis tool “Synlify Pro” or “GowinSynthesis”.
- Configure Top Module/Entity based on the actual top module name in the design.
- Configure Include Path based on the actual file reference path in the design.

Figure 3-29 Synthesis Option Configuration
3.5.2 Post-Place File Configuration

If download the merged file of Gowin_EMU_M1 software design and hardware design automatically, configure “Place & Route > General > Generate Post-Place File” to generate Post-Place File as shown in Figure 3-30.

Figure 3-30 Post-Place File Configuration
3.5.3 Dual-Purpose Pin Configuration

If Gowin_EMPU_M1 selecting off-chip SPI-Flash downloading, use SSPI and MSPI as regular IO, as shown in Figure 3-31. Or pin multiplexing is not required.

Figure 3-31 Dual-Purpose Pin Configuration
3.6 Synthesize

Run Synplify Pro or GowinSynthesis in Gowin Software to finish the RTL design synthesis, as shown in Figure 3-32.

Figure 3-32 Synthesis

For the tools usage, please refer to SUG100, Gowin Software User Guide.
3.7 Place & Route

Run the Place & Route tool in Gowin Software and generate the hardware design bitstream files, as shown in Figure 3-33.

Figure 3-33 Place & Route

For the tool usage, please refer to SUG100, Gowin Software User Guide.

3.8 Download

Run Programmer in Gowin Software to download hardware design bitstream files.

Open the download tool “Programmer” in the Gowin Software or software installation path. Click "Edit/Configure Device" in the Programmer menu bar or click “Configure Device” " đựng " in the toolbar to open “Device configuration”.

If the development board on-board device is GW1N-9/GW1NR-9/ GW1N-9C/GW1NR-9C, the download option configuration is shown in Figure 3-34.

- Select "Embedded Flash Mode" option from drop-down list "Access
Project Template

3.8 Download

- Select "embFlash Erase, Program" or "embFlash Erase, Program, Verify" option from drop-down list "Operation".
- Import the required hardware design bitstream file in "Programming Options > File name ".
- Click "Save" to finish configuring the hardware design bitstream file download options, as shown in Figure 3-34.

Figure 3-34 Device configuration for GW1N Series

If the development board on-board device is GW2A-18/GW2A-18C/GW2AR-18/GW2AR-18C/ GW2ANR-18C/ GW2A-55/GW2A-55C, the download option configuration is shown in Figure 3-35.

- Select "External Flash Mode" from drop-down list "Access Mode".
- Select "exFlash Erase, Program" from drop-down list "Operation",
- Import required hardware design bitstream file in " Programming Options > File name ".
- Please select "External Flash Options > Device" option according to the type of Flash chip on board (such as Gowin development board on-board Winbond W25Q64BV).
- Please set the "External Flash Options > Start Address" option to "0x000000".
- Click "Save" to finish configuring the hardware design bitstream file
download options, as shown in Figure 3-35.

Figure 3-35 Device configuration for GW2A

After device configuration, click "Program/Configure" on the Programmer toolbar to download the hardware design bitstream files.

For the usage of the download tool “Programmer”, please refer to SUG502, Gowin Programmer User Guide.
Gowin_EMPU_M1 provides reference designs for Debug and No Debug. Get following reference designs by this link:

- Gowin_EMPU_M1\ref_design\FPGA_RefDesign\Debug_RefDesign
- Gowin_EMPU_M1\ref_design\FPGA_RefDesign\NoDebug_RefDesign