



DK_LED-RxCard_GW3A-LV20UG324S_V2.1 Development Board **User Guide**

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1 About This Manual

1.1 Purpose

The DK_LED-RxCard_GW3A-LV20UG324S_V2.1 development board (hereinafter referred to as "the development board") user guide consists of the following three parts:

- A brief introduction to the features of the development board.
- An introduction to the development board system architecture and hardware resources.
- An introduction to the hardware circuits, functions and pin assignments.

1.2 Related Documents

You can find the related documents at www.gowinsemi.com:

- [DS1351, GW3A series of FPGA Products Data Sheet](#)
- [UG1353, GW3A-20 Pinout](#)
- [UG1354, GW3A series of FPGA Products Package and Pinout User Guide](#)
- [UG1356, GW3A series of FPGA Products Schematic Manual](#)
- [UG734, Arora III 20K FPGA Products Programming and Configuration User Guide](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
DDR	Double Data Rate
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable I/O
JTAG	Joint Test Action Group

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

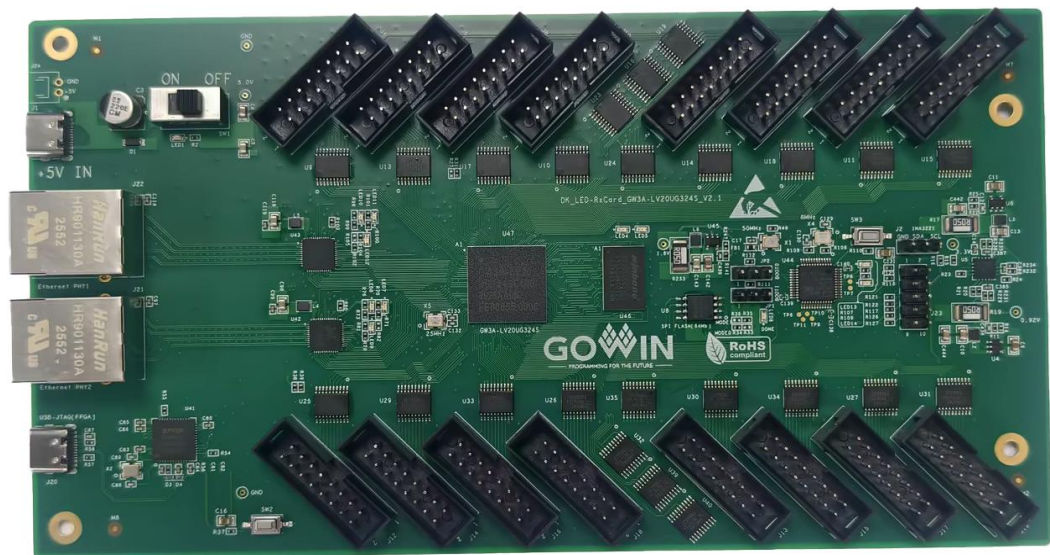
Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Development Board Introduction

2.1 Overview

Figure 2-1 Photo of the Development Board



The Gowin GW3A FPGAs belong to the Arora III series. They offer a wide range of on-chip resources, including versatile I/O interfaces and BSRAM, making them well suited for low-power, high-performance applications.

The DK_LED-RxCard_GW3A-LV20UG324S_V2.1 development board integrates an MCU, GPIO, an Ethernet interface, and other features. It meets the needs of FPGA performance evaluation, software learning, debugging, and other applications for LED receiving cards.

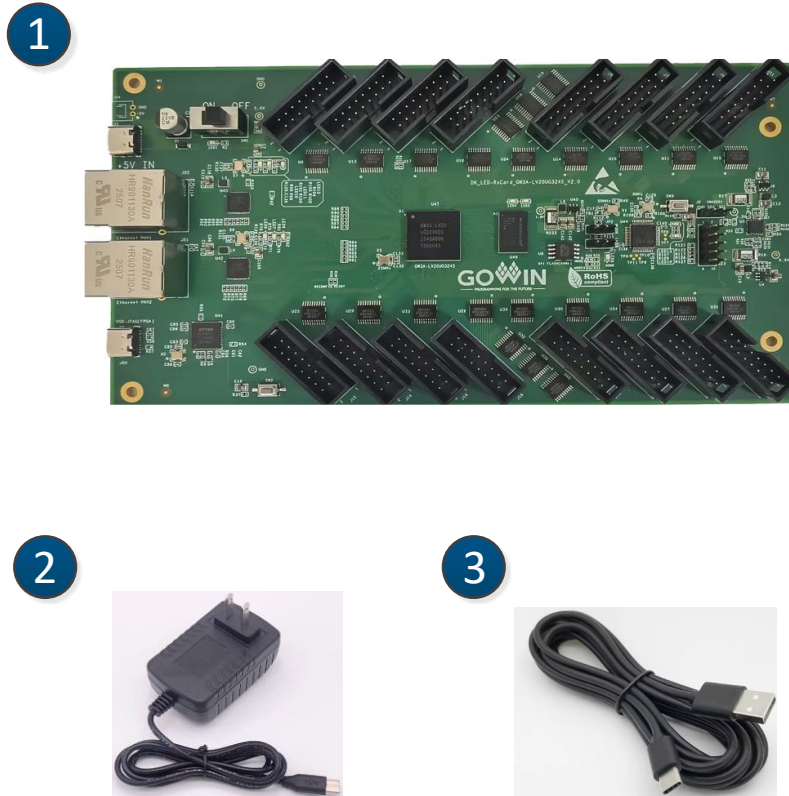
The development board uses a Gowin GW3A-LV20UG324S FPGA device. For the internal resources of the chip, see [DS1351, GW3A series of FPGA Products Data Sheet](#).

2.2 A Development Board Kit

The development board kit includes the following items:

1. DK_LED-RxCard_GW3A-LV20UG324S_V2.1 development board
2. 5 V/2 A Type-C power adapter
3. Type-A to Type-C cable

Figure 2-2 A Development Board Kit



- ① DK_LED-RxCard_GW3A-LV20UG324S_V2.1 development board
- ② 5 V input Type-C power adapter
- ③ Type-A to Type-C cable

2.5 Features

The key features are as follows:

- **FPGA Device**
 - Gowin GW3A-LV20UG324S FPGA
- **Download and Boot**
 - Integrates USB download circuit on the development board; downloads through Type-C interface.
 - External SPI Flash Boot
- **Power Supply**
 - External DC 5V power supply
 - The POWER LED turns on when power is applied.
 - The development board generates 3.3V, 1.8V, and 0.9V power supplies.
- **Clock system**
 - 50 MHz active crystal oscillator
 - 25 MHz crystal
- **Memory device**
 - 256 Mbit DDR2 SDRAM
 - 64 Mbit NOR Flash
- **HUB75 Interface**
 - 16 HUB75 interfaces
- **Ethernet Interface**
 - Includes 2 Ethernet interfaces, supporting 10/100/1000Base-T
- **MCU**
 - One STM32F103C8T6 processor
- **Key & LEDs**
 - 1 key
 - 2 LEDs

3 Development Board Circuit

3.1 FPGA

3.1.1 Overview

For the resources of GW3A FPGA products, please refer to [*DS1351, GW3A series of FPGA Products*](#).

3.1.2 I/O Bank

For the I/O Bank, package, and pinout information, see [*UG1354, GW3A series of FPGA Products Package and Pinout User Guide*](#) for more details.

3.2 Power Supply

3.2.1 Introduction

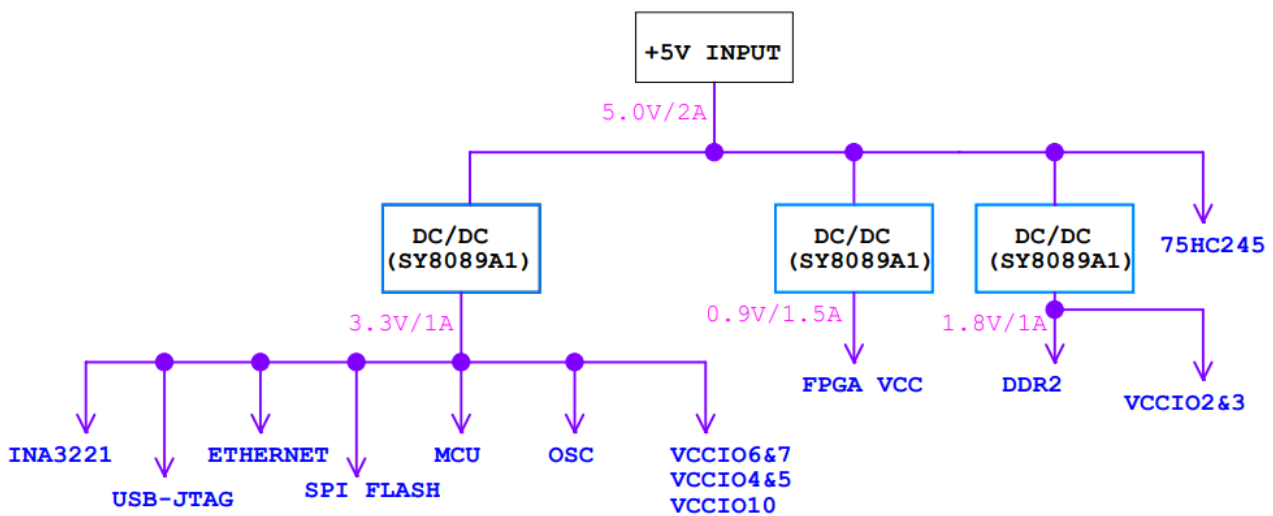
The development board needs to be powered by a 5V power adapter.

The input 5 V power supply is regulated by the PMIC on the development board to generate 3.3 V, 1.8 V, and 0.9 V power supplies, thus meeting the power supply requirements of the development board.

To facilitate accurate evaluation of the board's power consumption, an INA3221 current monitoring circuit is provided on-board, enabling current measurement for the FPGA's key power rails.

3.2.2 Power Assignment

Figure 3-1 Power Assignment Diagram



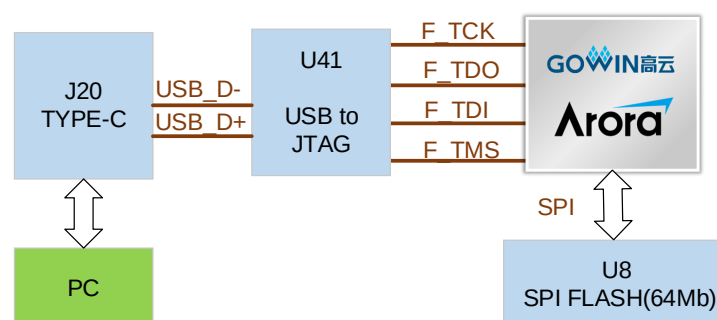
3.3 Download Module

3.3.1 Introduction

The development board is equipped with a USB Type-C download interface (J20) and a USB-JTAG chip (FTDI232). The interface supports programming the configuration file into the external SPI Flash or downloading it directly to the FPGA's internal SRAM.

The connection diagram is shown in Figure 3-2.

Figure 3-2 Connection Diagram of Download



3.3.2 Pin Assignment

Table 3-1 JTAG Pin Assignment

Signal Name	FPGA Pin No.	Bank	I/O Level	Description
F_TCK	A17	10	3.3V	JTAG signal
F_TDO	D15	10	3.3V	
F_TDI	D16	10	3.3V	
F_TMS	B18	10	3.3V	

Table 3-2 FLASH SPI Interface Pin Assignment

Signal Name	FPGA Pin No.	Bank	I/O Level	Description
QSPI_CS_N	V3	4	3.3V	Interface signals between SPI FLASH and FPGA
QSPI_CLK	R15	4	3.3V	
QSPI_IO0	T13	4	3.3V	
QSPI_IO1	R13	4	3.3V	
QSPI_IO2	T14	4	3.3V	
QSPI_IO3	V14	4	3.3V	

3.4 Clock

3.4.1 Introduction

The clock source provided on the development board for the FPGA includes one 50 MHz single-ended clock, which is connected to the FPGA's dedicated PLL input pin.

The GW3A-LV20UG324S device provides dedicated passive crystal oscillator input pins, OSC_XTP and OSC_XTN. An external 25 MHz passive crystal is connected to these pins to provide a clock signal to the FPGA.

The connection diagram of clock is shown in Figure 3-3.

Figure 3-3 Connection Diagram of Clock



3.4.2 Pin Assignment

Table 3-3 Clock Pin Assignment

Signal Name	FPGA Pin No.	Bank	I/O Level	Description
CLK_50MHz	B16	1	3.3V	50 MHz single-ended clock
OSC_XTP	N4	6	3.3V	25 MHz crystal
OSC_XTN	N3	6	3.3V	25 MHz crystal

3.5 DDR2

3.5.1 Introduction

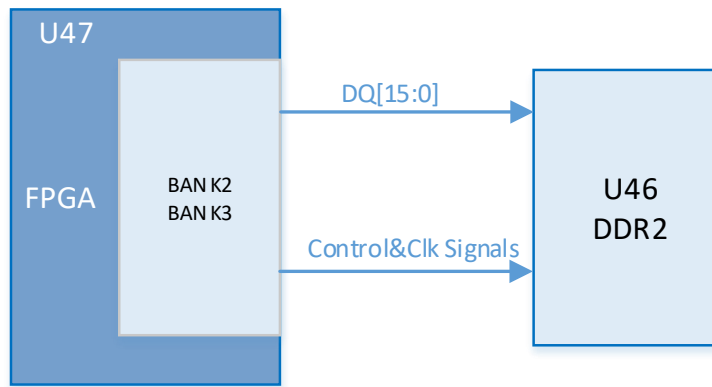
The development board is equipped with one 256-Mbit DDR2 chip (W9725G6KB25I). The signals of the DDR2 SDRAM are connected to the Bank 2 and Bank 3 of the FPGA. The specific information about DDR2 SDRAM is shown in Table 3-4.

Table 3-4 DDR2 SDRAM Information

Designator	Capacity
U46	16M x 16bit

The hardware connection diagram of DDR2 is shown in Figure 3-4.

Figure 3-4 Hardware Connection Diagram of DDR2



3.5.2 Pin Assignment

Table 3-5 DDR2 Pin Assignment

DDR2 Signal Name	FPGA Pin No.	Bank	I/O Level	Description
A0	L12	2	1.8V	Address
A1	H12	2	1.8V	Address
A2	L13	2	1.8V	Address
A3	L14	3	1.8V	Address
A4	N15	3	1.8V	Address
A5	M16	3	1.8V	Address
A6	M14	3	1.8V	Address
A7	N17	3	1.8V	Address
A8	U17	3	1.8V	Address
A9	P17	3	1.8V	Address
A10	L17	3	1.8V	Address
A11	T17	3	1.8V	Address
A12	P15	3	1.8V	Address
BA0	J16	3	1.8V	Bank address
BA1	K17	3	1.8V	Bank address
CS#	K12	2	1.8V	Chip select
CAS#	K13	2	1.8V	Column address strobe
CKE	F14	2	1.8V	Clock Enable
ODT	L15	3	1.8V	On-Die termination enable

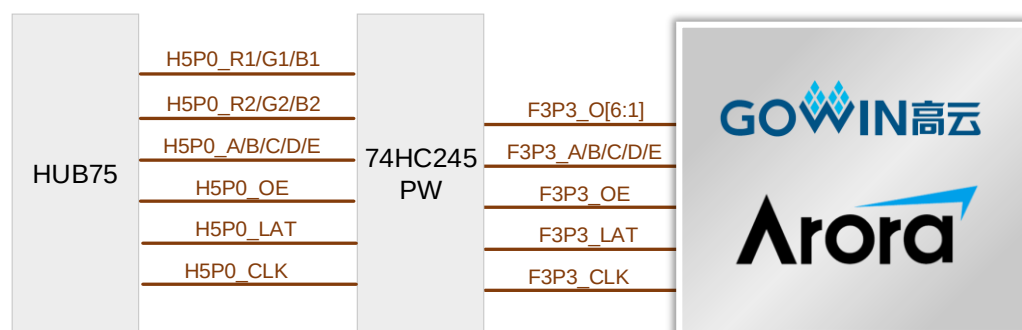
DDR2 Signal Name	FPGA Pin No.	Bank	I/O Level	Description
RAS#	G13	2	1.8V	Row address strobe
WE#	G14	2	1.8V	Write enable
CLK	H17	3	1.8V	Clock
CLK#	H18	3	1.8V	Clock
DQ0	G16	2	1.8V	Data
DQ1	G18	2	1.8V	Data
DQ2	K15	2	1.8V	Data
DQ3	H15	2	1.8V	Data
DQ4	H16	2	1.8V	Data
DQ5	K16	2	1.8V	Data
DQ6	F18	2	1.8V	Data
DQ7	F17	2	1.8V	Data
DQ8	H13	2	1.8V	Data
DQ9	H14	2	1.8V	Data
DQ10	F16	2	1.8V	Data
DQ11	E16	2	1.8V	Data
DQ12	E18	2	1.8V	Data
DQ13	F15	2	1.8V	Data
DQ14	C18	2	1.8V	Data
DQ15	C17	2	1.8V	Data
LDM	--	--	1.8V	Data mask (The FPGA does not use this I/O)
UDM	--	--	1.8V	Data mask (The FPGA does not use this I/O)
LDQS	J13	2	1.8V	Data strobe
LDQS#	K14	2	1.8V	Data strobe
UDQS	D17	2	1.8V	Data strobe
UDQS#	D18	2	1.8V	Data strobe

3.6 HUB75 Interface

3.6.1 Introduction

To facilitate functional verification of the LED receiving card, this development board provides 16 HUB75 interfaces. Each interface is driven by a 74HC245 device. Each interface includes six data signals, seven control signals, and one clock signal, following the commonly used industry-standard signal definition and pin assignment. A connection diagram of the HUB75 interface is shown in Figure 3-5.

Figure 3-5 Connection Diagram of HUB75 Interface



3.6.2 Pin Assignment I

The first group consists of eight HUB75 connectors, J4–J11. Each control signal and clock signal is shared by all eight HUB75 connectors and driven by a single FPGA I/O signal. For example, the signal output from FPGA pin B8 passes through a 74HC245 chip and drives the corresponding HOE signal on all eight HUB75 connectors.

Table 3-6 HUB75 J4 Connector Pin Assignment

J4 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
1	H5P0_O1	G6	7	3.3V	R1 data signal
2	H5P0_O2	F4	7	3.3V	G1 data signal
3	H5P0_O3	F5	7	3.3V	B1 data signal
4	GND	-	-	-	GND
5	H5P0_O4	F6	7	3.3V	R2 data signal
6	H5P0_O5	E1	7	3.3V	G2 data signal
7	H5P0_O6	E4	7	3.3V	B2 data signal

J4 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
8	H5P0_E1_1	C8	0	3.3V	HE (row select signal)
9	H5P0_A1_1	A7	0	3.3V	HA (row select signal)
10	H5P0_B1_1	C7	0	3.3V	HB (row select signal)
11	H5P0_C1_1	E6	0	3.3V	HC (row select signal)
12	H5P0_D1_1	A8	0	3.3V	HD (row select signal)
13	H5P0_CLK1_1	D6	0	3.3V	HCLK (clock signal)
14	H5P0_LAT1_1	E7	0	3.3V	HLAT (data latch signal)
15	H5P0_OE1_1	B8	0	3.3V	HOE (output enable signal)
16	GND	-	-	-	GND

Table 3-7 HUB75 J6 Connector Pin Assignment

J6 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
1	H5P0_O7	E3	7	3.3V	R1 data signal
2	H5P0_O8	D1	7	3.3V	G1 data signal
3	H5P0_O9	D2	7	3.3V	B1 data signal
4	GND	-	-	-	GND
5	H5P0_O10	C1	7	3.3V	R2 data signal
6	H5P0_O11	D3	7	3.3V	G2 data signal
7	H5P0_O12	C2	7	3.3V	B2 data signal
8	H5P0_E1_1	C8	0	3.3V	HE (row select signal)
9	H5P0_A1_1	A7	0	3.3V	HA (row select signal)
10	H5P0_B1_1	C7	0	3.3V	HB (row select signal)
11	H5P0_C1_1	E6	0	3.3V	HC (row select signal)
12	H5P0_D1_1	A8	0	3.3V	HD (row select signal)
13	H5P0_CLK1_2	D6	0	3.3V	HCLK (clock signal)
14	H5P0_LAT1_2	E7	0	3.3V	HLAT (data latch signal)
15	H5P0_OE1_2	B8	0	3.3V	HOE (output enable signal)

J6 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
16	GND	-	-	-	GND

Table 3-8 HUB75 J8 Connector Pin Assignment

J8 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
1	H5P0_O13	A2	0	3.3V	R1 data signal
2	H5P0_O14	B2	0	3.3V	G1 data signal
3	H5P0_O15	A3	0	3.3V	B1 data signal
4	GND	-	-	-	GND
5	H5P0_O16	B3	0	3.3V	R2 data signal
6	H5P0_O17	A4	0	3.3V	G2 data signal
7	H5P0_O18	B4	0	3.3V	B2 data signal
8	H5P0_E1_2	C8	0	3.3V	HE (row select signal)
9	H5P0_A1_2	A7	0	3.3V	HA (row select signal)
10	H5P0_B1_2	C7	0	3.3V	HB (row select signal)
11	H5P0_C1_2	E6	0	3.3V	HC (row select signal)
12	H5P0_D1_2	A8	0	3.3V	HD (row select signal)
13	H5P0_CLK1_3	D6	0	3.3V	HCLK (clock signal)
14	H5P0_LAT1_3	E7	0	3.3V	HLAT (data latch signal)
15	H5P0_OE1_3	B8	0	3.3V	HOE (output enable signal)
16	GND	-	-	-	GND

Table 3-9 HUB75 J10 Connector Pin Assignment

J10 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
1	H5P0_O19	C4	0	3.3V	R1 data signal
2	H5P0_O20	A5	0	3.3V	G1 data signal
3	H5P0_O21	C5	0	3.3V	B1 data signal
4	GND	-	-	-	GND
5	H5P0_O22	A6	0	3.3V	R2 data signal
6	H5P0_O23	B6	0	3.3V	G2 data signal

J10 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
7	H5P0_O24	C6	0	3.3V	B2 data signal
8	H5P0_E1_2	C8	0	3.3V	HE (row select signal)
9	H5P0_A1_2	A7	0	3.3V	HA (row select signal)
10	H5P0_B1_2	C7	0	3.3V	HB (row select signal)
11	H5P0_C1_2	E6	0	3.3V	HC (row select signal)
12	H5P0_D1_2	A8	0	3.3V	HD (row select signal)
13	H5P0_CLK1_4	D6	0	3.3V	HCLK (clock signal)
14	H5P0_LAT1_4	E7	0	3.3V	HLAT (data latch signal)
15	H5P0_OE1_4	B8	0	3.3V	HOE (output enable signal)
16	GND	-	-	-	GND

Table 3-10 HUB75 J5 Connector Pin Assignment

J5 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
1	H5P0_O25	D9	0	3.3V	R1 data signal
2	H5P0_O26	E8	0	3.3V	G1 data signal
3	H5P0_O27	A9	0	3.3V	B1 data signal
4	GND	-	-	-	GND
5	H5P0_O28	B9	0	3.3V	R2 data signal
6	H5P0_O29	C9	0	3.3V	G2 data signal
7	H5P0_O30	D8	0	3.3V	B2 data signal
8	H5P0_E1_3	C8	0	3.3V	HE (row select signal)
9	H5P0_A1_3	A7	0	3.3V	HA (row select signal)
10	H5P0_B1_3	C7	0	3.3V	HB (row select signal)
11	H5P0_C1_3	E6	0	3.3V	HC (row select signal)
12	H5P0_D1_3	A8	0	3.3V	HD (row select signal)
13	H5P0_CLK1_5	D6	0	3.3V	HCLK (clock signal)
14	H5P0_LAT1_5	E7	0	3.3V	HLAT (data latch signal)

J5 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
15	H5P0_OE1_5	B8	0	3.3V	HOE (output enable signal)
16	GND	-	-	-	GND

Table 3-11 HUB75 J7 Connector Pin Assignment

J7 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
1	H5P0_O31	A10	1	3.3V	R1 data signal
2	H5P0_O32	C10	1	3.3V	G1 data signal
3	H5P0_O33	A11	1	3.3V	B1 data signal
4	GND	-	-	-	GND
5	H5P0_O34	B11	1	3.3V	R2 data signal
6	H5P0_O35	C11	1	3.3V	G2 data signal
7	H5P0_O36	D11	1	3.3V	B2 data signal
8	H5P0_E1_3	C8	0	3.3V	HE (row select signal)
9	H5P0_A1_3	A7	0	3.3V	HA (row select signal)
10	H5P0_B1_3	C7	0	3.3V	HB (row select signal)
11	H5P0_C1_3	E6	0	3.3V	HC (row select signal)
12	H5P0_D1_3	A8	0	3.3V	HD (row select signal)
13	H5P0_CLK1_6	D6	0	3.3V	HCLK (clock signal)
14	H5P0_LAT1_6	E7	0	3.3V	HLAT (data latch signal)
15	H5P0_OE1_6	B8	0	3.3V	HOE (output enable signal)
16	GND	-	-	-	GND

Table 3-12 HUB75 J9 Connector Pin Assignment

J9 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
1	H5P0_O37	E11	1	3.3V	R1 data signal
2	H5P0_O38	A12	1	3.3V	G1 data signal
3	H5P0_O39	B12	1	3.3V	B1 data signal
4	GND	-	-	-	GND

J9 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
5	H5P0_O40	C12	1	3.3V	R2 data signal
6	H5P0_O41	D12	1	3.3V	G2 data signal
7	H5P0_O42	E12	1	3.3V	B2 data signal
8	H5P0_E1_4	C8	0	3.3V	HE (row select signal)
9	H5P0_A1_4	A7	0	3.3V	HA (row select signal)
10	H5P0_B1_4	C7	0	3.3V	HB (row select signal)
11	H5P0_C1_4	E6	0	3.3V	HC (row select signal)
12	H5P0_D1_4	A8	0	3.3V	HD (row select signal)
13	H5P0_CLK1_7	D6	0	3.3V	HCLK (clock signal)
14	H5P0_LAT1_7	E7	0	3.3V	HLAT (data latch signal)
15	H5P0_OE1_7	B8	0	3.3V	HOE (output enable signal)
16	GND	-	-	-	GND

Table 3-13 HUB75 J11 Connector Pin Assignment

J11 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
1	H5P0_O43	A13	1	3.3V	R1 data signal
2	H5P0_O44	C13	1	3.3V	G1 data signal
3	H5P0_O45	E13	1	3.3V	B1 data signal
4	GND	-	-	-	GND
5	H5P0_O46	A14	1	3.3V	R2 data signal
6	H5P0_O47	B14	1	3.3V	G2 data signal
7	H5P0_O48	C14	1	3.3V	B2 data signal
8	H5P0_E1_4	C8	0	3.3V	HE (row select signal)
9	H5P0_A1_4	A7	0	3.3V	HA (row select signal)
10	H5P0_B1_4	C7	0	3.3V	HB (row select signal)
11	H5P0_C1_4	E6	0	3.3V	HC (row select signal)
12	H5P0_D1_4	A8	0	3.3V	HD (row select signal)
13	H5P0_CLK1_8	D6	0	3.3V	HCLK (clock signal)
14	H5P0_LAT1_8	E7	0	3.3V	HLAT (data latch

J11 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
					signal)
15	H5P0_OE1_8	B8	0	3.3V	HOE (output enable signal)
16	GND	-	-	-	GND

3.6.3 Pin Assignment II

The second group consists of eight HUB75 connectors, J12–J19. Each control signal and clock signal is shared by all eight HUB75 connectors and driven by a single FPGA I/O signal. For example, the signal output from FPGA pin V8 passes through a 74HC245 chip and drives the corresponding HOE signal on all eight HUB75 connectors.

Table 3-14 HUB75 J12 Connector Pin Assignment

J12 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
1	H5P0_O49	U2	6	3.3V	R1 data signal
2	H5P0_O50	U1	6	3.3V	G1 data signal
3	H5P0_O51	T2	6	3.3V	B1 data signal
4	GND	-	-	-	GND
5	H5P0_O52	T1	6	3.3V	R2 data signal
6	H5P0_O53	R3	5	3.3V	G2 data signal
7	H5P0_O54	P2	6	3.3V	B2 data signal
8	H5P0_E2_1	U8	5	3.3V	HE (row select signal)
9	H5P0_A2_1	R8	4	3.3V	HA (row select signal)
10	H5P0_B2_1	T8	4	3.3V	HB (row select signal)
11	H5P0_C2_1	N8	5	3.3V	HC (row select signal)
12	H5P0_D2_1	P8	5	3.3V	HD (row select signal)
13	H5P0_CLK2_1	T5	5	3.3V	HCLK (clock signal)
14	H5P0_LAT2_1	T6	5	3.3V	HLAT (data latch signal)
15	H5P0_OE2_1	V8	5	3.3V	HOE (output enable signal)
16	GND	-	-	-	GND

Table 3-15 HUB75 J14 Connector Pin Assignment

J14 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
1	H5P0_O55	R5	5	3.3V	R1 data signal
2	H5P0_O56	T4	5	3.3V	G1 data signal
3	H5P0_O57	T3	5	3.3V	B1 data signal
4	GND	-	-	-	GND
5	H5P0_O58	N5	5	3.3V	R2 data signal
6	H5P0_O59	P4	6	3.3V	G2 data signal
7	H5P0_O60	P3	6	3.3V	B2 data signal
8	H5P0_E2_1	U8	5	3.3V	HE (row select signal)
9	H5P0_A2_1	R8	4	3.3V	HA (row select signal)
10	H5P0_B2_1	T8	4	3.3V	HB (row select signal)
11	H5P0_C2_1	N8	5	3.3V	HC (row select signal)
12	H5P0_D2_1	P8	5	3.3V	HD (row select signal)
13	H5P0_CLK2_2	T5	5	3.3V	HCLK (clock signal)
14	H5P0_LAT2_2	T6	5	3.3V	HLAT (data latch signal)
15	H5P0_OE2_2	V8	5	3.3V	HOE (output enable signal)
16	GND	-	-	-	GND

Table 3-16 HUB75 J16 Connector Pin Assignment

J16 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
1	H5P0_O61	P7	5	3.3V	R1 data signal
2	H5P0_O62	U5	5	3.3V	G1 data signal
3	H5P0_O63	P6	5	3.3V	B1 data signal
4	GND	-	-	-	GND
5	H5P0_O64	V5	5	3.3V	R2 data signal
6	H5P0_O65	N6	5	3.3V	G2 data signal
7	H5P0_O66	V4	5	3.3V	B2 data signal
8	H5P0_E2_2	U8	5	3.3V	HE (row select signal)

J16 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
9	H5P0_A2_2	R8	4	3.3V	HA (row select signal)
10	H5P0_B2_2	T8	4	3.3V	HB (row select signal)
11	H5P0_C2_2	N8	5	3.3V	HC (row select signal)
12	H5P0_D2_2	P8	5	3.3V	HD (row select signal)
13	H5P0_CLK2_3	T5	5	3.3V	HCLK (clock signal)
14	H5P0_LAT2_3	T6	5	3.3V	HLAT (data latch signal)
15	H5P0_OE2_3	V8	5	3.3V	HOE (output enable signal)
16	GND	-	-	-	GND

Table 3-17 HUB75 J18 Connector Pin Assignment

J18 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
1	H5P0_O67	V7	5	3.3V	R1 data signal
2	H5P0_O68	R7	5	3.3V	G1 data signal
3	H5P0_O69	T7	5	3.3V	B1 data signal
4	GND	-	-	-	GND
5	H5P0_O70	N7	5	3.3V	R2 data signal
6	H5P0_O71	U7	5	3.3V	G2 data signal
7	H5P0_O72	V6	5	3.3V	B2 data signal
8	H5P0_E2_2	U8	5	3.3V	HE (row select signal)
9	H5P0_A2_2	R8	4	3.3V	HA (row select signal)
10	H5P0_B2_2	T8	4	3.3V	HB (row select signal)
11	H5P0_C2_2	N8	5	3.3V	HC (row select signal)
12	H5P0_D2_2	P8	5	3.3V	HD (row select signal)
13	H5P0_CLK2_4	T5	5	3.3V	HCLK (clock signal)
14	H5P0_LAT2_4	T6	5	3.3V	HLAT (data latch signal)
15	H5P0_OE2_4	V8	5	3.3V	HOE (output enable signal)

J18 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
16	GND	-	-	-	GND

Table 3-18 HUB75 J13 Connector Pin Assignment

J13 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
1	H5P0_O73	M11	4	3.3V	R1 data signal
2	H5P0_O74	N10	4	3.3V	G1 data signal
3	H5P0_O75	V10	4	3.3V	B1 data signal
4	GND	-	-	-	GND
5	H5P0_O76	V9	4	3.3V	R2 data signal
6	H5P0_O77	T9	4	3.3V	G2 data signal
7	H5P0_O78	N9	5	3.3V	B2 data signal
8	H5P0_E2_3	U8	5	3.3V	HE (row select signal)
9	H5P0_A2_3	R8	4	3.3V	HA (row select signal)
10	H5P0_B2_3	T8	4	3.3V	HB (row select signal)
11	H5P0_C2_3	N8	5	3.3V	HC (row select signal)
12	H5P0_D2_3	P8	5	3.3V	HD (row select signal)
13	H5P0_CLK2_5	T5	5	3.3V	HCLK (clock signal)
14	H5P0_LAT2_5	T6	5	3.3V	HLAT (data latch signal)
15	H5P0_OE2_5	V8	5	3.3V	HOE (output enable signal)
16	GND	-	-	-	GND

Table 3-19 HUB75 J15 Connector Pin Assignment

J15 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
1	H5P0_O79	R11	4	3.3V	R1 data signal
2	H5P0_O80	U11	4	3.3V	G1 data signal
3	H5P0_O81	V11	4	3.3V	B1 data signal
4	GND	-	-	-	GND

J15 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
5	H5P0_O82	T10	4	3.3V	R2 data signal
6	H5P0_O83	R10	4	3.3V	G2 data signal
7	H5P0_O84	U10	4	3.3V	B2 data signal
8	H5P0_E2_3	U8	5	3.3V	HE (row select signal)
9	H5P0_A2_3	R8	4	3.3V	HA (row select signal)
10	H5P0_B2_3	T8	4	3.3V	HB (row select signal)
11	H5P0_C2_3	N8	5	3.3V	HC (row select signal)
12	H5P0_D2_3	P8	5	3.3V	HD (row select signal)
13	H5P0_CLK2_6	T5	5	3.3V	HCLK (clock signal)
14	H5P0_LAT2_6	T6	5	3.3V	HLAT (data latch signal)
15	H5P0_OE2_6	V8	5	3.3V	HOE (output enable signal)
16	GND	-	-	-	GND

Table 3-20 HUB75 J17 Connector Pin Assignment

J17 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
1	H5P0_O85	P12	4	3.3V	R1 data signal
2	H5P0_O86	V12	4	3.3V	G1 data signal
3	H5P0_O87	N11	4	3.3V	B1 data signal
4	GND	-	-	-	GND
5	H5P0_O88	P11	4	3.3V	R2 data signal
6	H5P0_O89	T12	4	3.3V	G2 data signal
7	H5P0_O90	T11	4	3.3V	B2 data signal
8	H5P0_E2_4	U8	5	3.3V	HE (row select signal)
9	H5P0_A2_4	R8	4	3.3V	HA (row select signal)
10	H5P0_B2_4	T8	4	3.3V	HB (row select signal)
11	H5P0_C2_4	N8	5	3.3V	HC (row select signal)
12	H5P0_D2_4	P8	5	3.3V	HD (row select signal)
13	H5P0_CLK2_7	T5	5	3.3V	HCLK (clock signal)

J17 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
14	H5P0_LAT2_7	T6	5	3.3V	HLAT (data latch signal)
15	H5P0_OE2_7	V8	5	3.3V	HOE (output enable signal)
16	GND	-	-	-	GND

Table 3-21 HUB75 J19 Connector Pin Assignment

J19 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
1	H5P0_O91	U16	4	3.3V	R1 data signal
2	H5P0_O92	V16	4	3.3V	G1 data signal
3	H5P0_O93	U15	4	3.3V	B1 data signal
4	GND	-	-	-	GND
5	H5P0_O94	V15	4	3.3V	R2 data signal
6	H5P0_O95	U13	4	3.3V	G2 data signal
7	H5P0_O96	V13	4	3.3V	B2 data signal
8	H5P0_E2_4	U8	5	3.3V	HE (row select signal)
9	H5P0_A2_4	R8	4	3.3V	HA (row select signal)
10	H5P0_B2_4	T8	4	3.3V	HB (row select signal)
11	H5P0_C2_4	N8	5	3.3V	HC (row select signal)
12	H5P0_D2_4	P8	5	3.3V	HD (row select signal)
13	H5P0_CLK2_8	T5	5	3.3V	HCLK (clock signal)
14	H5P0_LAT2_8	T6	5	3.3V	HLAT (data latch signal)
15	H5P0_OE2_8	V8	5	3.3V	HOE (output enable signal)
16	GND	-	-	-	GND

3.7 Ethernet Interface

3.7.1 Introduction

The development board has two Ethernet interfaces (RTL8211E), which support 10/100/1000Base-T. The connection diagram of the interface is shown in Figure 3-6.

Figure 3-6 Connection Diagram of Ethernet Interface



3.7.2 Pin Assignment

Table 3-22 U42 RGMII Interface Pin Assignment

U42 Pin Signal	FPGA Pin No.	Bank	I/O Level	Description
PHY2_GTCLK	M1	6	3.3V	TX clock
PHY2_TXEN	K3	6	3.3V	TX enable
PHY2_TXD0	L1	6	3.3V	TX data
PHY2_TXD1	L4	6	3.3V	TX data
PHY2_TXD2	L3	6	3.3V	TX data
PHY2_TXD3	L2	6	3.3V	TX data
PHY2_RXC	K4	6	3.3V	RX clock
PHY2_RXDV	P1	6	3.3V	RX enable
PHY2_RXD0	N2	6	3.3V	RX data
PHY2_RXD1	N1	6	3.3V	RX data
PHY2_RXD2	M5	6	3.3V	RX data
PHY2_RXD3	M3	6	3.3V	RX data
F_PHY_RST_N	F3	7	3.3V	Reset signal
F_PHY2_CLK125	L5	7	3.3V	125 MHz clock output

U42 Pin Signal	FPGA Pin No.	Bank	I/O Level	Description
PHY_MDC	K5	7	3.3V	Management data clock
PHY_MDIO	K6	7	3.3V	Management data input/output
F_PHY2_CLK	H6	7	3.3V	Backup clock signal for the PHY2 chip

Table 3-23 U43 RGMII Interface Pin Assignment

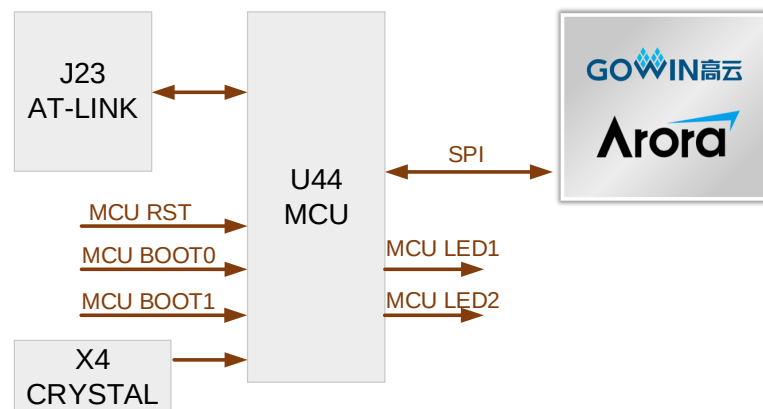
U43 Pin Signal	FPGA Pin No.	Bank	I/O Level	Description
PHY1_GTCLK	H3	7	3.3V	TX clock
PHY1_TXEN	F2	7	3.3V	TX enable
PHY1_TXD0	H5	7	3.3V	TX data
PHY1_TXD1	G1	7	3.3V	TX data
PHY1_TXD2	G3	7	3.3V	TX data
PHY1_TXD3	F1	7	3.3V	TX data
PHY1_RXC	H4	7	3.3V	RX clock
PHY1_RXDV	K1	6	3.3V	RX enable
PHY1_RXD0	K2	6	3.3V	RX data
PHY1_RXD1	J1	6	3.3V	RX data
PHY1_RXD2	J3	6	3.3V	RX data
PHY1_RXD3	H1	6	3.3V	RX data
F_PHY_RST_N	F3	7	3.3V	Reset signal
F_PHY1_CLK125	H2	6	3.3V	125 MHz clock output
PHY_MDC	K5	7	3.3V	Management data clock
PHY_MDIO	K6	7	3.3V	Management data input/output
F_PHY1_CLK	L6	6	3.3V	Backup clock signal for the PHY1 chip

3.8 MCU

3.8.1 Introduction

This development board has a reserved MCU circuit (model STM32F103C8T6), and an SPI interface is reserved between the MCU and the FPGA for data exchange. The external connection diagram of the MCU is shown in Figure 3-7.

Figure 3-7 External Connection Diagram of the MCU



3.8.2 Pin Assignment

Table 3-24 Pin Assignment for Connecting the MCU and the FPGA

U44 Pin No.	Signal Name	FPGA Pin No.	Bank	I/O Level	Description
14	F_MCU_SPI_NSS	C15	1	3.3V	Chip select signal
15	F_MCU_SPI_SCK	D14	1	3.3V	Clock signal
16	F_MCU_SPI_MISO	A16	1	3.3V	Master In, Slave Out
17	F_MCU_SPI_MOSI	A15	1	3.3V	Master Out, Slave In

Table 3-25 Pin Assignment for Connecting the MCU and AT-LINK

J23 Pin No.	Signal Name	U44 Pin No.	IO Level	Description
1	VCC3P3	-	3.3V	Power
2	VCC5P0	-	5V	Power
3	MCU_SWDIO	34	3.3V	Serial Wire Data Input/Output

J23 Pin No.	Signal Name	U44 Pin No.	IO Level	Description
4	MCU_BOOT0	44	3.3V	BOOT0 signal
5	MCU_SWCLK	37	3.3V	Serial Wire Clock
6	MCU_SWO	39	3.3V	Serial Wire Output
7	MCU_NIRST	7	3.3V	Reset signal
8	MCU_UART_RX	31	3.3V	UART Signal
9	GND	-	-	GND
10	MCU_UART_TX	30	3.3V	UART signal

Table 3-26 Pin Assignment for Connecting the MCU and LED, RST, BOOT

U44 Pin No.	Signal Name	IO Level	Description
7	MCU_NIRST	3.3V	Reset signal
44	MCU_BOOT0	3.3V	BOOT0
20	MCU_BOOT1	3.3V	BOOT1
46	MCU_LED1	3.3V	LED
45	MCU_LED2	3.3V	LED

Table 3-27 Pin Assignment for Connecting the MCU and the CRYSTAL

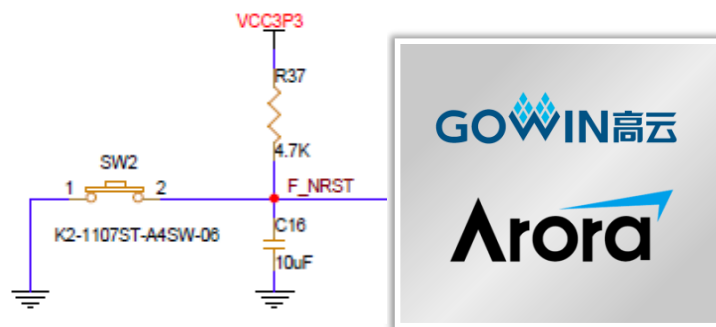
U44 Pin No.	Signal Name	X4 Pin No.
5	X_OSC_IN	1
6	X_OSC_OUT	3

3.9 Key & LEDs

3.9.1 Introduction

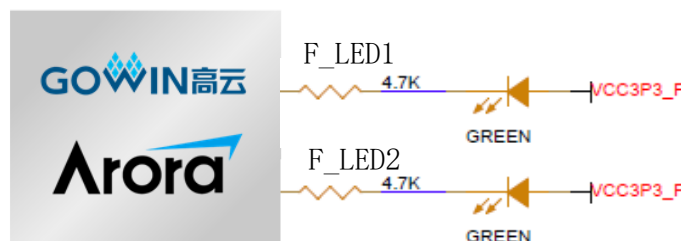
The DK_LED-RxCard_GW3A-LV20UG324S_V2.1 development board is equipped with one key. When the key is pressed, the corresponding IO input voltage of the FPGA is driven low, and when the key is released, the corresponding IO input voltage of the FPGA is driven high. The connection diagram is shown in Figure 3-8.

Figure 3-8 Connection Diagram of the Key



The development board has two user LEDs that can be controlled to turn on and off via the program. When the corresponding IO voltage is low, the user LED turns on; when the connected IO voltage is high, the user LED turns off. The connection diagram is shown in Figure 3-9.

Figure 3-9 Connection Diagram of LED



3.9.2 Pin Assignment

Table 3-28 Key & LED Pin Assignment

Signal Name	FPGA Pin No.	Bank	I/O Level	Description
F_NRST	J6	7	3.3V	Key
F_LED1	F12	1	3.3V	LED
F_LED2	F13	1	3.3V	LED

4 Precautions for Using the Development Board

Handle the development board with care and follow proper electrostatic discharge (ESD) protection procedures during use.

