



DK_PCIE_GW5AT-LV60UG324_V1.1

User Guide

DBUG1290-1.0E, 04/10/2026

Copyright © 2026 Guangdong Gowin Semiconductor Corporation. All Rights Reserved.

 is the trademark of Guangdong Gowin Semiconductor Corporation and is registered in China, the U.S. Patent and Trademark Office, and other countries. All other words and logos identified as trademarks or service marks are the property of their respective holders. No part of this document may be reproduced or transmitted in any form or by any means, electronic, mechanical, photocopying, recording or otherwise, without the prior written consent of GOWINSEMI.

Disclaimer

GOWINSEMI, LittleBee, Arora, and the GOWINSEMI logos are trademarks of GOWINSEMI and are registered in China, the U.S. Patent and Trademark Office, and other countries. GOWINSEMI assumes no liability and provides no warranty (either expressed or implied) and is not responsible for any damage incurred to your hardware, software, data, or property resulting from usage of the materials or intellectual property except as outlined in the GOWINSEMI Terms and Conditions of Sale. GOWINSEMI may make changes to this document at any time without prior notice. Anyone relying on this documentation should contact GOWINSEMI for the current documentation and errata.

Revision History

Date	Version	Description
04/10/2026	1.0E	Initial version published.

Contents

Contents	i
List of Figures	iii
List of Tables	iv
1 About This Guide	1
1.1 Purpose	1
1.2 Related Documents	1
1.3 Terminology and Abbreviations	1
1.4 Support and Feedback	2
2 Development Board Introduction	3
2.1 Overview	3
2.2 A Development Board Kit	4
2.3 PCB Components	5
2.4 System Block Diagram	5
2.5 Features	6
3 Development Board Circuit	8
3.1 FPGA	8
3.1.1 Overview	8
3.1.2 I/O BANK	8
3.2 Power Supply	8
3.2.1 Introduction	8
3.2.2 Power Distribution	9
3.3 Download Modules	9
3.3.1 Introduction	9
3.3.2 Pin Distribution	9
3.4 Clock	10

3.4.1 Introduction	10
3.4.2 Pin Distribution.....	10
3.5 DDR3	11
3.5.1 Introduction	11
3.5.2 Pin Distribution.....	11
3.6 PCIE Interface	14
3.6.1 Introduction	14
3.6.2 Pin Distribution.....	15
3.7 ADC Interface	16
3.7.1 Introduction	16
3.7.2 Pin Distribution.....	16
3.8 MIPI C-PHY Interface (Hard Core)	17
3.8.1 Introduction	17
3.8.2 Pin Distribution.....	17
3.9 MIPI D-PHY Interface (Hard Core)	18
3.9.1 Introduction	18
3.9.2 Pin Distribution.....	19
3.10 MIPI D-PHY Interface (Soft Core)	20
3.10.1 Introduction	20
3.10.2 Pin Distribution.....	21
3.11 LVDS Interface	22
3.11.1 Introduction	22
3.11.2 Pin Distribution	22
3.12 Key & Indicator	23
3.12.1 Introduction	23
3.12.2 Pin Distribution.....	24
3.13 GPIO	25
3.13.1 Introduction	25
3.13.2 Pin Distribution.....	25
4 Precaution	27

List of Figures

Figure 2-1 DK_PCIE_GW5AT-LV60UG324_V1.1 Development Board	3
Figure 2-2 A Development Board Kit	4
Figure 2-3 PCB Components.....	5
Figure 2-4 System Block Diagram	5
Figure 3-1 Power Distribution Diagram	9
Figure 3-2 Connection Diagram of Download	9
Figure 3-3 Clock Connection Diagram	10
Figure 3-4 Hardware Connection Diagram of DDR3.....	11
Figure 3-5 Connection Diagram of PCIE Interface.....	14
Figure 3-6 PCIE_PRSENT Connection Diagram.....	15
Figure 3-7 Connection Diagram of ADC Interface Schematic.....	16
Figure 3-8 Connection Diagram of MIPI C-PHY (Hard Core) Interface.....	17
Figure 3-9 Connection Diagram of MIPI D-PHY (Hard Core) Interface.....	19
Figure 3-10 Connection Diagram of MIPI D-PHY (Soft Core) Interface	21
Figure 3-11 Connection Diagram of LVDS Interface	22
Figure 3-12 Connection Diagram of Key	24
Figure 3-13 Connection Diagram of LED	24
Figure 3-14 Connection Diagram of GPIO Interface	25

List of Tables

Table 1-1 Terminology and Abbreviations	1
Table 3-1 JTAG Pin Distribution	9
Table 3-2 Clock Pin Distribution	10
Table 3-3 DDR3 Configuration	11
Table 3-4 DDR3 Pin Distribution	11
Table 3-5 Pin Distribution of PCIe Interface	15
Table 3-6 Pin Distribution of ADC Interface	16
Table 3-7 Pin Distribution of MIPI C-PHY (Hard Core) Interface	17
Table 3-8 Pin Distribution of MIPI D-PHY (Hard Core) Interface	19
Table 3-9 Pin Distribution of MIPI D-PHY (Soft Core) Interface	21
Table 3-10 Pin Distribution of LVDS Interface	22
Table 3-11 Pin Distribution of Key	24
Table 3-12 Pin Distribution of Indicators	24
Table 3-13 Pin Distribution of GPIO Interface	25

1 About This Guide

1.1 Purpose

The DK_PCIE_GW5AT-LV60UG324_V1.1 development board (hereinafter referred to as "the development board") user guide consists of following three parts:

- A brief introduction to the features of the development board.
- An introduction to the development board system architecture and hardware resources.
- An introduction to the hardware circuits, functions and pin distribution.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [UG1222, GW5AT-60 Pinout](#)
- [UG983, GW5AT series of FPGA Products Package and Pinout User Guide](#)
- [UG718, Arora V 60K FPGA Products Programming and Configuration User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
DDR	Double Data Rate

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable I/O
JTAG	Joint Test Action Group
LDO	Low Dropout Regulator
PCIE	Peripheral Component Interconnect Express

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Development Board Introduction

2.1 Overview

Figure 2-1 DK_PCIE_GW5AT-LV60UG324_V1.1 Development Board



Gowin GW5AT series of FPGA products are the 5 series products of Arora family, with abundant internal resources, high-performance DSP with a new architecture that supports AI operations, high-speed interfaces such as SerDes, MIPI, and LVDS, as well as rich BSRAM memory resources. It is suitable for applications such as low power, high performance and compatibility design.

DK_PCIE_GW5AT-LV60UG324_V1.1 development board integrates DDR3, LVDS, MIPI, PCIe, and hard ADC interfaces, meeting a wide range of application requirements, including FPGA functional evaluation, hardware reliability verification, and software development and debugging.

The development board uses Gowin GW5AT-LV60UG324 FPGA device. For the internal resources of the chip, see [DS981, GW5AT series](#)

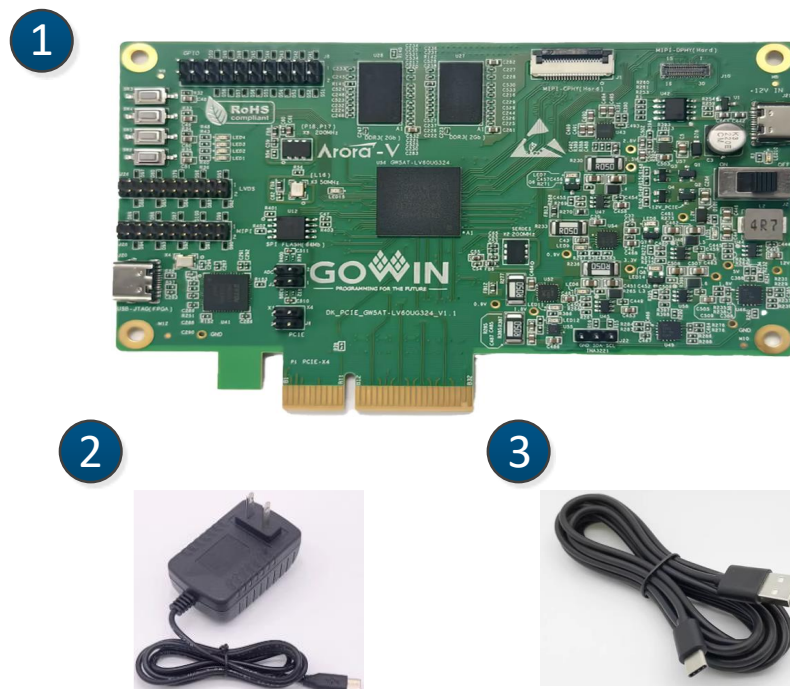
[of FPGA Products Data Sheet.](#)

2.2 A Development Board Kit

The development board kit includes the following items:

1. DK_PCIE_GW5AT-LV60UG324_V1.1 development board
2. 12V input Type-C power adapter (Input: AC 100-240V~50/60Hz 0.6A, output: DC12V 2A)
3. Type-A to Type-C interface data cable

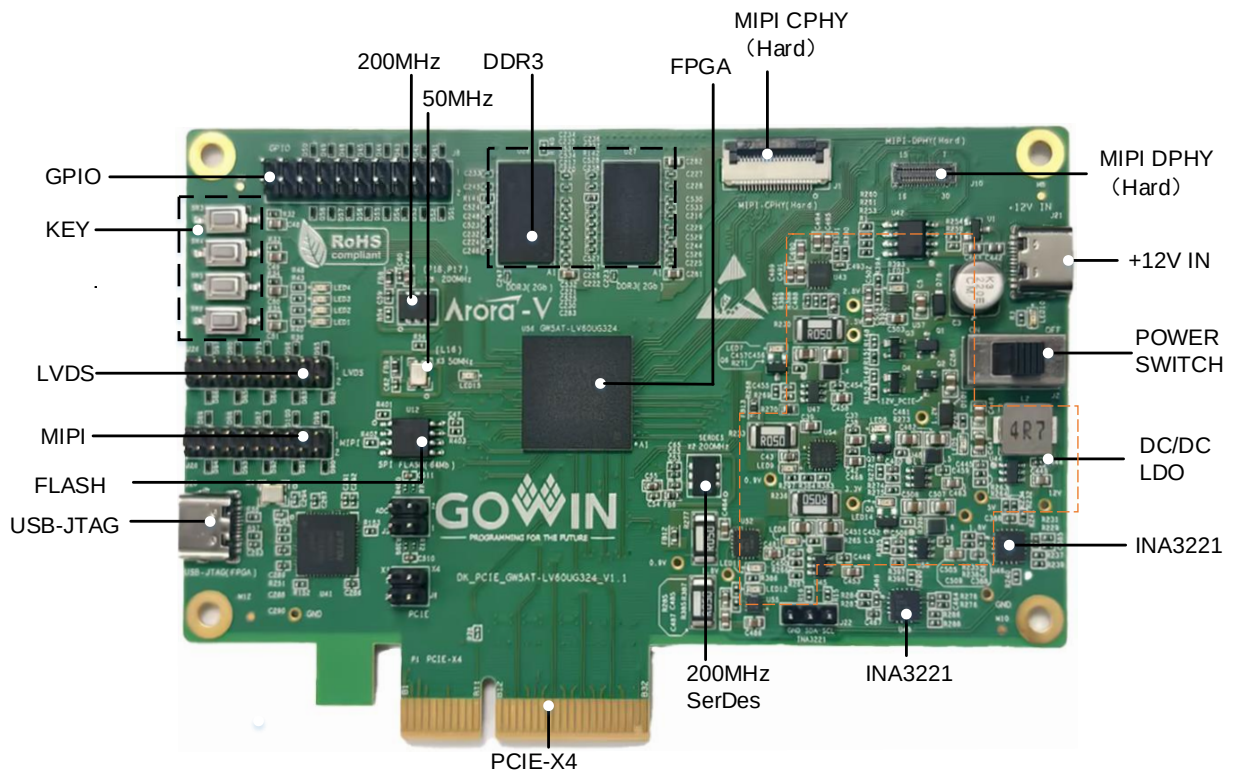
Figure 2-2 A Development Board Kit



- ① DK_PCIE_GW5AT-LV60UG324_V1.1 development board
- ② 12V input Type-C power adapter
- ③ Type-A to Type-C interface data cable

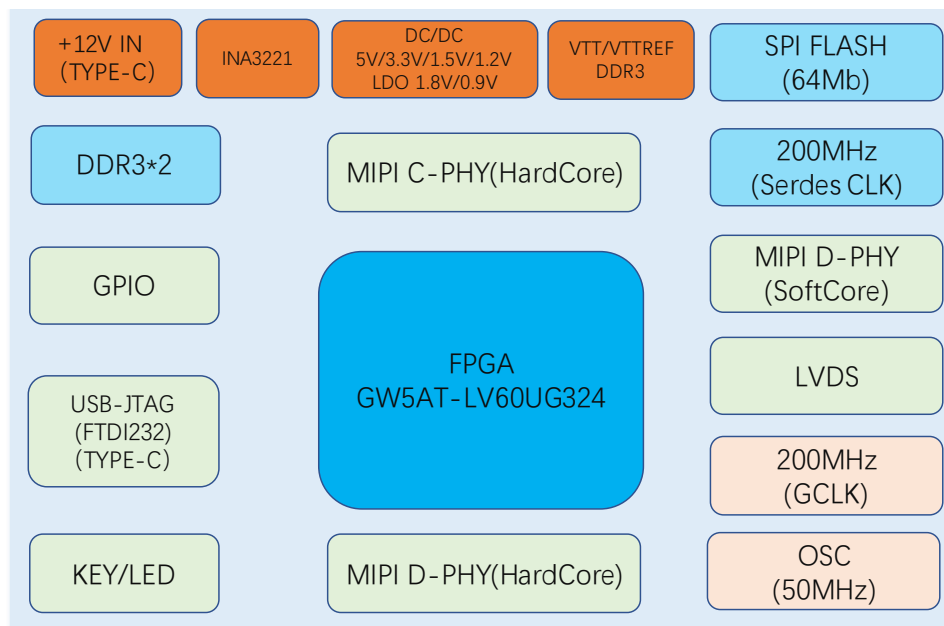
2.3 PCB Components

Figure 2-3 PCB Components



2.4 System Block Diagram

Figure 2-4 System Block Diagram



2.5 Features

The key features are as follows:

- **FPGA device**
 - Gowin GW5AT-LV60UG324 FPGA
- **Download and boot**
 - Integrates USB download circuit on the development board; downloads through Type- C interface
 - External SPI Flash Boot
- **Power supply**
 - Powered by external DC 12V or via PCIe slot
 - The Power LED is on after power on
 - The board generates 5V, 3.3V, 2.8V, 1.8V, 1.5V, 1.2V, 0.9V, 0.75V power rails
- **Clock system**
 - 50 MHz single-ended clock
 - 200 MHz differential clock (GCLK)
 - 200 MHz differential clock (SerDes)
- **Memory device**
 - 4 Gbit DDR3 SDRAM
 - 64 Mbit NOR Flash
- **PCIe interface**
 - PCIE-X4 interface, supporting PCIe Gen2/Gen3
- **MIPI C-PHY Interface (Hard Core)**
 - One C-PHY hard core interface, consisting of 3 data lanes, supporting RX/TX at 2 Gbps.
- **MIPI D-PHY Interface (Hard Core)**
 - One D-PHY hard core interface, consisting of 4 data lanes + 1 clock lane, supporting RX/TX at 2.5 Gbps.
- **MIPI D-PHY Interface (Soft Core)**
 - One D-PHY soft core interface, consisting of 4 data lanes + 1 clock lane, supporting RX/TX at 1.5 Gbps.
- **LVDS interface**
 - One LVDS interface, consisting of 4 data lanes + 1 clock lane, supporting RX/TX at 1.5 Gbps.
- **ADC interface**
 - 2 ADC interfaces
- **Key & Indicator**
 - 4 keys
 - 4 LED indicators

- GPIO
 - 16 GPIOs

3 Development Board Circuit

3.1 FPGA

3.1.1 Overview

For the resources of GW5AT FPGA products, please refer to [DS981, GW5AT series of FPGA Products](#).

3.1.2 I/O BANK

For the I/O BANK, package, and pinout information, see [UG983, GW5AT series of FPGA Products Package and Pinout User Guide](#) for more details.

3.2 Power Supply

3.2.1 Introduction

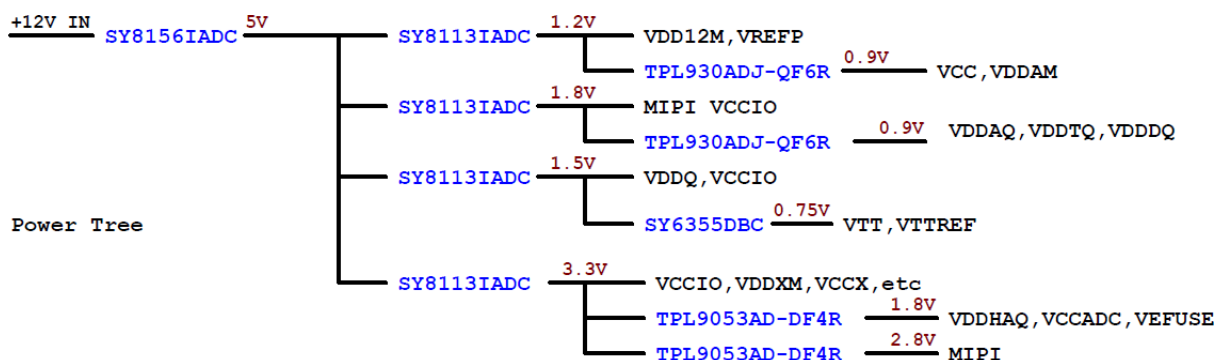
The development board can be powered either via a 12 V DC adapter or through the PCIe slot, and both power sources can supply the board simultaneously.

The input 12V power is regulated by the PMIC on the development board to generate 5V, 3.3V, 2.8V, 1.8V, 1.5V, 1.2V, 0.9V, and 0.75V power supplies, thus meeting the power supply requirements of the development board.

To facilitate accurate evaluation of the board's power consumption, an INA3221 current monitoring circuit is provided on-board, enabling current measurement for the FPGA's key power rails.

3.2.2 Power Distribution

Figure 3-1 Power Distribution Diagram



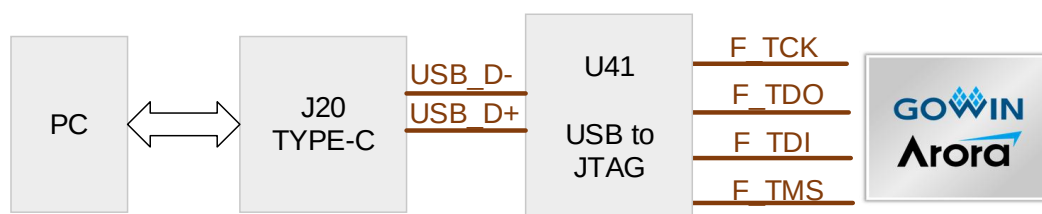
3.3 Download Modules

3.3.1 Introduction

The development board includes a TYPE-C download port (J20) designed to program the programs to external SPI FLASH or SRAM.

The download connection diagram is show in Figure 3-2.

Figure 3-2 Connection Diagram of Download



3.3.2 Pin Distribution

Table 3-1 JTAG Pin Distribution

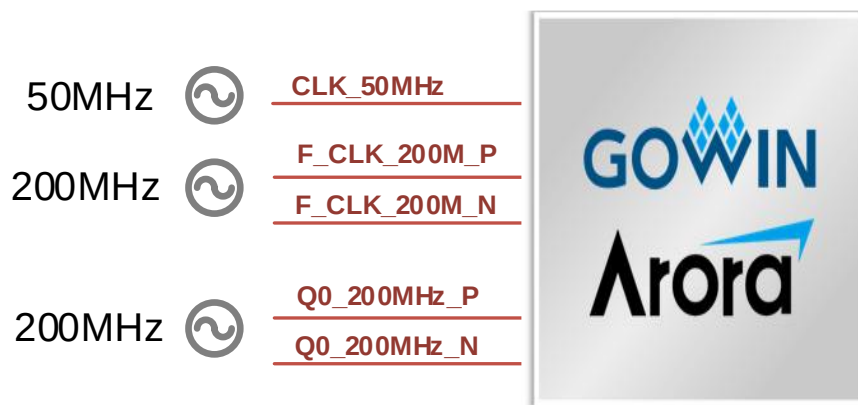
Signal	FPGA Pin No.	BANK	I/O Level	Description
F_TCK	C17	12	3.3V	JTAG signal
F_TDO	C18	12	3.3V	
F_TDI	B18	12	3.3V	
F_TMS	D17	12	3.3V	

3.4 Clock

3.4.1 Introduction

The development board provides multiple FPGA clock sources, including one 50 MHz single-ended clock and two 200 MHz differential clocks, with one 200 MHz clock connected to the FPGA SerDes high-speed clock pins and the other to the FPGA GCLK pins. The clock pin distribution is shown in Figure 3-3.

Figure 3-3 Clock Connection Diagram



3.4.2 Pin Distribution

Table 3-2 Clock Pin Distribution

Signal	FPGA Pin No.	BANK	I/O Level	Description
CLK_50MHz	L16	4	3.3V	50 MHz single-ended clock
F_CLK_200M_P	P18	5	3.3V	200 MHz differential clock
F_CLK_200M_N	P17	5	3.3V	200 MHz differential clock
Q0_200MHz_P	E8	Q0	-	200 MHz differential clock
Q0_200MHz_N	D8	Q0	-	200 MHz differential clock

3.5 DDR3

3.5.1 Introduction

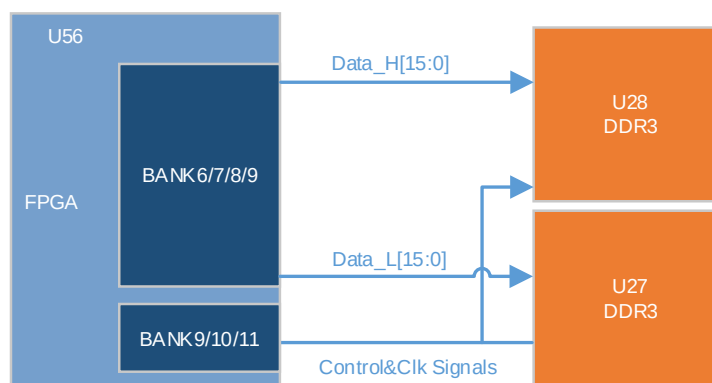
The development board includes two 2 Gbit DDR3 chips. The signals of DDR3 chip are connected to the BANK6, BANK7, BANK8, BANK9, BANK10, and BANK11 of FPGA. The specific configurations of DDR3 are as shown in Table 3-3.

Table 3-3 DDR3 Configuration

Designator	Capacity
U28	128M x 16bit
U27	128M x 16bit

The hardware connection diagram of DDR3 is as show in Figure 3-4.

Figure 3-4 Hardware Connection Diagram of DDR3



3.5.2 Pin Distribution

Table 3-4 DDR3 Pin Distribution

Signal	FPGA Pin No.	BANK	I/O Level	Description
DDR3_A0	L7	10	1.5V	Address
DDR3_A1	J6	11	1.5V	Address
DDR3_A2	K4	10	1.5V	Address
DDR3_A3	L6	10	1.5V	Address
DDR3_A4	H7	11	1.5V	Address
DDR3_A5	J7	10	1.5V	Address

Signal	FPGA Pin No.	BANK	I/O Level	Description
DDR3_A6	G3	11	1.5V	Address
DDR3_A7	H5	11	1.5V	Address
DDR3_A8	E3	11	1.5V	Address
DDR3_A9	F4	11	1.5V	Address
DDR3_A10	N4	10	1.5V	Address
DDR3_A11	G6	11	1.5V	Address
DDR3_A12	L3	10	1.5V	Address
DDR3_A13	H4	11	1.5V	Address
DDR3_BA0	M3	10	1.5V	Bank address
DDR3_BA1	K5	10	1.5V	Bank address
DDR3_BA2	L5	10	1.5V	Bank address
DDR3_CS#	P4	10	1.8V	Chip select
DDR3_CAS#	R5	9	1.5V	Column address strobe
DDR3_CKE	R3	10	1.8V	Clock enable
DDR3_ODT	T4	9	1.8V	On-die termination enable
DDR3_RAS#	U3	9	1.5V	Row address strobe
DDR3_RESET	F5	11	1.8V	Reset
DDR3_WE#	M5	10	1.5V	Write enable
DDR3_CLK_P	V2	9	1.5V	Differential clock
DDR3_CLK_N	V3	9	1.5V	Differential clock
DDR3_DQ0	U5	9	1.5V	Data
DDR3_DQ1	U8	9	1.5V	Data

Signal	FPGA Pin No.	BANK	I/O Level	Description
DDR3_DQ2	T5	9	1.5V	Data
DDR3_DQ3	R7	9	1.5V	Data
DDR3_DQ4	T6	9	1.5V	Data
DDR3_DQ5	T7	9	1.5V	Data
DDR3_DQ6	V5	9	1.5V	Data
DDR3_DQ7	U7	9	1.5V	Data
DDR3_DQ8	P8	9	1.5V	Data
DDR3_DQ9	P7	9	1.5V	Data
DDR3_DQ10	M8	9	1.5V	Data
DDR3_DQ11	N6	9	1.5V	Data
DDR3_DQ12	R8	9	1.5V	Data
DDR3_DQ13	N5	9	1.5V	Data
DDR3_DQ14	N9	9	1.5V	Data
DDR3_DQ15	P6	9	1.5V	Data
DDR3_DQ0_1	U10	8	1.5V	Data
DDR3_DQ1_1	T12	8	1.5V	Data
DDR3_DQ2_1	V9	8	1.5V	Data
DDR3_DQ3_1	T13	8	1.5V	Data
DDR3_DQ4_1	U11	8	1.5V	Data
DDR3_DQ5_1	T11	8	1.5V	Data
DDR3_DQ6_1	V10	8	1.5V	Data
DDR3_DQ7_1	V13	8	1.5V	Data
DDR3_DQ8_1	U17	6	1.5V	Data
DDR3_DQ9_1	U16	7	1.5V	Data
DDR3_DQ10_1	U18	6	1.5V	Data
DDR3_DQ11_1	P13	7	1.5V	Data
DDR3_DQ12_1	V16	7	1.5V	Data
DDR3_DQ13_1	R13	7	1.5V	Data
DDR3_DQ14_1	V17	7	1.5V	Data
DDR3_DQ15_1	U15	7	1.5V	Data

Signal	FPGA Pin No.	BANK	I/O Level	Description
DDR3_LDM0	V8	9	1.5V	Data input mask
DDR3_UDM0	N8	9	1.5V	Data input mask
DDR3_LDQS0_P	V6	9	1.5V	Data clock
DDR3_LDQS0_N	V7	9	1.5V	Data clock
DDR3_UDQS0_P	T8	9	1.5V	Data clock
DDR3_UDQS0_N	T9	9	1.5V	Data clock
DDR3_LDM1	U13	8	1.5V	Data input mask
DDR3_UDM1	T14	7	1.5V	Data input mask
DDR3_LDQS1_P	V11	8	1.5V	Data clock
DDR3_LDQS1_N	V12	8	1.5V	Data clock
DDR3_UDQS1_P	V15	7	1.5V	Data clock
DDR3_UDQS1_N	V14	7	1.5V	Data clock

3.6 PCIe Interface

3.6.1 Introduction

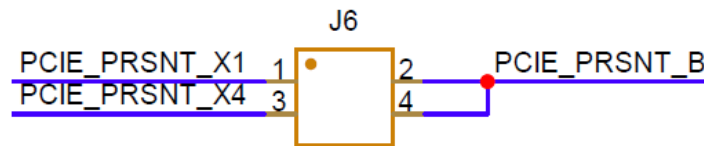
The development board provides one PCIe x4 interface. The transceiver signals of the PCIe interface are directly connected to the SerDes high-speed signals of the FPGA, and the TX and RX signals of the four lanes are connected to the FPGA as differential signals. The design diagram is shown in Figure 3-5.

Figure 3-5 Connection Diagram of PCIe Interface



Additionally, a header J6 (dual-row 4-pin, 2.54 mm pitch) is reserved to bring out the signals PCIE_PRSENT_X1, PCIE_PRSENT_X4, and PCIE_PRSENT_B. Depending on PCIe testing requirements, PCIE_PRSENT_X1 or PCIE_PRSENT_X4 can be tied to PCIE_PRSENT_B. The connection diagram is shown in Figure 3-6.

Figure 3-6 PCIe_PRSENT Connection Diagram



3.6.2 Pin Distribution

Table 3-5 Pin Distribution of PCIe Interface

Signal	FPGA Pin No.	BANK	I/O Level	Description
PCIE_WAKE_B	F6	1	3.3V	PCIe device wake-up
PCIE_PERST	F7	1	3.3V	PCIe device reset
PCIE_CLK_QO_P	E7	Q0	-	PCIe reference clock
PCIE_CLK_QO_N	E6	Q0	-	PCIe reference clock
PCIE_RX0_P	B2	Q0	-	PCIe receive data
PCIE_RX0_N	A2	Q0	-	PCIe receive data
PCIE_RX1_P	A4	Q0	-	PCIe receive data
PCIE_RX1_N	A5	Q0	-	PCIe receive data
PCIE_RX2_P	A7	Q0	-	PCIe receive data
PCIE_RX2_N	A8	Q0	-	PCIe receive data
PCIE_RX3_P	A10	Q0	-	PCIe receive data
PCIE_RX3_N	A11	Q0	-	PCIe receive data
PCIE_TX0_P	D4	Q0	-	PCIe transmit data
PCIE_TX0_N	C4	Q0	-	PCIe transmit data
PCIE_TX1_P	C6	Q0	-	PCIe transmit data
PCIE_TX1_N	B6	Q0	-	PCIe transmit data
PCIE_TX2_P	C9	Q0	-	PCIe transmit data

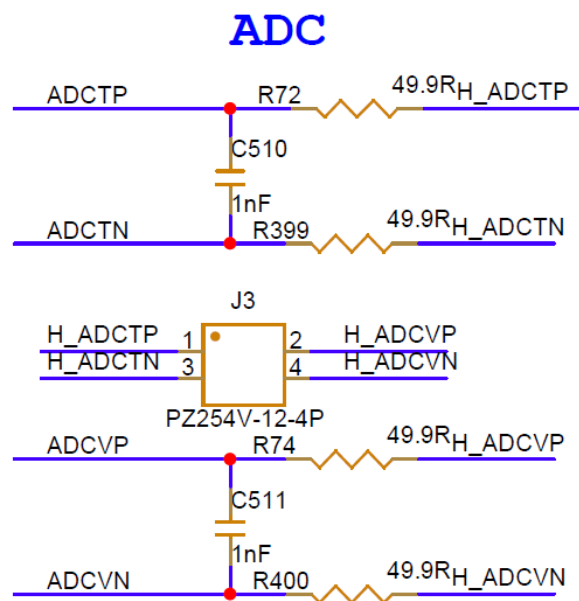
Signal	FPGA Pin No.	BANK	I/O Level	Description
PCIE_TX2_N	B9	Q0	-	PCIe transmit data
PCIE_TX3_P	D11	Q0	-	PCIe transmit data
PCIE_TX3_N	C11	Q0	-	PCIe transmit data

3.7 ADC Interface

3.7.1 Introduction

The development board includes input interfaces for ADC signals. The connector uses a 2x2P pin header with 2.54 mm pitch. Figure 3-7 shows the ADC interface schematic connection diagram and the anti-aliasing filter circuit.

Figure 3-7 Connection Diagram of ADC Interface Schematic



3.7.2 Pin Distribution

Table 3-6 Pin Distribution of ADC Interface

J3 Pin No.	Signal	FPGA Pin No.	BANK	I/O Level	Description
1	ADCTP	F15	ADC	-	Analog signal input
2	ADCTN	F16	ADC	-	Analog signal input
3	ADCVP	G14	ADC	-	Analog signal

J3 Pin No.	Signal	FPGA Pin No.	BANK	I/O Level	Description
					input
4	ADCVN	F14	ADC	-	Analog signal input

3.8 MIPI C-PHY Interface (Hard Core)

3.8.1 Introduction

This interface includes one MIPI C-PHY hard core interface, consisting of 3 data lanes. The interface is routed out via an FPC connector (20-pin, 0.5 mm pitch). The connection diagram is shown in Figure 3-8.

Figure 3-8 Connection Diagram of MIPI C-PHY (Hard Core) Interface



3.8.2 Pin Distribution

Table 3-7 Pin Distribution of MIPI C-PHY (Hard Core) Interface

J1 Pin No.	Signal	FPGA Pin No.	BANK	I/O Level	Description
1	GND	-	-	-	GND
2	CPHY_C2	U1	M1	-	MIPI C-PHY data signal
3	CPHY_B2	T1	M1	-	MIPI C-PHY data signal
4	CPHY_A2	T2	M1	-	MIPI C-PHY data signal
5	GND	-	-	-	GND
6	CPHY_C1	P1	M1	-	MIPI C-PHY data signal
7	CPHY_B1	P2	M1	-	MIPI C-PHY

J1 Pin No.	Signal	FPGA Pin No.	BANK	I/O Level	Description
					data signal
8	CPHY_A1	N2	M1	-	MIPI C-PHY data signal
9	GND	-	-	-	GND
10	CPHY_C0	M1	M1	-	MIPI C-PHY data signal
11	CPHY_B0	L1	M1	-	MIPI C-PHY data signal
12	CPHY_A0	K2	M1	-	MIPI C-PHY data signal
13	GND	-	-	-	GND
14	MIPI_RESET	N14	5	1.8V	MIPI C-PHY reset signal
15	CPHY-SCL	G8	1	1.8V	MIPI C-PHY I2C SCL
16	CPHY-SDA	G9	1	1.8V	MIPI C-PHY I2C SDA
17	GND	-	-	-	GND
18	GND	-	-	-	GND
19	VCC3P3	-	-	3.3V	Power
20	VCC3P3	-	-	3.3V	Power
21	GND	-	-	-	GND
22	GND	-	-	-	GND

3.9 MIPI D-PHY Interface (Hard Core)

3.9.1 Introduction

This interface includes one MIPI D-PHY hard core interface, consisting of 4 data lanes and 1 clock lane. The interface signals are routed out via an OK-10F030-04 connector. The connection diagram of MIPI interface is shown in Figure 3-9.

Figure 3-9 Connection Diagram of MIPI D-PHY (Hard Core) Interface



3.9.2 Pin Distribution

Table 3-8 Pin Distribution of MIPI D-PHY (Hard Core) Interface

J10 Pin No.	Signal	FPGA Pin No.	BANK	I/O Level	Description
1	AVDD	-	-	2.8V	Power
2	AVDD	-	-	2.8V	Power
3	DGND	-	-	-	GND
4	DPHY_CK P	F1	M0	-	MIPI clock signal
5	DPHY_CK N	F2	M0	-	MIPI clock signal
6	DGND	-	-	-	GND
7	DPHY_D0 P	J1	M0	-	MIPI data signal
8	DPHY_D0 N	H2	M0	-	MIPI data signal
9	DGND	-	-	-	GND
10	DPHY_D2 P	E1	M0	-	MIPI data signal
11	DPHY_D2 N	D1	M0	-	MIPI data signal
12	DOVDD	-	-	1.8V	Power
13	DVDD	-	-	1.2V	Power
14	DVDD	-	-	1.2V	Power
15	DVDD	-	-	1.2V	Power

J10 Pin No.	Signal	FPGA Pin No.	BANK	I/O Level	Description
16	DGND	-	-	-	GND
17	AFVDD	-	-	2.8V	Power
18	AFGND	-	-	-	GND
19	DPHY_D1 P	H1	M0	-	MIPI data signal
20	DPHY_D1 N	G1	M0	-	MIPI data signal
21	DGND	-	-	-	GND
22	DPHY_D3 P	C1	M0	-	MIPI data signal
23	DPHY_D3 N	D2	M0	-	MIPI data signal
24	DGND	-	-	-	GND
25	DPHY_VS YNC	G13	2	1.8V	MIPI D-PHY VSYNC signal
26	MIPI_RES ET	N14	5	1.8V	MIPI D-PHY reset signal
27	DPHY_SC L	F9	1	1.8V	MIPI D-PHY I2C SCL
28	DPHY_SD A	F8	1	1.8V	MIPI D-PHY I2C SDA
29	DPHY_MC LK	F13	2	1.8V	MIPI D-PHY MCLK signal
30	AGND	-	-	-	GND

3.10 MIPI D-PHY Interface (Soft Core)

3.10.1 Introduction

This interface includes one MIPI D-PHY soft core interface, consisting of 4 data lanes and 1 clock lane. The interface signals are routed out via a 2×10-pin header with 2.0 mm pitch. The connection diagram of MIPI D-PHY soft core interface is shown in Figure 3-10.

Figure 3-10 Connection Diagram of MIPI D-PHY (Soft Core) Interface



3.10.2 Pin Distribution

Table 3-9 Pin Distribution of MIPI D-PHY (Soft Core) Interface

J28 Pin No.	Signal	FPGA Pin No.	BANK	I/O Level	Description
1	F_MIPI_D0_P	C15	2	1.8V	MIPI data signal
2	F_MIPI_D0_N	D15	2	1.8V	MIPI data signal
3	GND	-	-	-	GND
4	GND	-	-	-	GND
5	F_MIPI_D1_P	A15	2	1.8V	MIPI data signal
6	F_MIPI_D1_N	A16	2	1.8V	MIPI data signal
7	GND	-	-	-	GND
8	GND	-	-	-	GND
9	F_MIPI_CK0_P	C14	2	1.8V	MIPI clock signal
10	F_MIPI_CK0_N	D14	2	1.8V	MIPI clock signal
11	GND	-	-	-	GND
12	GND	-	-	-	GND
13	F_MIPI_D2_P	B16	2	1.8V	MIPI data signal
14	F_MIPI_D2_N	A17	2	1.8V	MIPI data signal

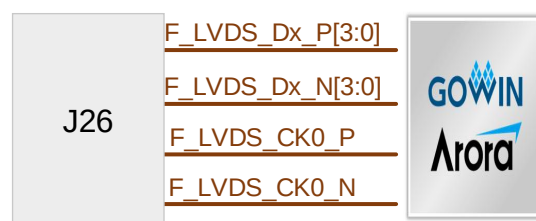
J28 Pin No.	Signal	FPGA Pin No.	BANK	I/O Level	Description
15	GND	-	-	-	GND
16	GND	-	-	-	GND
17	F_MIPI_D3_P	D16	2	1.8V	MIPI data signal
18	F_MIPI_D3_N	E16	2	1.8V	MIPI data signal
19	GND	-	-	-	GND
20	GND	-	-	-	GND

3.11 LVDS Interface

3.11.1 Introduction

The development board provides one LVDS interface, consisting of 5 differential pairs (4 data lanes and 1 clock lane). The interface signals are routed out via a 2×10-pin header with 2.0 mm pitch. The connection diagram is shown in Figure 3-11.

Figure 3-11 Connection Diagram of LVDS Interface



3.11.2 Pin Distribution

Table 3-10 Pin Distribution of LVDS Interface

J26 Pin No.	Signal	FPGA Pin No.	BANK	I/O Level	Description
1	F_LVDS_D0_P	F11	1	3.3V	LVDS data
2	F_LVDS_D0_N	F12	1	3.3V	LVDS data
3	GND	-	-	-	GND
4	GND	-	-	-	GND
5	F_LVDS_	F10	1	3.3V	LVDS data

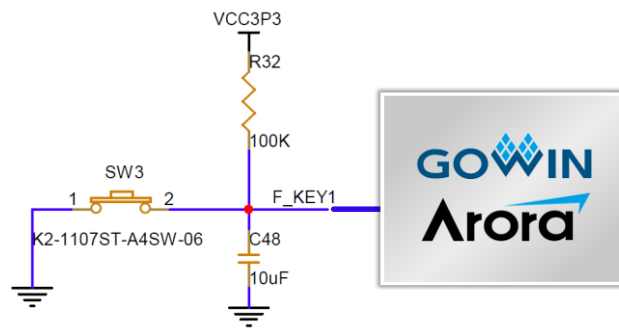
J26 Pin No.	Signal	FPGA Pin No.	BANK	I/O Level	Description
	D1_P				
6	F_LVDS_ D1_N	G11	1	3.3V	LVDS data
7	GND	-	-	-	GND
8	GND	-	-	-	GND
9	F_LVDS_ CK0_P	E12	1	3.3V	LVDS Clock
10	F_LVDS_ CK0_N	E13	1	3.3V	LVDS Clock
11	GND	-	-	-	GND
12	GND	-	-	-	GND
13	F_LVDS_ D2_P	C13	1	3.3V	LVDS data
14	F_LVDS_ D2_N	B14	1	3.3V	LVDS data
15	GND	-	-	-	GND
16	GND	-	-	-	GND
17	F_LVDS_ D3_P	A13	1	3.3V	LVDS data
18	F_LVDS_ D3_N	A14	1	3.3V	LVDS data
19	GND	-	-	-	GND
20	GND	-	-	-	GND

3.12 Key & Indicator

3.12.1 Introduction

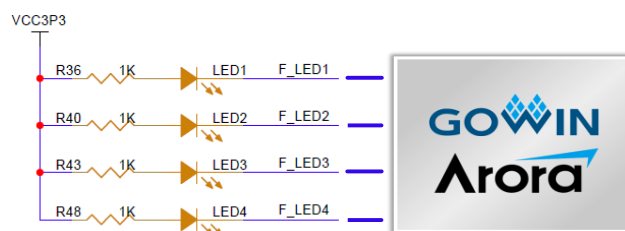
DK_PCIE_GW5AT-LV60UG324_V1.1 development board is equipped with four keys. The corresponding IO input voltage of the FPGA is low when the key is pressed while high when the key is not pressed. The connection diagram is shown in Figure 3-12.

Figure 3-12 Connection Diagram of Key



The development board includes four user LEDs, which can be switched on and off via the program. When the IO voltage is low, it will be on; When the IO voltage is high, it will be off. The connection diagram is shown in Figure 3-13.

Figure 3-13 Connection Diagram of LED



3.12.2 Pin Distribution

Table 3-11 Pin Distribution of Key

Signal	FPGA Pin No.	BANK	I/O Level	Description
F_KEY1	K18	4	3.3V	Key
F_KEY2	H18	3	3.3V	Key
F_KEY3	H14	3	3.3V	Key
F_KEY4	G16	3	3.3V	Key

Table 3-12 Pin Distribution of Indicators

Signal	FPGA Pin No.	BANK	I/O Level	Description
F_LED1	H13	4	3.3V	LED indicator

Signal	FPGA Pin No.	BANK	I/O Level	Description
F_LED2	H12	4	3.3V	LED indicator
F_LED3	M13	5	3.3V	LED indicator
F_LED4	H17	3	3.3V	LED indicator

3.13 GPIO

3.13.1 Introduction

The development board provides 16 GPIOs with 3.3 V I/O standard, which are routed out via a 2×10-pin header with 2.54 mm pitch, facilitating user testing. Each GPIO is equipped with an ESD protection device.

Figure 3-14 Connection Diagram of GPIO Interface



3.13.2 Pin Distribution

Table 3-13 Pin Distribution of GPIO Interface

J8 Pin No.	Signal	FPGA Pin No.	BANK	I/O Level	Description
1	F_GPIO1	R15	5	3.3V	GPIO
2	F_GPIO2	R16	5	3.3V	GPIO
3	F_GPIO3	P15	5	3.3V	GPIO
4	F_GPIO4	P16	5	3.3V	GPIO
5	F_GPIO5	N15	5	3.3V	GPIO
6	F_GPIO6	N16	5	3.3V	GPIO
7	F_GPIO7	M14	5	3.3V	GPIO
8	F_GPIO8	N17	5	3.3V	GPIO
9	F_GPIO9	L14	5	3.3V	GPIO
10	F_GPIO10	N18	5	3.3V	GPIO
11	F_GPIO11	L15	4	3.3V	GPIO
12	F_GPIO12	L17	4	3.3V	GPIO
13	F_GPIO13	K15	4	3.3V	GPIO

J8 Pin No.	Signal	FPGA Pin No.	BANK	I/O Level	Description
14	F_GPIO14	L18	4	3.3V	GPIO
15	F_GPIO15	K16	4	3.3V	GPIO
16	F_GPIO16	K17	4	3.3V	GPIO
17	GND	-	-	-	GND
18	VCC3P3	-	-	3.3V	Power
19	GND	-	-	-	GND
20	VCC3P3	-	-	3.3V	Power

4 Precaution

When using the development board, handle it with care and observe proper ESD protection.

