



# DK\_PCIE\_GW5ART-LV15MG132P\_V1.1

## **User Guide**

DBUG1294-1.0E, 05/22/2026

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**Revision History**

| Date       | Version | Description                |
|------------|---------|----------------------------|
| 05/22/2026 | 1.0E    | Initial version published. |

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# 1 About This Guide

## 1.1 Purpose

The DK\_PCIE\_GW5ART-LV15MG132P\_V1.1 development board (hereinafter referred to as "the development board") user guide consists of following three parts:

- A brief introduction to the features of the development board.
- An introduction to the development board system architecture and hardware resources.
- An introduction to the hardware circuits, functions and pin assignment.

## 1.2 Related Documents

You can find the related documents at GOWINSEMI website:

- [DS1118, GW5ART series of FPGA Products Data Sheet](#)
- [UG1120, GW5ART-15 Pinout](#)
- [UG1233, GW5ART series of FPGA Products Package and Pinout User Guide](#)
- [UG720, Arora V 15K FPGA Products Programming and Configuration User Guide](#)

## 1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

| Terminology and Abbreviations | Meaning                       |
|-------------------------------|-------------------------------|
| FPGA                          | Field Programmable Gate Array |
| GPIO                          | Gowin Programmable I/O        |

| Terminology and Abbreviations | Meaning                 |
|-------------------------------|-------------------------|
| JTAG                          | Joint Test Action Group |
| LDO                           | Low Dropout Regulator   |

## 1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

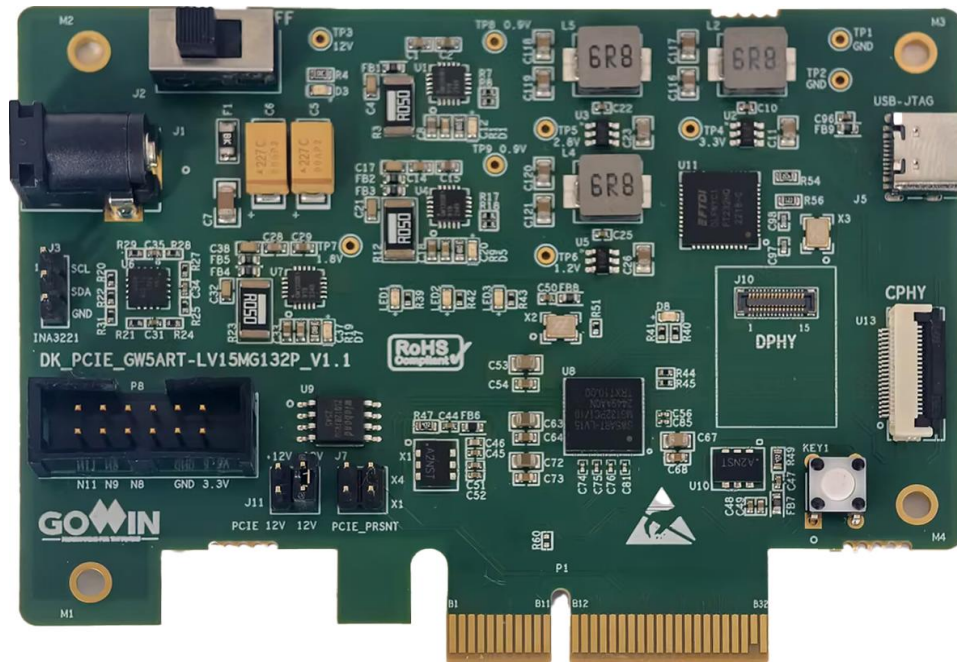
Website: [www.gowinsemi.com](http://www.gowinsemi.com)

E-mail: [support@gowinsemi.com](mailto:support@gowinsemi.com)

# 2 Development Board Introduction

## 2.1 Overview

Figure 2-1 DK\_PCIE\_GW5ART-LV15MG132P\_V1.1 Development Board



Gowin GW5ART series of FPGA products are the 5 series products of Arora family. It is a System-in-Package (SiP) device featuring abundant on-chip resources, including an integrated PCIe 3.0 hard IP core, support for custom high-speed SerDes protocols ranging from 270 Mbps to 12.5 Gbps, integrated PSRAM memory, and a new high-performance DSP architecture with AI computing capability. The device also integrates high-speed LVDS interfaces, abundant BSRAM memory resources, MIPI D-PHY hard IP, and MIPI C-PHY hard IP, and is available in multiple package options. Combined with the 22 nm SRAM process technology, these integrated resources enable the GW5ART series FPGA to meet the

requirements of low-power, high-performance, and high-compatibility application designs.

The development board supports PCIe 3.0 communication, MIPI D-PHY communication, MIPI C-PHY communication, and LVDS interface communication, meeting various application requirements such as FPGA functional evaluation, hardware reliability verification, software development, and debugging.

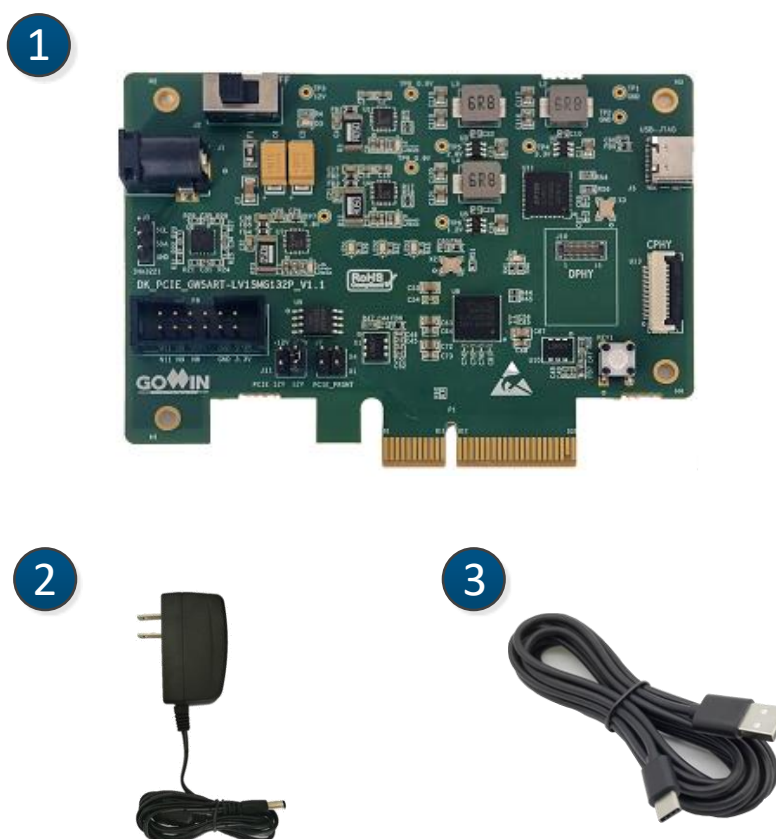
The development board uses Gowin GW5ART-LV15MG132P FPGA device. For the internal resources of the chip, see [DS1118, GW5ART series of FPGA Products Data Sheet](#).

## 2.2 A Development Board Kit

The development board kit includes the following items:

1. DK\_PCIE\_GW5ART-LV15MG132P\_V1.1 development board
2. 12V power adapter (Input: AC 100-240V~50/60 Hz 0.6A, output: DC12V 2A)
3. Type-A to Type-C interface data cable

Figure 2-2 A Development Board Kit



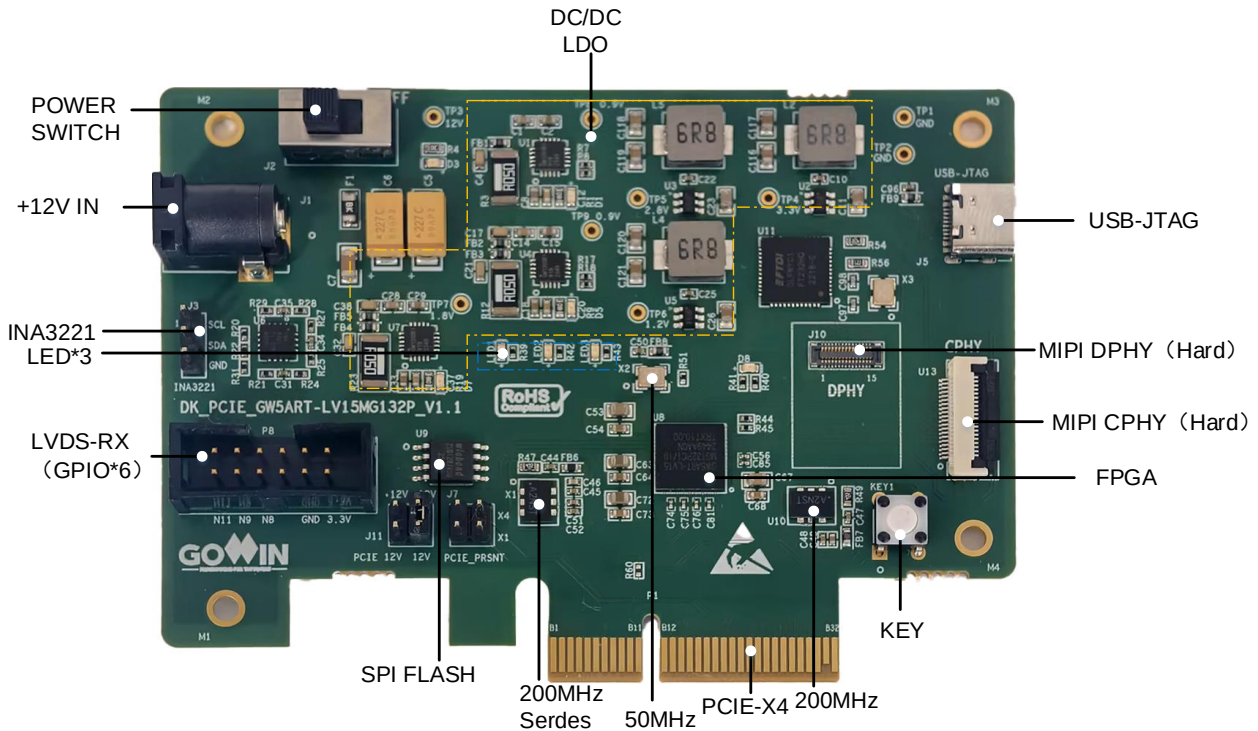
① DK\_PCIE\_GW5ART-LV15MG132P\_V1.1

development board

- ② 12V power supply adapter
- ③ Type-A to Type-C interface data cable

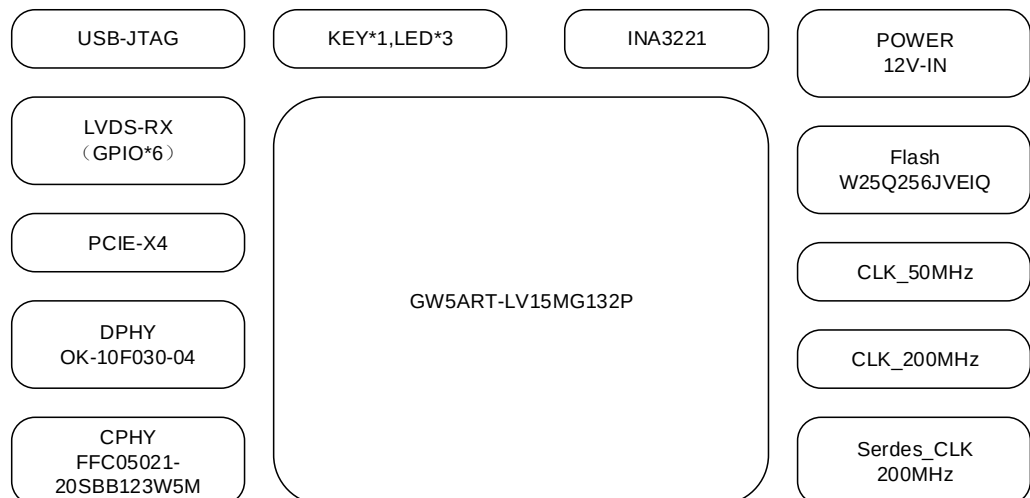
## 2.3 PCB Components

Figure 2-3 PCB Components



## 2.4 System Block Diagram

Figure 2-4 System Block Diagram



## 2.5 Features

The key features are as follows:

- **FPGA Device**
  - Gowin GW5ART-LV15MG132P FPGA
- **Download and Boot**
  - Integrates USB download circuit on the development board, download through Type- C interface.
  - External SPI Flash boot
- **Power Supply**
  - External DC 12V 2A power
  - The POWER LED lights up after power-on
  - The development board generates 3.3V, 2.8V, 1.8V, 1.2V, 0.9V power.
- **Clock system**
  - 50 MHz single-ended clock
  - 200 MHz differential clock
- **Memory device**
  - 128 Mbit NOR Flash
- **MIPI-DPHY interface**
  - One MIPI D-PHY interface connected to the MIPI D-PHY hard core, supporting communication rates up to 2.5 Gbps.
- **MIPI-CPHY interface**
  - One MIPI C-PHY interface connected to the MIPI C-PHY hard core, supporting communication rates up to 2.0 Gbps.
- **LVDS-RX interface**
  - LVDS interface with 3 lanes, and can also be used as GPIOs.
- **Keys & LEDs**
  - 1 reset key
  - 3 LED indicators

# 3 Development Board Circuit

## 3.1 FPGA

### Overview

For the resources of GW5ART FPGA products, please refer to [DS1118, GW5ART series of FPGA Products](#).

### I/O BANK

For the I/O BANK, package, and pinout information, see [UG1233, GW5ART series of FPGA Products Package and Pinout User Guide](#) for more details.

## 3.2 Power Supply

### 3.2.1 Introduction

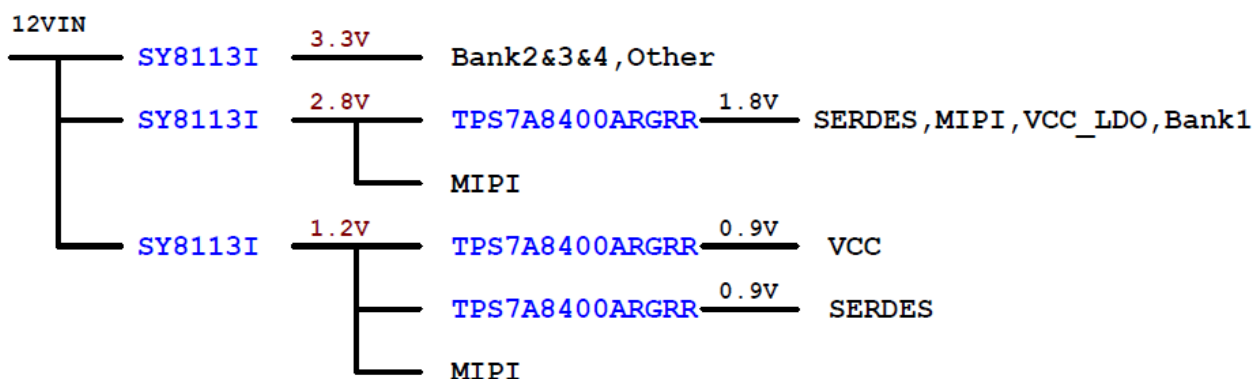
The development board can be powered either through the power connector (J1) or the PCIe interface (P1), but both cannot be used simultaneously. When using the PCIe interface to supply 12 V power, pins 1 and 3 or pins 2 and 4 of J11 must be shorted.

Power adapter input: AC 100-240V~50/60 Hz 0.6A; output: DC12V 2A.

The input 12V power supply is regulated by the PMIC on the development board to generate 3.3V, 2.8V, 1.8V, 1.2V and 0.9V power supplies, thus meeting the power supply requirements of the development board.

## 3.2.2 Power Assignment

Figure 3-1 Power Assignment Diagram



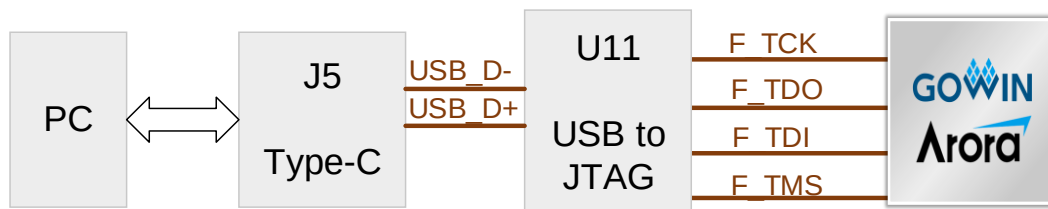
## 3.3 Download Module

### 3.3.1 Introduction

The development board includes a TYPE-C download port (J5) designed to program the programs to external SPI FLASH or SRAM.

The connection diagram is shown in Figure 3-2.

Figure 3-2 Connection Diagram of Download



### 3.3.2 Pin Assignment

Table 3-1 JTAG Pin Assignment

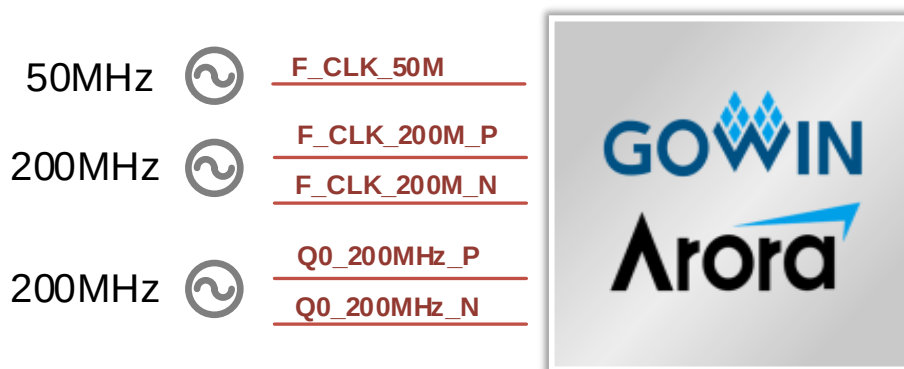
| Signal Name | FPGA Pin No. | BANK | I/O Level | Description |
|-------------|--------------|------|-----------|-------------|
| F_TCK       | G2           | 4    | 3.3V      | JTAG signal |
| F_TDO       | J2           | 4    | 3.3V      |             |
| F_TDI       | J3           | 4    | 3.3V      |             |
| F_TMS       | G3           | 4    | 3.3V      |             |

## 3.4 Clock

### 3.4.1 Introduction

The development board provides multiple FPGA clock sources, including one 50 MHz single-ended clock and two 200 MHz differential clocks, with one 200 MHz clock connected to the FPGA SerDes high-speed clock pins. The clock pin assignment is shown in Figure 3-3.

Figure 3-3 Clock Connection Diagram



### 3.4.2 Pin Assignment

Table3-2 Clock Pin Assignment

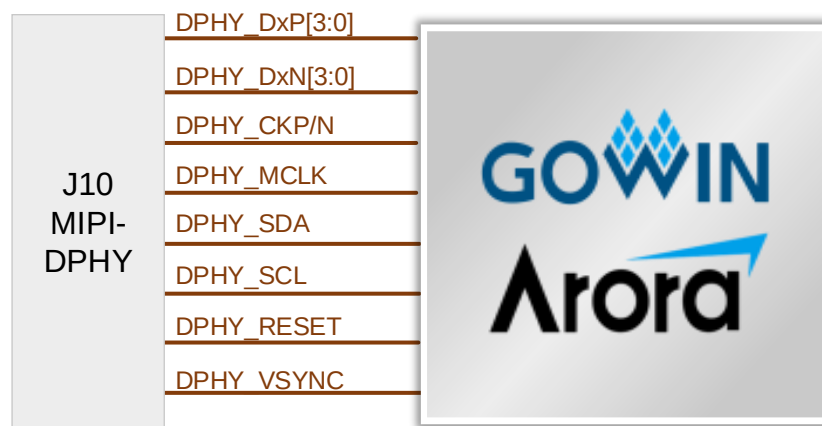
| Signal Name  | FPGA Pin No. | BANK | I/O Level | Description                |
|--------------|--------------|------|-----------|----------------------------|
| F_CLK_50M    | M2           | 3    | 3.3V      | 50 MHz single-ended clock  |
| F_CLK_200M_P | K3           | 4    | 3.3V      | 200 MHz differential clock |
| F_CLK_200M_N | K2           | 4    | 3.3V      | 200 MHz differential clock |
| Q0_200MHz_P  | C10          | Q0   | -         | 200 MHz differential clock |
| Q0_200MHz_N  | B10          | Q0   | -         | 200 MHz differential clock |

## 3.5 MIPI-DPHY interface

### 3.5.1 Introduction

This interface provides a single-channel MIPI D-PHY (hard core) connection, supporting 4 data lanes + 1 clock lane. The interface uses a 30-pin OK-10F030-04 connector with 0.4 mm pitch, enabling communication with peripherals equipped with an OK-10GM30-04 connector. The connection diagram of MIPI-DPHY interface is shown in Figure 3-4 .

Figure 3-4 Connection Diagram of MIPI-DPHY Interface



### 3.5.2 Pin Assignment

Table 3-3 Pin Distribution of MIPI-DPHY Interface

| J10 Pin No. | Signal Name | FPGA Pin No. | BANK | I/O Level | Description         |
|-------------|-------------|--------------|------|-----------|---------------------|
| 1           | 2.8V        | -            | -    | -         | 2.8V power          |
| 2           | 2.8V        | -            | -    | -         | 2.8V power          |
| 3           | GND         | -            | -    | -         | GND                 |
| 4           | DPHY_CKP    | N5           | M0   | -         | DPHY (clock signal) |
| 5           | DPHY_CKN    | P5           | M0   | -         | DPHY (clock signal) |
| 6           | GND         | -            | -    | -         | GND                 |
| 7           | DPHY_D0P    | N7           | M0   | -         | DPHY data signal    |
| 8           | DPHY_D0N    | P7           | M0   | -         | DPHY data signal    |
| 9           | GND         | -            | -    | -         | GND                 |
| 10          | DPHY_D2P    | N4           | M0   | -         | DPHY data signal    |

| J10 Pin No. | Signal Name    | FPGA Pin No. | BANK | I/O Level | Description                        |
|-------------|----------------|--------------|------|-----------|------------------------------------|
| 11          | DPHY_D2N       | P4           | M0   | -         | DPHY data signal                   |
| 12          | 1.8V           | -            | -    | -         | 1.8V power                         |
| 13          | 1.2V           | -            | -    | -         | 1.2V power                         |
| 14          | 1.2V           | -            | -    | -         | 1.2V power                         |
| 15          | 1.2V           | -            | -    | -         | 1.2V power                         |
| 16          | GND            | -            | -    | -         | GND                                |
| 17          | 2.8V           | -            | -    | -         | 2.8V power                         |
| 18          | GND            | -            | -    | -         | GND                                |
| 19          | DPHY_D1N       | N6           | M0   | -         | DPHY data signal                   |
| 20          | DPHY_D1P       | P6           | M0   | -         | DPHY data signal                   |
| 21          | GND            | -            | -    | -         | GND                                |
| 22          | DPHY_D3N       | P3           | M0   | -         | DPHY data signal                   |
| 23          | DPHY_D3P       | N3           | M0   | -         | DPHY data signal                   |
| 24          | GND            | -            | -    | -         | GND                                |
| 25          | DPHY_VSYN<br>C | N14          | 1    | 1.8V      | Vertical synchronization<br>signal |
| 26          | DPHY_RESE<br>T | P14          | 1    | 1.8V      | Reset signal                       |
| 27          | DPHY_SCL       | P13          | 1    | 1.8V      | IIC signal                         |
| 28          | DPHY_SDA       | N13          | 1    | 1.8V      | IIC signal                         |
| 29          | DPHY_MCLK      | N12          | 1    | 1.8V      | Clock signal                       |
| 30          | GND            | -            | -    | -         | GND                                |

## 3.6 MIPI-CPHY interface

### 3.6.1 Introduction

This interface provides a single-channel MIPI C-PHY (hard core) connection. The interface uses a 20-pin FFC05021-20SBB123W5M connector with 0.5 mm pitch, enabling communication with external peripherals through an FPC flexible cable. The connection diagram of MIPI-CPHY interface is shown in Figure 3-5.

Figure 3-5 Connection Diagram of MIPI-CPHY Interface



### 3.6.2 Pin Assignment

Table 3-4 Pin Distribution of MIPI-CPHY Interface

| U13 Pin No. | Signal Name | FPGA Pin No. | BANK | I/O Level | Description  |
|-------------|-------------|--------------|------|-----------|--------------|
| 1           | GND         | -            | -    | -         | GND          |
| 2           | CPHY_C2     | D1           | M1   | -         | CPHY signal  |
| 3           | CPHY_B2     | D2           | M1   | -         | CPHY signal  |
| 4           | CPHY_A2     | C1           | M1   | -         | CPHY signal  |
| 5           | GND         | -            | -    | -         | GND          |
| 6           | CPHY_C1     | J1           | M1   | -         | CPHY signal  |
| 7           | CPHY_B1     | K1           | M1   | -         | CPHY signal  |
| 8           | CPHY_A1     | L1           | M1   | -         | CPHY signal  |
| 9           | GND         | -            | -    | -         | GND          |
| 10          | CPHY_C0     | G1           | M1   | -         | CPHY signal  |
| 11          | CPHY_B0     | F1           | M1   | -         | CPHY signal  |
| 12          | CPHY_A0     | F2           | M1   | -         | CPHY signal  |
| 13          | GND         | -            | -    | -         | GND          |
| 14          | CPHY_RESETN | N10          | 1    | 1.8V      | Reset signal |
| 15          | CPHY_SDA    | P10          | 1    | 1.8V      | IIC signal   |
| 16          | CPHY_SCL    | P12          | 1    | 1.8V      | IIC signal   |
| 17          | GND         | -            | -    | -         | GND          |
| 18          | GND         | -            | -    | -         | GND          |
| 19          | 3.3V        | -            | -    | -         | 3.3V power   |

| U13 Pin No. | Signal Name | FPGA Pin No. | BANK | I/O Level | Description |
|-------------|-------------|--------------|------|-----------|-------------|
| 20          | 3.3V        | -            | -    | -         | 3.3V power  |

## 3.7 LVDS-RX interface

### 3.7.1 Introduction

The board provides one LVDS-RX interface with 3 pairs of differential signals, which can also be used as GPIOs; the interface uses one 12P header (model TST-106-01-G-D) with 2.5mm pitch. The LVDS-RX connection diagram is shown in Figure 3-6.

Figure 3-6 Connection Diagram of LVDS-RX Interface



### 3.7.2 Pin Assignment

Table 3-5 Pin Distribution of LVDS-RX Interface

| J4 Pin No. | Signal Name | FPGA Pin No. | BANK | I/O Level | Description    |
|------------|-------------|--------------|------|-----------|----------------|
| 1          | 3.3V        | -            | -    | -         | 3.3V power     |
| 2          | 3.3V        | -            | -    | -         | 3.3V power     |
| 3          | GND         | -            | -    | -         | GND            |
| 4          | GND         | -            | -    | -         | GND            |
| 5          | NC          | -            | -    | -         | -              |
| 6          | NC          | -            | -    | -         | -              |
| 7          | F_LVDS1_1N  | P8           | 1    | 1.8V      | Receive signal |
| 8          | F_LVDS1_1P  | N8           | 1    | 1.8V      | Receive signal |
| 9          | F_LVDS1_2N  | P9           | 1    | 1.8V      | Receive signal |
| 10         | F_LVDS1_2P  | N9           | 1    | 1.8V      | Receive signal |
| 11         | F_LVDS1_3N  | P11          | 1    | 1.8V      | Receive signal |

| J4 Pin No. | Signal Name | FPGA Pin No. | BANK | I/O Level | Description    |
|------------|-------------|--------------|------|-----------|----------------|
| 12         | F_LVDS1_3P  | N11          | 1    | 1.8V      | Receive signal |

## 3.8 PCIe Interface

### 3.8.1 Introduction

The development board provides one PCIe-X4 interface. The connection diagram of PCIe interface is shown in Figure 3-7.

Figure 3-7 Connection Diagram of PCIe Interface



### 3.8.2 Pin Assignment

Table 3-6 Pin Distribution of PCIe Interface

| Signal Name   | FPGA Pin No. | BANK | I/O Level | Description             |
|---------------|--------------|------|-----------|-------------------------|
| PCIE_WAKE_B   | M1           | 3    | 3.3V      | The PCIe device wake-up |
| PCIE_PERST    | P2           | 3    | 3.3V      | PCIe device reset       |
| PCIE_CLK_QO_P | A8           | Q0   | -         | PCIe reference clock    |
| PCIE_CLK_QO_N | A7           | Q0   | -         | PCIe reference clock    |
| PCIE_RX0_P    | A2           | Q0   | -         | PCIe receive data       |
| PCIE_RX0_N    | A1           | Q0   | -         | PCIe receive data       |
| PCIE_RX1_P    | A4           | Q0   | -         | PCIe receive data       |
| PCIE_RX1_N    | A5           | Q0   | -         | PCIe receive data       |

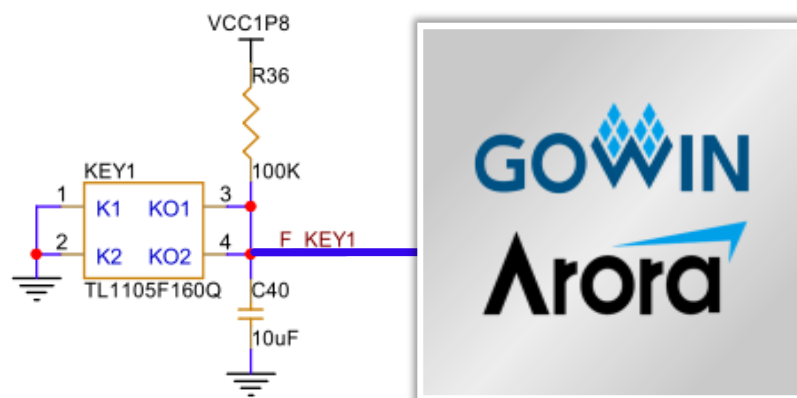
| Signal Name | FPGA Pin No. | BANK | I/O Level | Description        |
|-------------|--------------|------|-----------|--------------------|
| PCIE_RX2_P  | A10          | Q0   | -         | PCle receive data  |
| PCIE_RX2_N  | A11          | Q0   | -         | PCle receive data  |
| PCIE_RX3_P  | A13          | Q0   | -         | PCle receive data  |
| PCIE_RX3_N  | A14          | Q0   | -         | PCle receive data  |
| PCIE_TX0_P  | B3           | Q0   | -         | PCle transmit data |
| PCIE_TX0_N  | C3           | Q0   | -         | PCle transmit data |
| PCIE_TX1_P  | B6           | Q0   | -         | PCle transmit data |
| PCIE_TX1_N  | C6           | Q0   | -         | PCle transmit data |
| PCIE_TX2_P  | B8           | Q0   | -         | PCle transmit data |
| PCIE_TX2_N  | C8           | Q0   | -         | PCle transmit data |
| PCIE_TX3_P  | C12          | Q0   | -         | PCle transmit data |
| PCIE_TX3_N  | B12          | Q0   | -         | PCle transmit data |

## 3.9 Key & LED

### 3.9.1 Introduction

The development board provides one reset key connected to a general-purpose I/O pin in FPGA BANK1. When the key is pressed, the corresponding IO input voltage of the FPGA is low; when the key is not pressed, the corresponding IO input voltage of the FPGA is high. The connection diagram is shown in Figure 3-8.

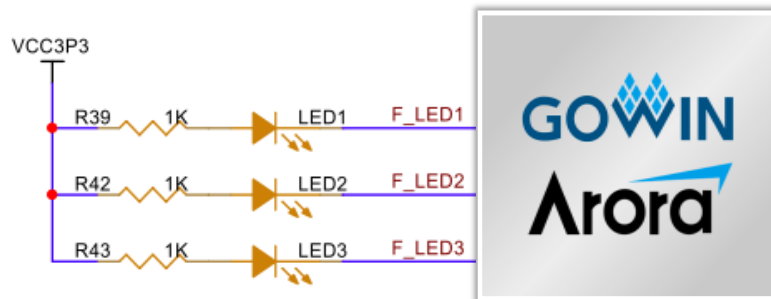
Figure 3-8 Connection Diagram of the Key



The development board includes three user LEDs. The user LEDs are

connected to the IO of FPGA BANK3&4 and can be switched on and off via the program. The user LEDs will be on when the IO voltage is high. The user LEDs will be off when the IO voltage is low. The connection diagram is shown in Figure 3-9.

**Figure 3-9 Connection Diagram of LED**



### 3.9.2 Pin Assignment

**Table 3-7 Pin Distribution of Key**

| Signal Name | FPGA Pin No. | BANK | I/O Level | Description |
|-------------|--------------|------|-----------|-------------|
| F_KEY1      | M8           | 1    | 1.8V      | Reset key   |

**Table 3-8 Pin Distribution of Indicators**

| Signal Name | FPGA Pin No. | BANK | I/O Level | Description   |
|-------------|--------------|------|-----------|---------------|
| F_LED1      | P1           | 3    | 3.3V      | LED indicator |
| F_LED2      | H2           | 4    | 3.3V      | LED indicator |
| F_LED2      | H3           | 4    | 3.3V      | LED indicator |

