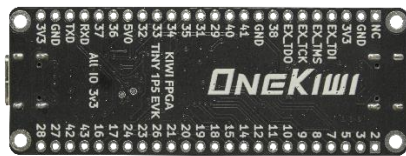
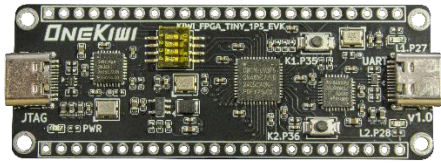


KIWI 1P5 FPGA BOARD

Gowin FPGA 1K5 LUTs, onboard high-speed USB-UART converter



- Main FPGA Chip: GW1N-UV1P5 on chip Flash
- Embedded 1584 FPGA LUTs
- Onboard Gowin GWU2X USB-JTAG debugger
- Onboard Button and LED
- **On-chip Flash – no need external Flash IC**
- Support JTAG DIP Switch program external FPGA

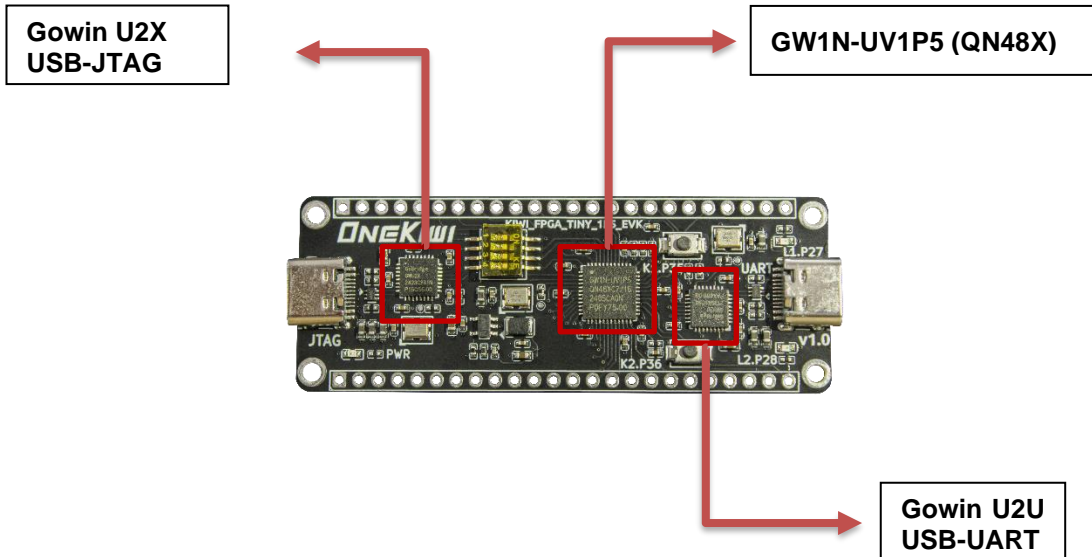
		Kiwi 1P5
FPGA Details	FPGA Chip	GW1N-UV1P5 GW1N-UV1P5QN48XC7/I6
	Logic Units	1584
	Hard processor	None
	Block SRAM (bits)	96K
	User Flash (bits)	256K
	Number of PLL	2
	Number of I/O Bank	6
	Number of user I/O	125
User Interface	User Button	02
	User LED	02
Programmer	Programmer IC	Gowin U2X Support Programming for External FPGA (Change Switch SW1)
Physical	Size	70mm x 22 mm
	Interface	Double row header pitch 2.54mm
Power	Main Voltage	5V
	I/O Voltage	All IO 3.3V
Environment	Temperature	Industrial: -40°C to 75°C
	Humidity	Humidity (Non-condensing): 10% - 90%

KIWI 1P5 FPGA BOARD

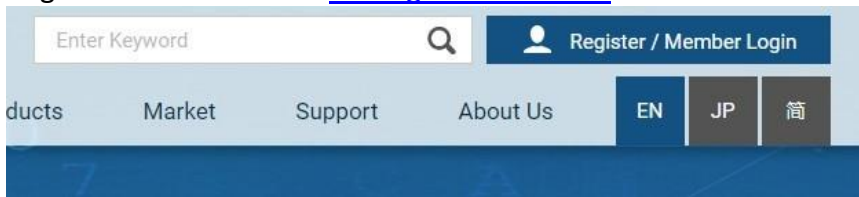
Gowin FPGA 1K5 LUTs, onboard high-speed USB-UART converter

Quick Start Guide

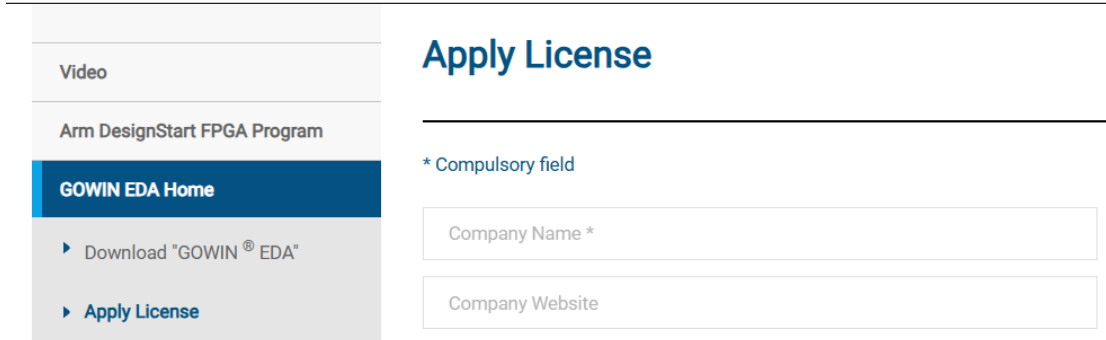
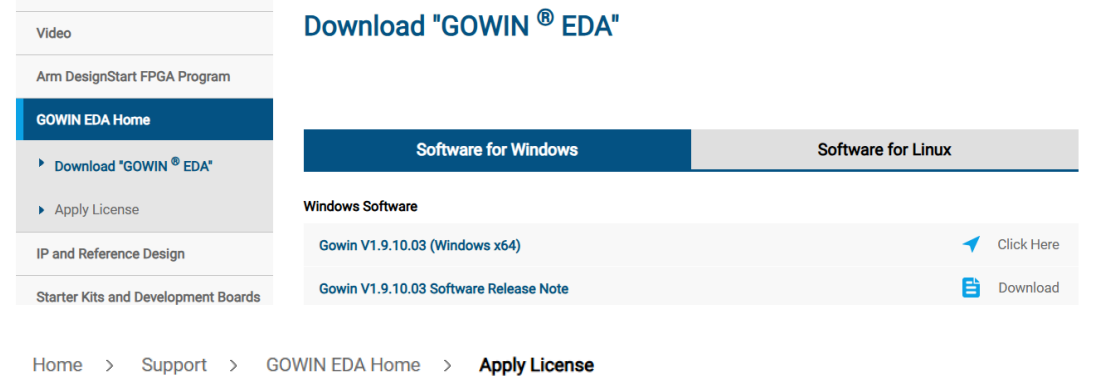
- Kiwi 1P5 Peripheral Description



- Register on the website: www.gowinsemi.com



- Download the GOWIN EDA Development Environment and Apply License https://www.gowinsemi.com/en/support/download_eda/



KIWI 1P5 FPGA BOARD

Gowin FPGA 1K5 LUTs, onboard high-speed USB-UART converter

Block Diagram and Pinout Table

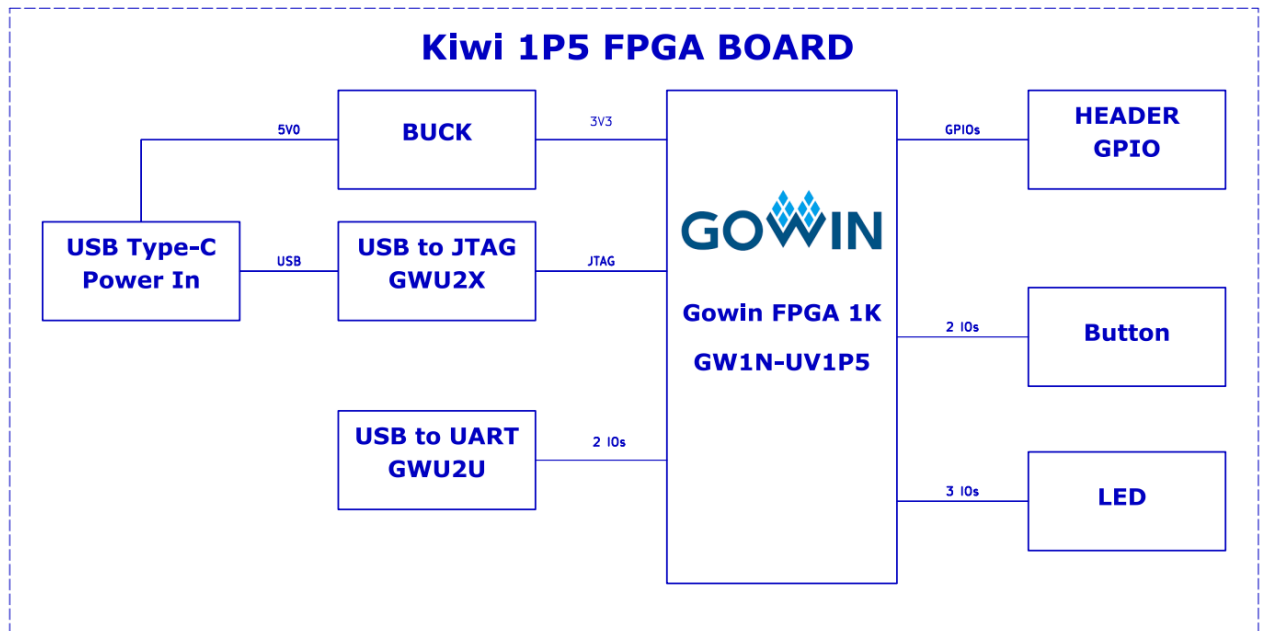


Fig 01. Kiwi 1P5 Block Diagram

KIWI 1P5 FPGA BOARD

Gowin FPGA 1K5 LUTs, onboard high-speed USB-UART converter

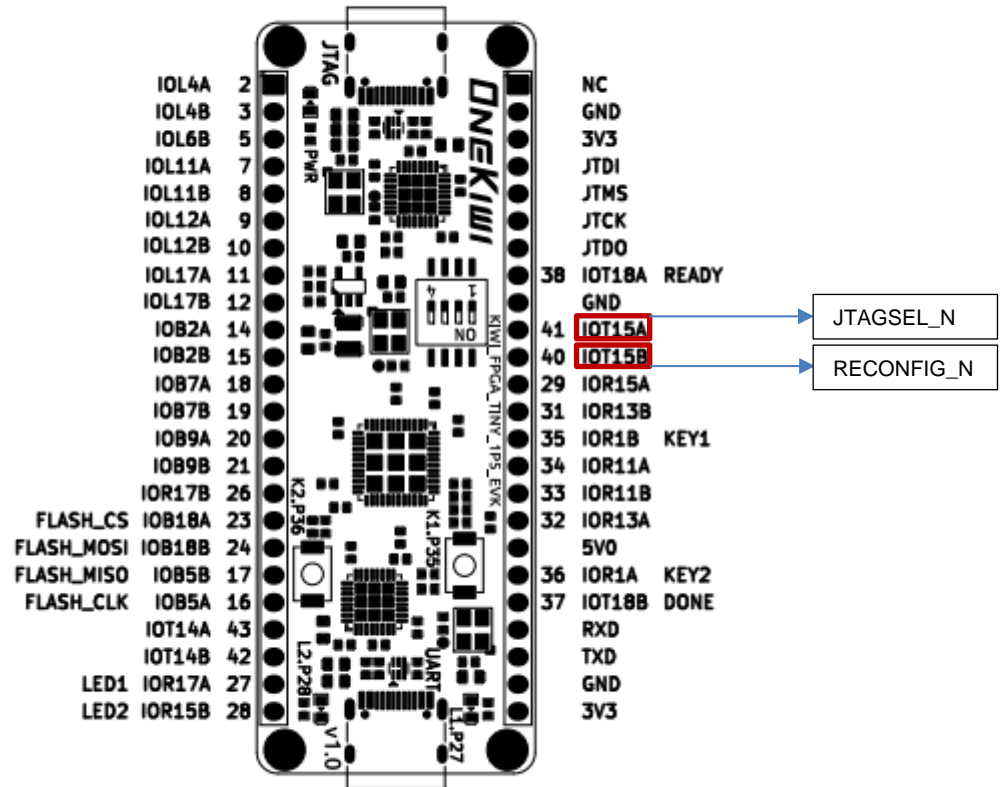


Fig 02. Kiwi 1P5 Pinout Mapping (All IO 3.3V voltage level)

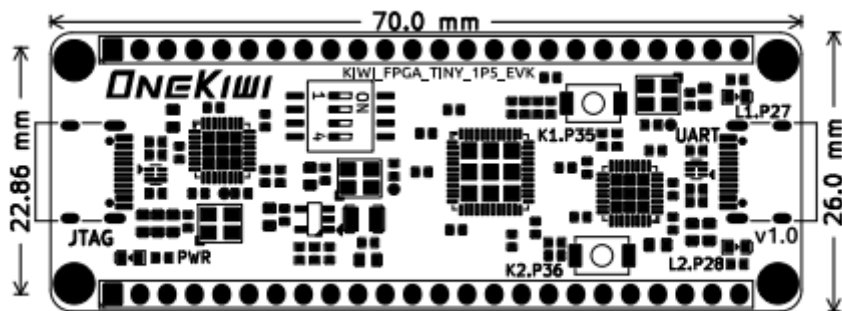
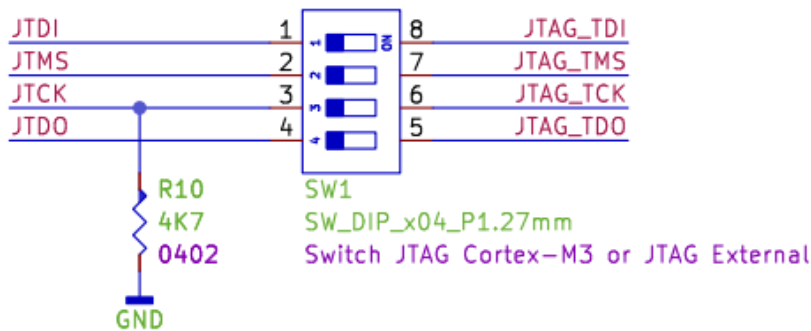


Fig 03. Kiwi 1P5 board dimension

KIWI 1P5 FPGA BOARD

Gowin FPGA 1K5 LUTs, onboard high-speed USB-UART converter

- JTAG Switch function instruction

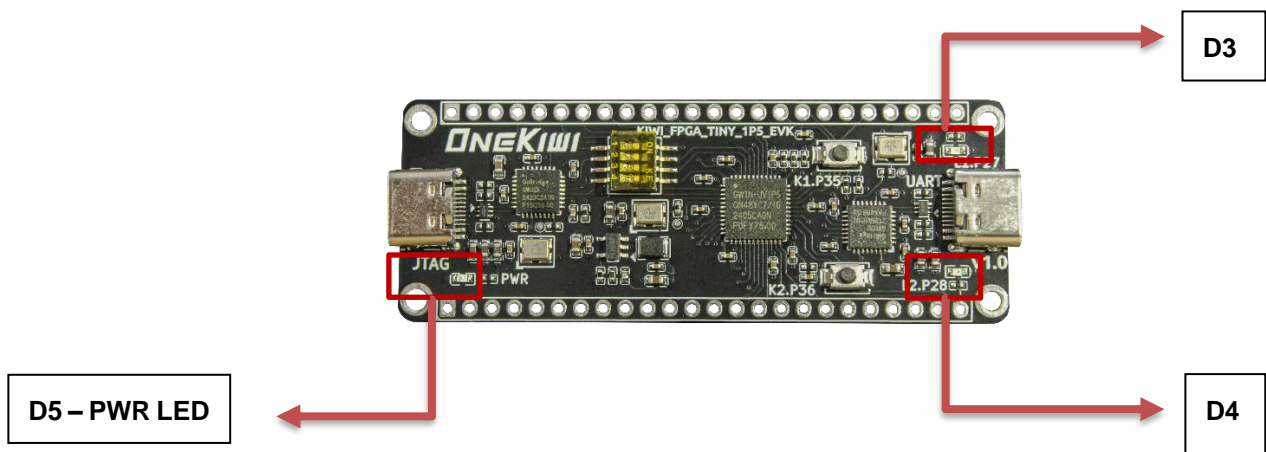
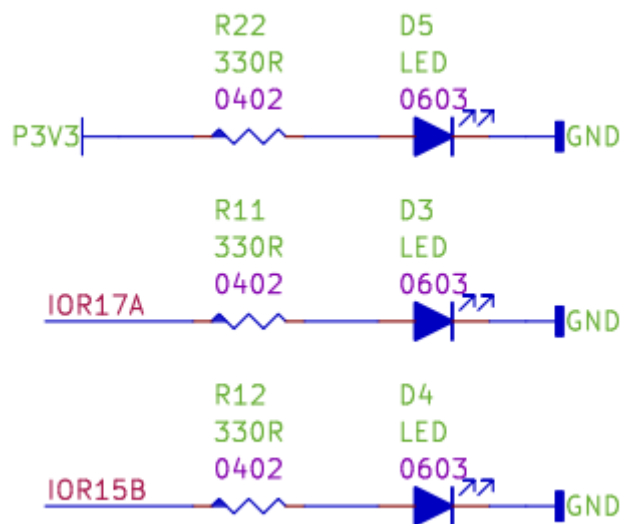


Switch ON: USB JTAG connected to FPGA chip

Switch OFF: Disconnect FPGA chip from USB-JTAG, can use programmer with external FPGA chip

- LED circuit description

There are total 3 LEDs available on the 1P5 board D3, D4, D5, maximum voltage 3.3V.

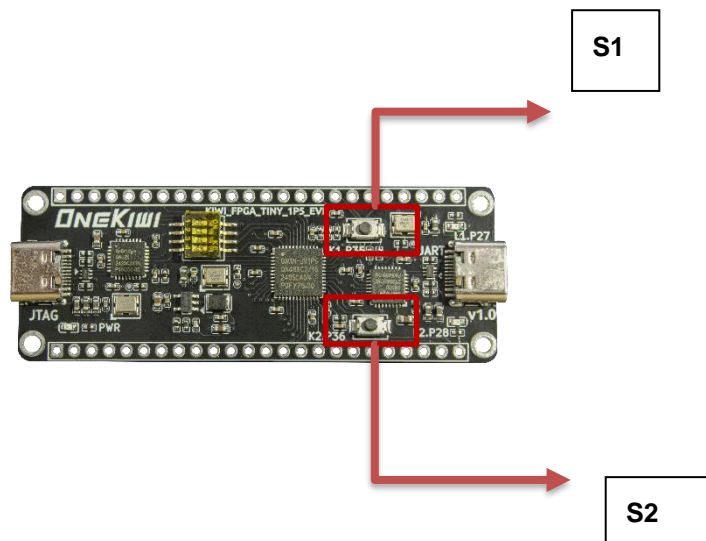
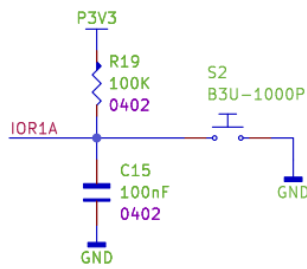
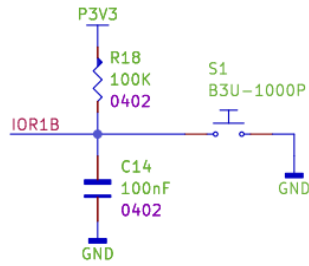


KIWI 1P5 FPGA BOARD

Gowin FPGA 1K5 LUTs, onboard high-speed USB-UART converter

- **Button circuit description**

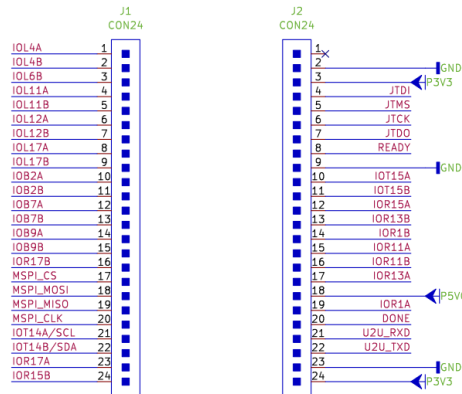
There are total 2 User buttons default Active Low with voltage level 3.3V



KIWI 1P5 FPGA BOARD

Gowin FPGA 1K5 LUTs, onboard high-speed USB-UART converter

- FPGA Pin assign list table



Note: There are some Pins with specific function you should not use as GPIOs:

- JTAG Pin: JTDI, JTMS, JTCK, JTDO, IOT15A (JTAGSEL_N)
- Reconfig Pin: IOT15B (RECONFIG_N)

Table 01: Pinout description CON24 – J1

Signal Name	Pin No.	J1 Pin No.	BANK	Description	I/O
IOL4A	2	1	5	General I/O	VCCIO5
IOL4B	3	2	5	General I/O	VCCIO5
IOL6B	5	3	5	General I/O Global Clock	VCCIO5
IOL11A	7	4	4	General I/O	VCCIO4
IOL11B	8	5	4	General I/O	VCCIO4
IOL12A	9	6	4	General I/O Global Clock	VCCIO4
IOL12B	10	7	4	General I/O	VCCIO4
IOL17A	11	8	3	General I/O	VCCIO3
IOL17B	12	9	3	General I/O	VCCIO3
IOB2A	14	10	2	General I/O	VCCIO2
IOB2B	15	11	2	General I/O	VCCIO2
IOB7A	18	12	2	General I/O	VCCIO2
IOB7B	19	13	2	General I/O Global Clock	VCCIO2
IOB9A	20	14	2	General I/O Global Clock	VCCIO2
IOB9B	21	15	2	General I/O Global Clock	VCCIO2
IOR17B	26	16	2	General I/O	VCCIO2
MSPI_CS	23	17	2	General I/O (Remapping) Special Pin MSPI	VCCIO2
MSPI_MOSI	24	18	2	General I/O (Remapping) Special Pin SPI SI	VCCIO2
MSPI_MISO	17	19	2	General I/O (Remapping) Special Pin SPI SO	VCCIO2
MSPI_CLK	26	20	2	General I/O (Remapping) Special Pin SPI CLK	VCCIO2
IOT14A/SCL	43	21	0	General I/O (Remapping) Special Pin I2C CLK	VCCIO0

KIWI 1P5 FPGA BOARD

Gowin FPGA 1K5 LUTs, onboard high-speed USB-UART converter

IOT14B/SDA	42	22	0	General I/O (Remapping) Special Pin I2C DATA	VCCIO0
IOR17A	27	23	2	General I/O	VCCIO2
IOR15B	28	24	2	General I/O	VCCIO2

Table 02: Pinout description CON24 – J2

Signal Name	Pin No.	J2 Pin No.	BANK	Description	I/O
NC	-	1	-	General I/O	
GND	-	2	-	General I/O	
P3V3	-	3	-	General I/O	
JTDI*	-	4	-	JTAG Pin	
JTMS*	-	5	-	JTAG Pin	
JTCK*	-	6	-	JTAG Pin	
JTDO*	-	7	-	JTAG Pin	
READY	38	8	0	General I/O JTAG READY	VCCIO0
GND	-	9	-	General I/O	
JTAGSEL_N	41	10	0	JTAG Pin	VCCIO0
RECONFIG_N	40	11	0	JTAG Pin	VCCIO0
IOR15A	29	12	2	General I/O	VCCIO2
IOR13B	31	13	2	General I/O	VCCIO2
IOR1B	35	14	2	General I/O	VCCIO2
IOR11A	34	15	2	General I/O Global Clock	VCCIO2
IOR11B	33	16	2	General I/O Global Clock	VCCIO2
IOR13A	32	17	2	General I/O	VCCIO2
P5V0	-	18	-		
IOR1A	36	19	2	General I/O	VCCIO2
DONE	37	20	0	JTAG DONE General I/O (Remapping)	VCCIO0
U2U_RXD	-	21	-	U2U Rx Pin	
U2U_TXD	-	22	-	U2U Tx Pin	
GND	-	23	-	General I/O	
P3V3	-	24	-	General I/O	

* Should not be used for General I/O Pin

KIWI 1P5 FPGA BOARD

Gowin FPGA 1K5 LUTs, onboard high-speed USB-UART converter

Development Board Suite

A development board suite includes the following items:

- 1 x KIWI 1P5 development board (1)
- 1 x USB Type-C cable (2)
- 2 x Header 2.54mm 24 pin (3)
- Carton Box (4)

