Gowin AXI to AHB Sync IP

User Guide

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Revision History

Date	Version	Description
04/18/2025	1.0E	Initial version published.
05/23/2025	1.1E	Reference deisgn added.
10/30/2026	1.1.1E	Updated the hardware reference design and software programming reference design.

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1 About This Guide

1.1 Purpose

The purpose of Gowin AXI to AHB Sync IP User Guide is to help you learn the features and usage of Gowin AXI to AHB Sync IP by providing the descriptions of the functions, signals, parameters, and reference design, etc. The software screenshots and the supported products listed in this manual are based on Gowin Software 1.9.12.04 (64-bit). As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at *www.gowinsemi.com*:

- *SUG100, Gowin Software User Guide*
- *SUG549, GMD(GOWIN MCU Designer) User Guide*
- *DS100, GW1N series of FPGA Products Data Sheet*
- *DS117, GW1NR series of FPGA Products Data Sheet*
- *DS821, GW1NS series of FPGA Products Data Sheet*
- *DS861, GW1NSR series of FPGA Products Data Sheet*
- *DS841, GW1NZ series of FPGA Products Data Sheet*
- *DS102, GW2A series of FPGA Products Data Sheet*
- *DS226, GW2AR series of FPGA Products Data Sheet*
- *DS971, GW2AN-18X &9X Data Sheet*
- *DS976, GW2AN-55 Data Sheet*
- *DS981, GW5AT series of FPGA Products Data Sheet*
- *DS1103, GW5A series of FPGA Products Data Sheet*

- *DS1239, GW5AST series of FPGA Products Data Sheet*
- *DS1105, GW5AS series of FPGA Products Data Sheet*
- *DS1108, GW5AR series of FPGA Products Data Sheet*
- *DS1118, GW5ART series of FPGA Products Data Sheet*

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
AHB	Advanced High performance Bus
AMBA	Advanced Microcontroller Bus Architecture
AXI	Advanced Extensible Interface
FPGAs	Field Programmable Gate Array
IP	Intellectual Property

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: *www.gowinsemi.com*

E-mail: *support@gowinsemi.com*

2 Overview

2.1 Introduction

Gowin AXI to AHB Sync IP is a protocol converter that is used to convert the AMBA AXI4 protocol to the AMBA AHB-Lite protocol, enabling AXI4 masters to access AHB-Lite slaves.

Table 2-1 Gowin AXI to AHB Sync IP Overview

Gowin AXI to AHB Sync IP	
Logic Resource	Please refer to Table 2-2.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.11.02 and above)

Note!

For the devices supported, you can click *here* to get the information.

2.2 Features

Gowin AXI to AHB Sync IP includes the following features:

- Compatible with AMBA AXI4 protocol
- Compatible with AMBA AHB-Lite protocol
- Configurable address width: 24-64 bits
- Configurable data width: 32 or 64 bits
- The AXI4 and AHB-Lite interfaces share the clock and reset signal.

- The AXI4 and AHB-Lite interfaces have the same address and data widths.
- Supports narrow transfers:
  - For 32-bit data bus: Supports 8-bit and 16-bit narrow transfers.
  - For 64-bit data bus: Supports 8-bit, 16-bit, and 32-bit narrow transfers.

2.3 Resource Utilization

Gowin AXI to AHB Sync IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW5AT series of FPGA as an instance, the resource utilization of Gowin AXI to AHB Sync IP is as shown in Table 2-2.

Table 2-2 Resource Utilization

Device	Resource	Resource Utilization	Configuration
GW5AT	Logic	704	Address Bus Width: 32 Data Bus Width: 32 AXI ID Width: 4
	Register	289	
	BSRAM	0	

3 Functional Description

It supports up to two outstanding read/write transactions (2R, 2W, or 1R1W).

If the AXI4 side is not ready for the next AHB-Lite transfer, AHB-Lite will initiate a BUSY or IDLE cycle.

The mapping between AXI4 burst types and AHB-Lite burst types is as shown in Table 3-1. If an AXI4 transaction crosses a 1 KB address boundary, an AXI4 incremental burst with AxLEN of 3, 7, or 15 will be converted into an AHB INCR burst.

Table 3-1 AXI4 and AHB-Lite Burst Type Mapping

ARBURST/AWBURST	ARLEN/AWLEN	HBURST	HBURST (cross 1K)
INCR	0	SINGLE	N/A
INCR	3	INCR4	INCR
INCR	7	INCR8	INCR
INCR	15	INCR16	INCR
INCR	1, 2, 4-6, 8-14, 16-255	INCR	INCR
FIX	0-15	SINGLE	N/A
WRAP	1	SINGLE	N/A
WRAP	3	WRAP4	N/A
WRAP	7	WRAP8	N/A
WRAP	15	WRAP16	N/A

Complies with the AHB-Lite 1 KB address boundary requirement.

If the AHB-Lite interface receives an error response, the remaining transfers in a burst will continue rather than be canceled.

Read and Write transaction arbitration priority is as described as below.

- An AXI4 write transaction participates in arbitration only after both the AXI4 write command and its first data transfer are received.

- In the first arbitration round, read transactions are usually prioritized over write transactions.
- If a write transaction loses arbitration to a read transaction, it will be cached. Such cached write transactions are categorized as "pending write transactions".
- The arbitration priority order is: Pending write transactions > Read transactions > Write transactions.

The orders of write transactions and read transactions are maintained separately, but the order between read and write transactions is not maintained.

For narrow AXI4 write transfers with partial write enable signals, only the designated WDATA bytes are written to the AHB-Lite interface.

Limitations and Constraints

1. Certain AXI signals are not supported, as listed in Table 3-2.

Table 3-2 Unsupported AXI Signals

Signal Name	Source	Description
Read/Write Address Channel		
AxQOS	Master	Quality of service
AxREGION	Master	Region identifier
AxUSER	Master	User signal
Low Power Interface		
CSYSREQ	Clock controller	System exit low-power state request
CSYSACK	Peripheral device	Exit low-power state acknowledgement
CACTIVE	Peripheral device	Clock active

2. RRESP/BRESP returns only OKAY or SLVERR, but DECERR and EXOKAY are not returned.
3. AXI4 signal to HPROT signal mapping is as shown in Table 3-3.

Table 3-3 AXI4 Signal to HPROT Signal Mapping

AXI signals	AHB-Lite signals
ARCACHE[0]/AWCACHE[0] (AXI4 bufferable/nonbufferable)	HPROT[2](bufferable)
ARCACHE[1]/AWCACHE[1] (AXI4 modifiable)	HPROT[3](cacheable)
ARCACHE[2]/AWCACHE[2] (AXI4 read allocate)	Ignored
ARCACHE[3]/AWCACHE[3] (AXI4 write allocate)	Ignored

AXI signals	AHB-Lite signals
ARPROT[0]/AWPROT[0] (AXI4 privileged/non-privileged)	HPROT[1](privileged/user access)
ARPROT[1]/AWPROT[1] (AXI4 secure/non-secure)	Secure accesses are not supported
ARPROT[2]/AWPROT[2] (AXI4 data/instruction access)	HPROT[0](data/opcode access) Note: HPROT[0] is the inverse of ARPROT[2]/AWPROT[2]

4. WSTRB Constraints

- Only AXI4 write transactions with single transfers support partial write enable signals.
  - When partial write enable signals are used, the transfer on the AHB-Lite interface will be converted into single or multiple narrow transfers.
  - If the write enable signal is zero, an IDLE transfer will be initiated on the AHB-Lite interface.
- For other AXI4 write transactions:
  - Partial write enable signals and zero write enable signals are not supported; otherwise, an SLVERR error will be reported.
  - The valid bytes of WDATA are determined by AWADDR and AWSIZE, independent of WSTRB.

4 Signal Descriptions

The port descriptions of Gowin AXI to AHB Sync IP are as shown in Table 4-1.

Table 4-1 Signal Descriptions

Signal	I/O	Data Width	Description
araddr	input	[ADDR_BUS_WIDTH[1] - 1:0]	AXI read address
arburst	input	[1:0]	AXI read burst type (0 = fixed, 1 = increment, 2 = wrap)
arcache	input	[3:0]	AXI read cache type
arid	input	[AXI_ID_WIDTH[2] - 1:0]	AXI read address ID tag
arlen	input	[7:0]	AXI read burst length (0=1 transfer, 1=2 transfers, …, 255=256 transfers)
arlock	input	1	AXI read lock type, only support normal access (arlock=0)
arprot	input	[2:0]	AXI read protection type
arready	output	1	AXI read address ready
arsize	input	[2:0]	AXI read burst size (0=1byte, 1=2bytes, 2=4bytes, 3=8bytes, others: unsupported)
arvalid	input	1	AXI read address valid
awaddr	input	[ADDR_BUS_WIDTH[1] - 1:0]	AXI write address
awburst	input	[1:0]	AXI write burst type (0 = fixed, 1 = increment, 2 = wrap)
awcache	input	[3:0]	AXI write cache type
awid	input	[AXI_ID_WIDTH[2] - 1:0]	AXI write address ID
awlen	input	[7:0]	AXI write burst length (0=1 transfer, 1=2 transfers, …, 255=256 transfers)
awlock	input	1	AXI write lock type, only support normal access (awlock = 0)

Signal	I/O	Data Width	Description
awprot	input	[2:0]	AXI write protection type
awready	output	1	AXI write address ready
awsize	input	[2:0]	AXI write burst size (0=1byte, 1=2bytes, 2=4bytes, 3=8bytes, others: unsupported)
awvalid	input	1	AXI write address valid
bid	output	[AXI_ID_WIDTH[2] - 1:0]	AXI write response ID
bready	input	1	AXI write response ready
bresp	output	[1:0]	AXI write response
bvalid	output	1	AXI write response valid
rdata	output	[DATA_BUS_WIDTH[3] - 1:0]	AXI read data
rid	output	[AXI_ID_WIDTH[2] - 1:0]	AXI read ID tag
rlast	output	1	AXI read last
rready	input	1	AXI read data ready
rresp	output	[1:0]	AXI read response
rvalid	output	1	AXI read data valid
wdata	input	[DATA_BUS_WIDTH[3] - 1:0]	AXI write data
wlast	input	1	AXI write last
wready	output	1	AXI write data ready
wstrb	input	[(DATA_BUS_WIDTH[3] / 8) - 1:0]	AXI write strobes
wvalid	input	1	AXI write data valid
clk	input	1	System bus clock
resetn	input	1	System bus reset
haddr	output	[ADDR_BUS_WIDTH[1] - 1:0]	AHB-Lite address bus
hburst	output	[2:0]	AHB-Lite burst type
hprot	output	[3:0]	AHB-Lite protection control
hrdata	input	[DATA_BUS_WIDTH[3] - 1:0]	AHB-Lite read data bus
hready	input	1	AHB-Lite transfer done
hresp	input	1	AHB-Lite transfer response
hsize	output	[2:0]	AHB-Lite transfer size
htrans	output	[1:0]	AHB-Lite transfer type
hwdata	output	[DATA_BUS_WIDTH[3] - 1:0]	AHB-Lite write data bus
hwrite	output	1	AHB-Lite read/write transfer signal

Note!

- [1]ADDR_BUS_WIDTH is the value of the Address Bus Width option.
- [2]AXI_ID_WIDTH is the value of the AXI ID Width option.
- [3]DATA_BUS_WIDTH is the value of the Data Bus Width option.

5 Parameter Description

The port descriptions of Gowin AXI to AHB Sync IP are as shown in Table 5-1.

Table 5-1 Parameter Description

Name	Description	Value	Default
Address Bus Width	Address bus width	24-64	32
Data Bus Width	Data bus width	32, 64	32
AXI ID Width	AXI ID tag width	1-16	4

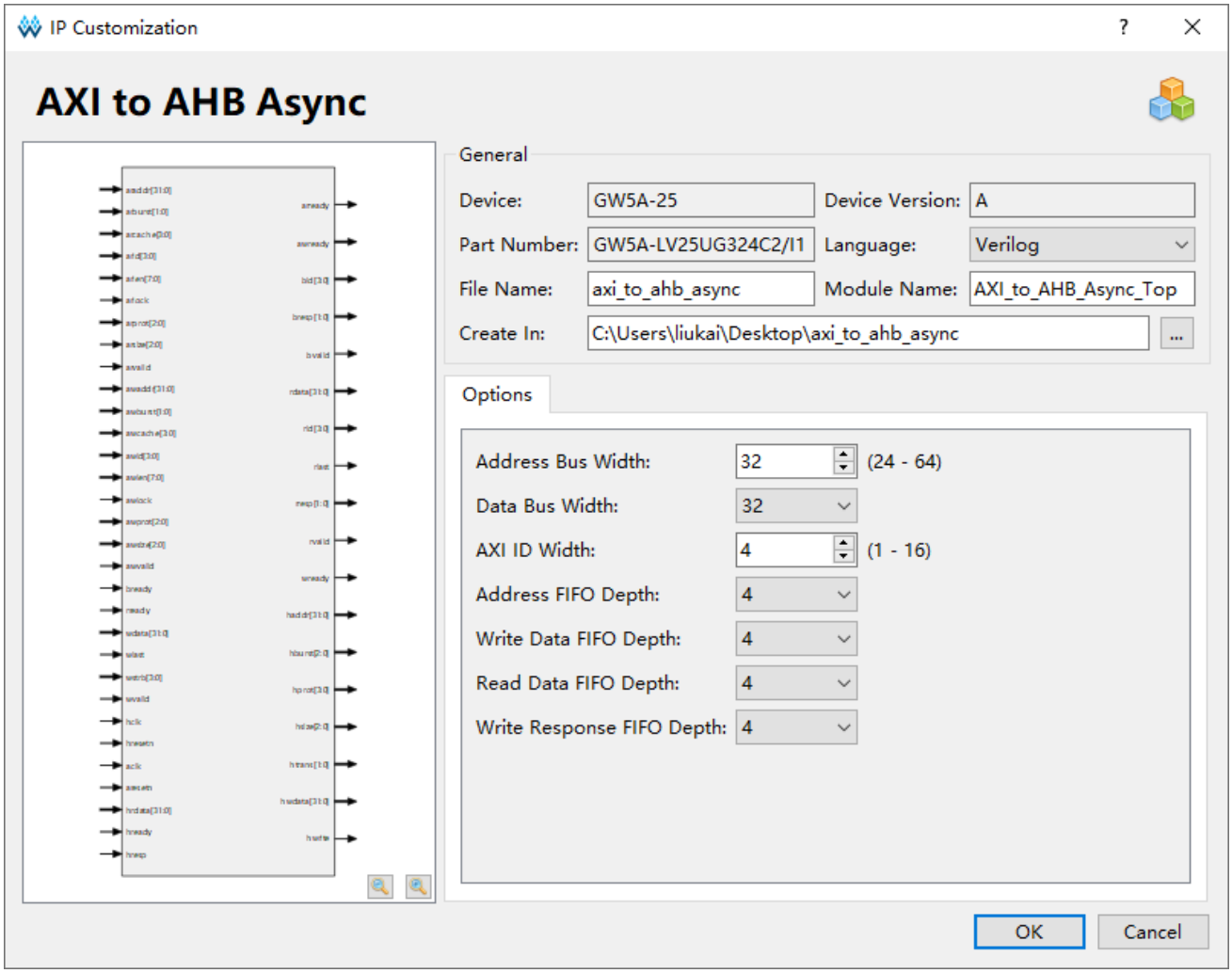
6 Interface Configuration

You can select IP Core Generator Tool in Gowin Software to call and configure Gowin AXI to AHB Sync IP.

Select "Tools > IP Core Generator" on the menu bar or click the “  ” on the tool bar to open IP Core Generator; then select "Soft IP Core > Microprocessor System > Bus Interconnect > AXI to AHB Sync 1.0”.

Gowin AXI to AHB Sync IP interface configuration is as shown in Figure 6-1.

Figure 6-1 Interface Configuration



The option configuration descriptions are as follows:

- Address Bus Width: The width of the address bus, with a range of 24 to 64, and a default value of 32.
- Data Bus Width: The width of the data bus, with values of 32 or 64, and a default value of 32.
- AXI ID Width: The width of the AXI ID tag, with a range of 1 to 16, and a default value of 4.

7 Application Scenarios

The application scenarios of Gowin AXI to AHB Sync IP generally include two cases. The first one is an AXI4 master device connected to an AHB-Lite interconnect, as shown in Figure 7-1. The second is an AXI4 master device connected to an AHB-Lite slave device, as shown in Figure 7-2. The HMASTLOCK input signal of the AHB-Lite slave device or interconnect must be set to low level, as the AXI to AHB Sync does not support locked transfers. The HSEL input signal of the AHB-Lite slave device or interconnect must be set to high level, as the transfer state is controlled by the HTRANS output signal from AXI to AHB Sync.

Figure 7-1 AXI Connected to AHB-Lite Interconnect

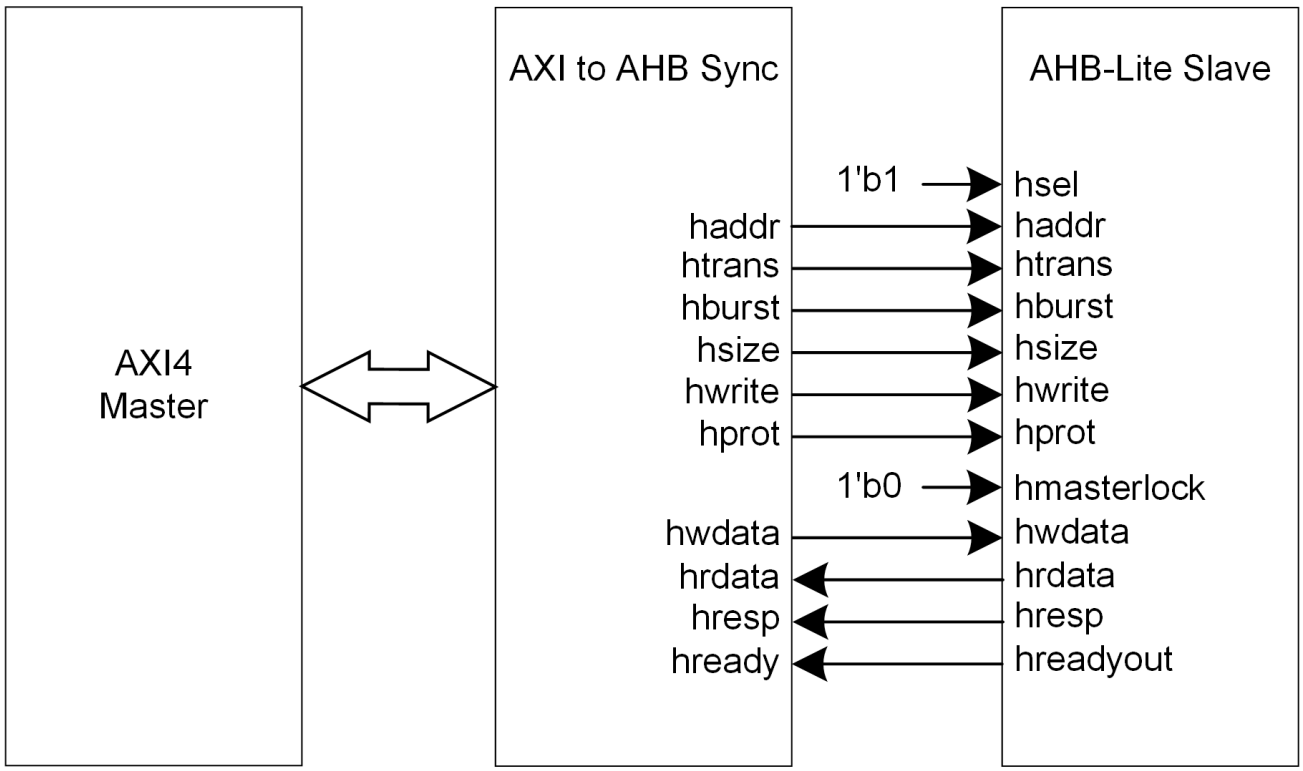
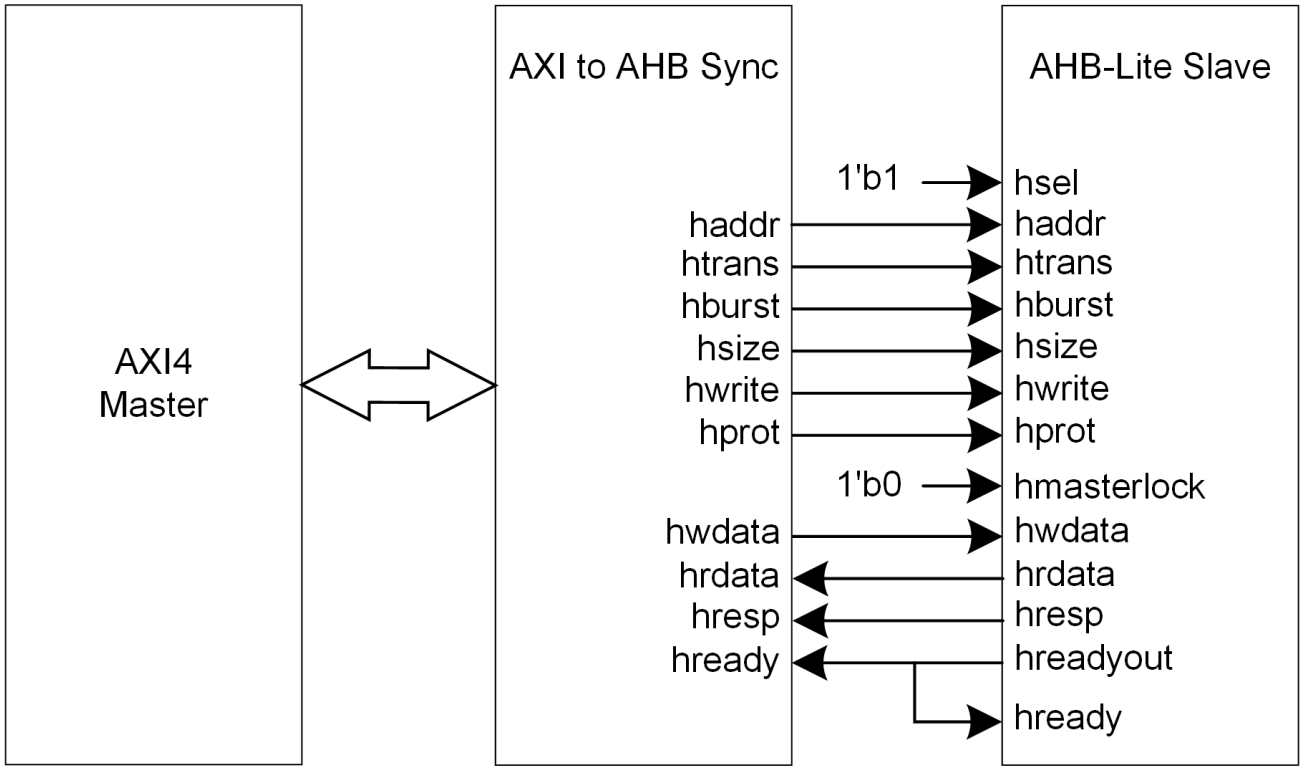


Figure 7-2 AXI Connected to AHB-Lite Slave Device



8 Reference Design

For more details, please refer to the *reference design* for Gowin AXI to AHB Sync IP on the Gowinsemi website:

- Hardware Reference Design:
  ...\ref_design\FPGA_RefDesign\DK_START_GW5A25_V2.0\axi2ahb_sync
- Software Reference Design:
  ...\ref_design\MCU_RefDesign\axi2abh_sync


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