



Gowin SDI Encoder IP User Guide

IPUG1205-1.5E, 03/27/2026

Copyright © 2026 Guangdong Gowin Semiconductor Corporation. All Rights Reserved.

GOWIN is a trademark of Guangdong Gowin Semiconductor Corporation and is registered in China, the U.S. Patent and Trademark Office, and other countries. All other words and logos identified as trademarks or service marks are the property of their respective holders. No part of this document may be reproduced or transmitted in any form or by any means, electronic, mechanical, photocopying, recording or otherwise, without the prior written consent of GOWINSEMI.

Disclaimer

GOWINSEMI assumes no liability and provides no warranty (either expressed or implied) and is not responsible for any damage incurred to your hardware, software, data, or property resulting from usage of the materials or intellectual property except as outlined in the GOWINSEMI Terms and Conditions of Sale. GOWINSEMI may make changes to this document at any time without prior notice. Anyone relying on this documentation should contact GOWINSEMI for the current documentation and errata.

Revision History

Date	Version	Description
04/11/2025	1.0E	Initial version published.
05/14/2025	1.1E	● Audio supported. ● Compatibility enhanced.
07/25/2025	1.2E	● Level B DS supported. ● IP port diagram and corresponding port descriptions updated. ● The reference design block diagram updated.
09/12/2025	1.3E	Level B DL supported.
01/16/2026	1.4E	● i and psf resolutions supported. ● Audio transmission at 1.485 Gbps/1.001 and 2.97 Gbps/1.001 supported.
03/27/2026	1.5E	● Added support for SD-SDI. ● Added support for dynamic rate switching among SD-SDI, HD-SDI, and 3G-SDI (148.5 MHz SerDes reference clock required). ● Updated the reference design.

Contents

Contents	i
List of Figures	ii
List of Tables	iii
1 About This Guide	1
1.1 Purpose	1
1.2 Related Documents	1
1.3 Terminology and Abbreviations	1
1.4 Support and Feedback	2
2 Overview	3
2.1 Overview	3
2.2 Features	3
2.3 Resource Utilization	3
3 Functional Description	5
3.1 System Block Diagram	5
3.2 Function Modules	5
3.3 Supported Format	6
3.4 Port List	6
3.5 Timing Description	9
4 Interface Configuration	10
5 Reference Design	12
6 File Delivery	13
6.1 Documentation	13
6.2 Design Source Code (Encryption)	13
6.3 Reference Design	13

List of Figures

Figure 3-1 Gowin SDI Encoder IP Block Diagram	5
Figure 3-2 Gowin SDI Encoder IP Block Diagram	5
Figure 3-3 Timing Diagram of Video Input Interface	9
Figure 4-1 Open IP Core Generator	10
Figure 4-2 Select SDI Encoder IP.....	11
Figure 4-3 Gowin SDI Encoder IP Configuration Interface	11
Figure 5-1 Block Diagram of Reference Design	12

List of Tables

Table 1-1 Terminology and Abbreviations	1
Table 2-1 Gowin SDI Encoder IP	3
Table 2-2 Gowin SDI Encoder IP Resource Utilization	4
Table 3-1 Formats Supported by Gowin SDI Encoder IP	6
Table 3-2 I/O List of Gowin SDI Encoder IP	6
Table 6-1 Document List	13
Table 6-2 File List of Gowin SDI Encoder IP	13
Table 6-2 Gowin SDI Encoder IP RefDesign Folder Content List	13

1 About This Guide

1.1 Purpose

The purpose of Gowin SDI Encoder IP is to help you learn the features and usage of Gowin SDI Encoder IP by providing the descriptions of features, functions, ports, timing, GUI and reference design, etc. The software screenshots and the supported products listed in this manual are based on Gowin Software 1.9.12.02 (64-bit). As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI website. You can find the related documents at www.gowinsemi.com:

- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1239, GW5AST series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)
- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1118, GW5ART series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
DE	Data Enable
FPGA	Field Programmable Gate Array
HS	Horizontal Sync
IP	Intellectual Property
SDI	Serial Digital Interface

Terminology and Abbreviations	Meaning
SerDes	Serializer/Deserializer
SMPTE	Society of Motion Picture and Television Engineers
VESA	Video Electronics Standards Association
VS	Vertical Sync

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Overview

The Serial Digital Interface (SDI) is a member of the digital video interface family and is used for transmitting digital video signals. Gowin SDI Encoder IP can be operated under SD, HD or 3G rate standards defined by the Society of Motion Picture and Television Engineers (SMPTE), converting video signals into SDI signals.

Table 2-1 Gowin SDI Encoder IP

Gowin SDI Encoder IP	
Logic Resource	Please refer to Table 2-2.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.11 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Features

- Operates with 1 lane
- Supports link rates of 0.27/1.485/2.97 Gbps per lane
- Supports SD-SDI, HD-SDI, 3G-SDI
- Supports audio
- Supports Level B DS
- Supports Level B DL

2.3 Resource Utilization

Gowin SDI Encoder IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades.

Taking Gowin GW5AT series of FPGA as an instance, the resource utilization of Gowin SDI Encoder IP is as shown in Table 2-2.

Table 2-2 Gowin SDI Encoder IP Resource Utilization

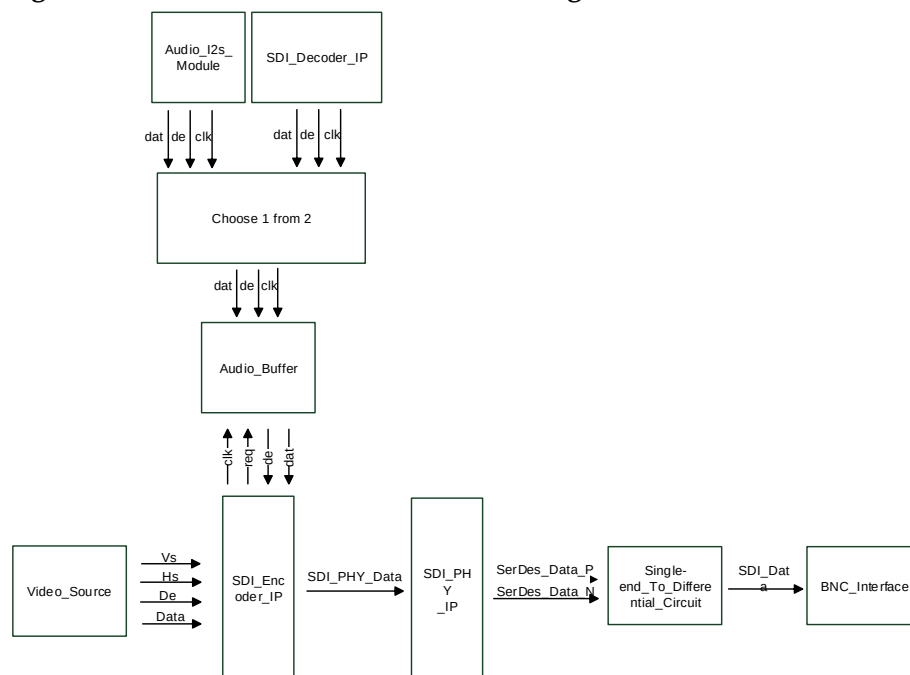
Device	GW5AT-60
Register	3360
LUT	3188
BSRAM	16

3 Functional Description

3.1 System Block Diagram

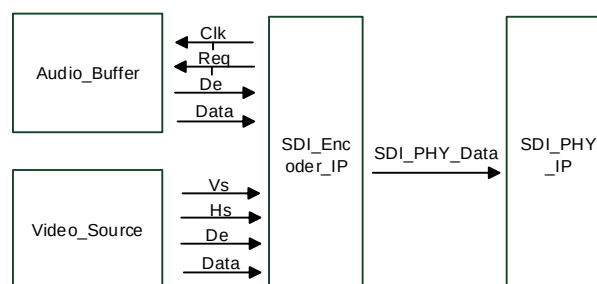
Gowin SDI Encoder IP can convert video signals into SDI signals. The SDI signal is then connected into the SDI PHY IP. The block diagram of Gowin SDI Encoder IP is as shown in Figure 3-1.

Figure 3-1 Gowin SDI Encoder IP Block Diagram



3.2 Function Modules

Figure 3-2 Gowin SDI Encoder IP Block Diagram



As shown in the diagram above, Gowin SDI Encoder IP can convert video data into SDI data.

3.3 Supported Format

Table 3-1 shows the formats supported by Gowin SDI Encoder IP.

Table 3-1 Formats Supported by Gowin SDI Encoder IP

Standard	SD-SDI		HD-SDI and Level B DS					3G-SDI	
Hor Addr Pixel	720	720	1280	1280	1920	1920	1920	1920	1920
Ver Addr Line	480	576	720	720	1080	1080	1080	1080	1080
Hor Total Pixel	858	864	1650	1980	2200	2640	2750	2200	2640
Ver Total Line	525	625	750	750	1125	1125	1125	1125	1125
Scan Mode	I	I	P	P	P,PSF,I	P,PSF,I	P,PSF	P	P
Frame Rate	59.94I	50I	60P 59.94P	50P	30P/PSF 60I 29.97P/PSF 59.94I	25P/PSF 50I	24P/PSF 23.98P/PSF	60P 59.94P	50P
Bit Per Word	20	20	20	20	20	20	20	20	20
Word Rate(Mhz)	13.5	13.5	74.25	74.25	74.25	74.25	74.25	148.5	148.5
Pixel Sample Rate(Mhz)	13.5	13.5	74.25	74.25	74.25	74.25	74.25	148.5	148.5
Structure	YC4:2:2	YC4:2:2	YC4:2:2	YC4:2:2	YC4:2:2	YC4:2:2	YC4:2:2	YC4:2:2	YC4:2:2
Pixel Depth	10	10	10	10	10	10	10	10	10

3.4 Port List

The IO ports vary slightly depending on the parameters.

The details of IO port of Gowin SDI Encoder IP are shown in Table 3-2.

Table 3-2 I/O List of Gowin SDI Encoder IP

Signal Name	Direction	Width	Description
I_rst_n	I	1	Reset signal, active-low.
I_drp_clk	I	1	DRP port configuration
I_pll_sel	I	2	PLL selection: 0: CPLL 1: QPLL0 2: Reserved 3: Reserved
I_config_en	I	1	Drp enable: 0: Disable 1: Enable (Effective only when the SerDes reference clock is 148.5 MHz for dynamic rate switching)

Signal Name	Direction	Width	Description
I_config_st	I	1	When I_config_en = 1, the configuration rate is updated on the rising edge of I_config_st.
I_rate_sel	I	2	Rate selection: 0: sd-sdi 1: hd-sdi 2: 3g-sdi (level a and level b dl) 3: 3g-sdi (level b ds)
I_q_sel	I	1	SerDes BANK Q selection: 0: Q0 1: Q1
I_lane_mask	I	4	SerDes Lane enable: 4b0001: lane 0 enable 4b0010: lane 1 enable 4b0100: lane 2 enable 4b1000: lane 3 enable
O_drp_wren	O	1	DRP Port write enable (Connect according to the reference design; no user operation required)
O_drp_addr	O	24	DRP Port write address (Connect according to the reference design; no user operation required)
O_drp_wrdata	O	32	DRP Port write data (Connect according to the reference design; no user operation required)
O_drp_rden	O	1	DRP Port read enable (Connect according to the reference design; no user operation required)
I_drp_rddata	I	32	DRP Port read data (Connect according to the reference design; no user operation required)
I_drp_rdvld	I	1	DRP Port read valid (Connect according to the reference design; no user operation required)
I_drp_ready	I	1	DRP Port read ready (Connect according to the reference design; no user operation required)
I_soft_rst_n	I	1	Reset signal, active-low; reset all internal IP logic except the DRP block.
I_level	I	2	Level selection 0: Level A 1: Level B DS 2: Level B DL 3: Reserved
I_rate	I	3	Rate input: 0: SD-SDI 1: HD-SDI 2: 3G-SDI

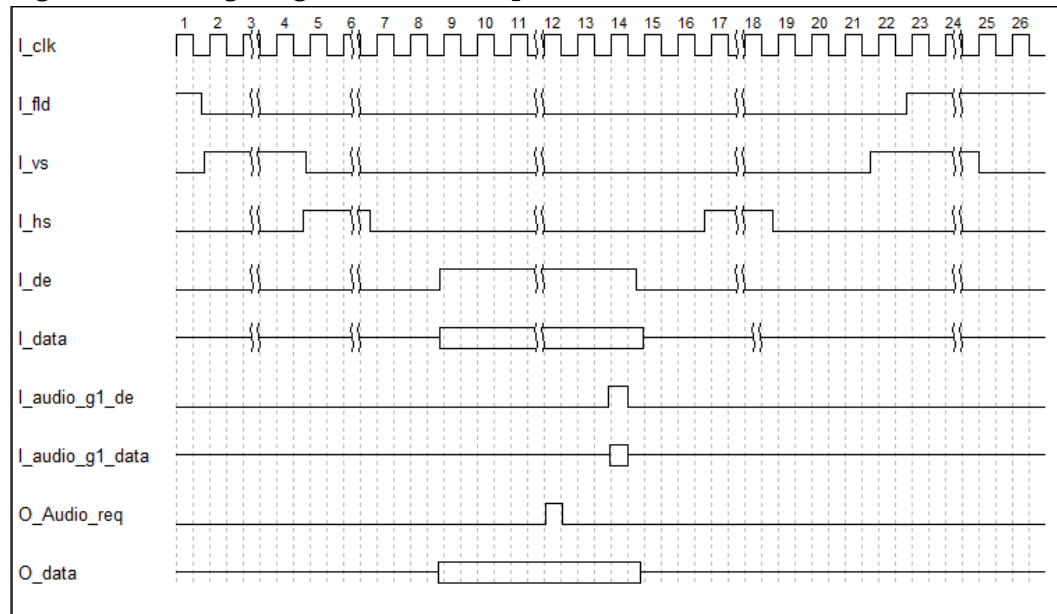
Signal Name	Direction	Width	Description
			3-7: Reserved
I_hres	I	16	Horizontal resolution input
I_vres	I	16	Vertical resolution input
I_ver_fre	I	3	Vertical frequency input 0: 60 Hz 1: 50 Hz 2: 30 Hz 3: 25 Hz 4: 24 Hz
I_interlace_trans	I	1	Transmission input: 0: Interlaced transmission (I) 1: Progressive transmission (P)
I_interlace	I	1	Scanned image input: 0: Interlaced image (I) 1: Progressive image (P)
I_color	I	1	Color input 0: YC 1: Reserved
I_mfactor	I	1	Rate Factor: 0: m = standard rate / 1 1: m = standard rate / 1.001
I_pixbit	I	1	Pixel bit input 0: 10 bits 1: Reserved
I_pixstruc	I	2	Pixel structure input 2'b00: 4:2:2 2'b01: Reserved 2'b10: Reserved 2'b11: Reserved
I_clk	I	1	Clock input
I fld	I	1	Video field input (odd/even)
I_vs	I	1	Video VS (vertical sync) input (positive polarity)
I_hs	I	1	Video HS (horizontal sync) input (positive polarity)
I_de	I	1	Video DE (data enable) input
I_data	I	40	Video data input 20 bits for Level A 40 bits for Level B DS (SerDes rate set to 2.97, Data Width = 20, Data Ratio = 1:2)
I_audio_g1_de	I	1	Audio DE input, 48 KHz
I_audio_g1_data	I	96	Audio data input
O_audio_req	O	1	Audio data request, 48 KHz

Signal Name	Direction	Width	Description
O_data	O	80	Encoded data output, connected to Gowin SDI PHY IP.

3.5 Timing Description

This section introduces the timing of Gowin SDI Encoder IP. Figure 3-3 shows the input interface timing diagram of Gowin SDI Encoder IP. For standard video, simply connect the corresponding signals, and the IP will perform encoding. The encoded data is then output to Gowin SDI PHY IP.

Figure 3-3 Timing Diagram of Video Input Interface



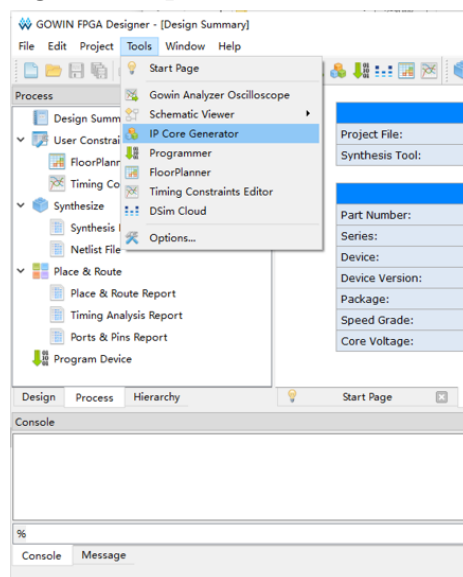
4 Interface Configuration

You can use IP core generator tool in Gowin Software to call and configure Gowin SDI Encoder IP.

1. Open IP Core Generator

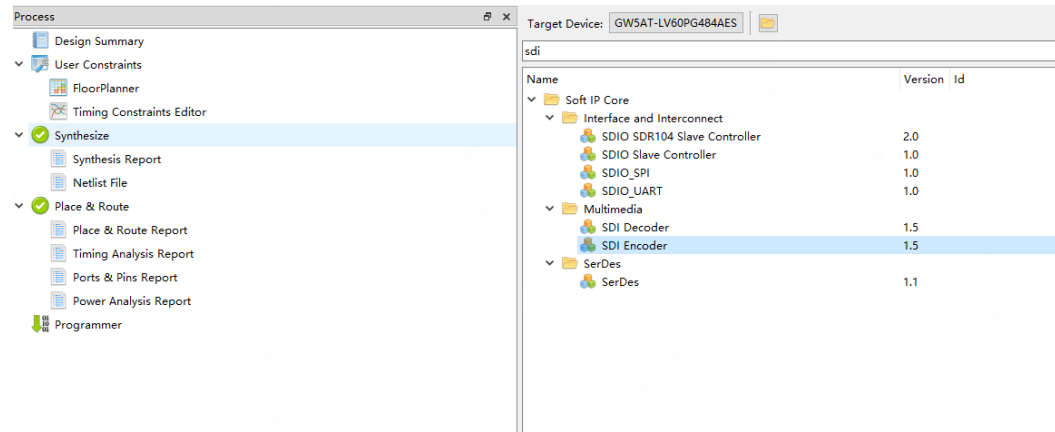
After creating the project, click the "Tools" tab in the upper left, click "IP Core Generator" from the drop-down list to open Gowin IP Core Generator, as shown in Figure 4-1.

Figure 4-1 Open IP Core Generator



2. Select SDI Encoder IP.

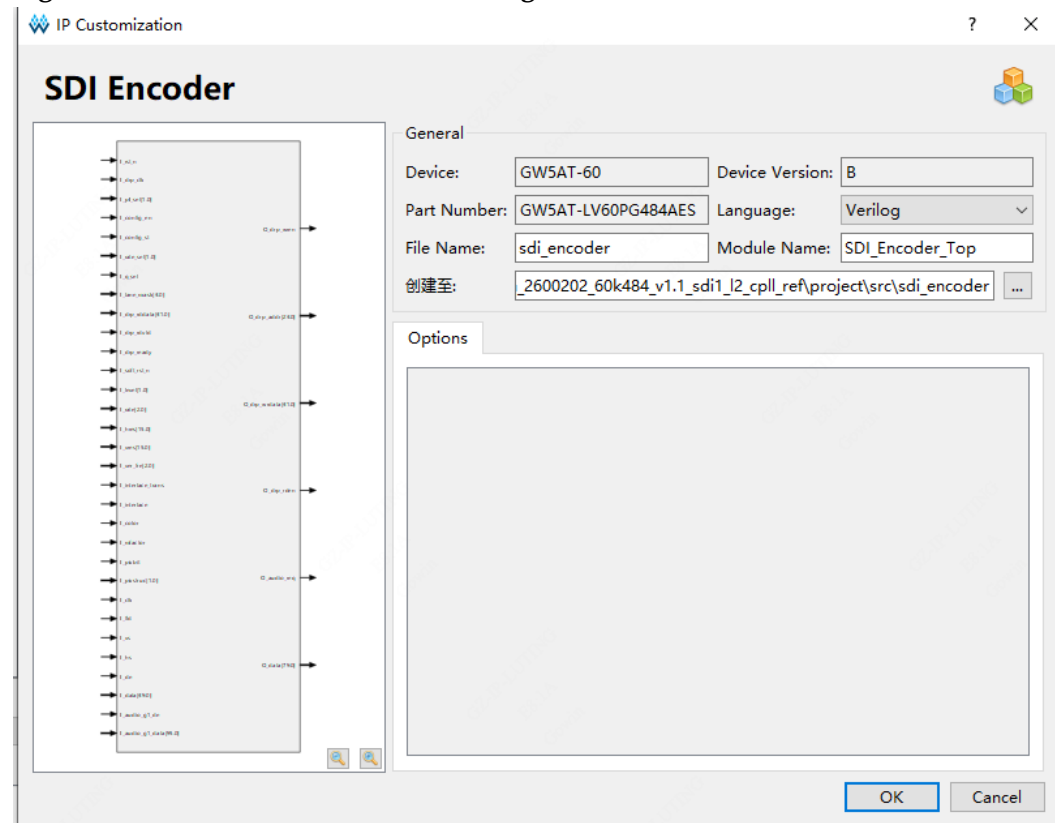
Double Click "Multimedia" and select SDI Encoder to open SDI Encoder IP configuration interface, as shown in Figure 4-2.

Figure 4-2 Select SDI Encoder IP

3. Gowin SDI Encoder IP Configuration Interface

First configure “General” tab in the SDI Encoder IP interface as shown in Figure 4-3.

- Device, Device Version, Part Number: Part number settings, determined by the current project, and the user can not configure it.
- Language: Supports Verilog and VHDL; choose the language as requirements, and the default is Verilog.
- File Name, Module Name, Create In: Displays SerDes file name, module name and the generated file path.

Figure 4-3 Gowin SDI Encoder IP Configuration Interface

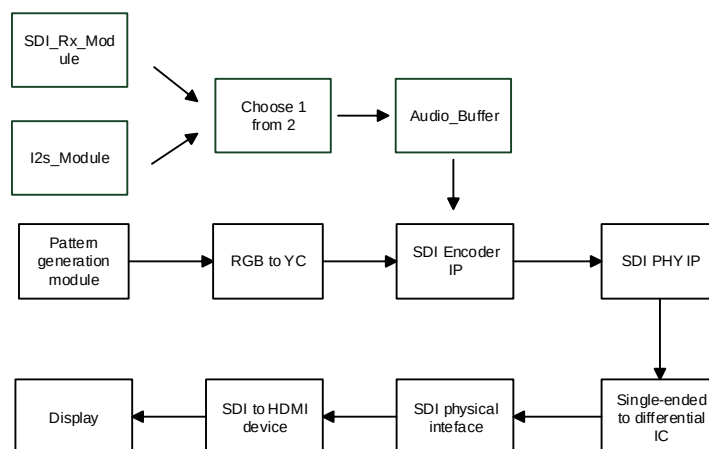
4. Click "OK" directly to generate the IP.

5 Reference Design

This chapter is intended to introduce the usage and structure of the [reference design](#) of Gowin SDI Encoder IP. Please see the SDI Encoder IP Reference Design for details at Gowinsemi website.

This reference design takes DK_START_GW5AT-LV60PG484A_V1.1 development board as an example. For more information about DK_START_GW5AT-LV60PG484A_V1.1 development board, please refer to Gowinsemi website. The block diagram of reference design is shown in Figure 5-1.

Figure 5-1 Block Diagram of Reference Design



6 File Delivery

The file delivery for Gowin SDI Encoder IP includes the documentation, the design source code, and the reference design.

6.1 Documentation

Table 6-1 Document List

Name	Description
IPUG1025, Gowin SDI Encoder IP User Guide	Gowin SDI Encoder IP User Guide, i.e., this manual.

6.2 Design Source Code (Encryption)

The encrypted code folder contains encrypted RTL code for Gowin SDI Encoder IP. This code is intended for use with GUI to generate the IP core as needed.

Table 6-2 File List of Gowin SDI Encoder IP

Name	Description
sdi_encoder.v	SDI Decoder IP File, encrypted.

6.3 Reference Design

The RefDesign folder contains the netlist files, user reference designs, constraints files, top-level files, and project files for Gowin SDI Encoder IP and Gowin SDI Decoder IP.

Table 6-2 Gowin SDI Encoder IP RefDesign Folder Content List

Name	Description
video_top.v	The top module of reference design
testpattern.v	Test pattern generation module
dk_video.cst	Project physical constraints file
dk_video.sdc	Project timing constraints file
key_debounceN.v	Key debouncing
adv7513_iic_init.v	adv7513 configuration file
yc_to_rgb	yc_to_rgb folder
rgb_to_yc	rgb_to_yc folder
i2c_master	I2c_master folder, encrypted.

Name	Description
sdi_decoder	sdi_decoder folder, encrypted.
sdi_encoder	sdi_decoder folder, encrypted.
serdes	SerDes project folder, encrypted.
gowin_pll	gowin_pll folder
sdi_audio_buffer_pro	sdi_audio_buffer_pro folder
i2s_interface	i2s_interface folder

