



Gowin SDI PHY IP User Guide

IPUG1206-1.1E, 07/25/2025

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Revision History

Date	Version	Description
04/11/2025	1.0E	Initial version published.
07/25/2025	1.1E	DRP Port configuration option added to support the adaptive functionality of Gowin SDI Decoder IP.

Contents

Contents	i
List of Figures	ii
List of Tables	iii
1 About This Guide	1
1.1 Purpose	1
1.2 Related Documents	1
1.3 Terminology and Abbreviations	2
1.4 Support and Feedback	2
2 Overview	3
2.1 Overview	3
2.2 Features	3
2.3 Resource Utilization	3
3 Functional Description	5
3.1 System Block Diagram	5
3.2 Function Modules	5
3.2.1 TX	5
3.2.2 RX	6
3.2.3 SerDes Clock	6
3.2.4 SerDes Data	6
3.3 Supported Format	7
3.4 Port List	7
3.5 Parameter Configuration	9
3.6 Timing Description	10
4 Interface Configuration	11
5 Reference Design	17
6 File Delivery	18
6.1 Documentation	18
6.2 Design Source Code (Encryption)	18
6.3 Reference Design	18

List of Figures

Figure 3-1 Gowin SDI PHY IP System Diagram	5
Figure 3-2 Structure Diagram of Gowin SDI PHY IP TX	5
Figure 3-3 Structure Diagram of Gowin SDI PHY IP RX.....	6
Figure 3-4 Gowin SDI PHY IP Port Diagram.....	7
Figure 3-5 Timing Diagram of Video Input Interface	10
Figure 3-6 Timing Diagram of Video Output Interface.....	10
Figure 4-1 Open IP Core Generator	11
Figure 4-2 Open SerDes IP Configuration Interface	12
Figure 4-3 Open SDI PHY Configuration Interface	13
Figure 4-4 SDI PHY Configuration Interface	13
Figure 4-5 General Tab	14
Figure 4-6 PHY Configuration Tab	15
Figure 4-7 SDI PHY IP in SerDes IP Configuration Interface.....	16
Figure 5-1 Block Diagram of Reference Design	17

List of Tables

Table 1-1 Terminology and Abbreviations	2
Table 2-1 Gowin SDI PHY IP Overview	3
Table 2-2 Gowin SDI PHY IP Resource Utilization	4
Table 3-1 Formats Supported by Gowin SDI PHY IP	7
Table 3-2 I/O List of Gowin SDI PHY IP	8
Table 3-3 Gowin SDI PHY IP Parameter.....	9
Table 6-1 Document List.....	18
Table 6-2 File List of Gowin SDI PHY IP	18
Table 6-3 Gowin SDI PHY IP RefDesign Folder Content List	18

1 About This Guide

1.1 Purpose

The purpose of Gowin SDI PHY IP is to help you learn the features and usage of Gowin SDI PHY IP by providing the descriptions of features, functions, ports, timing, GUI and reference design, etc. The software screenshots and the supported products listed in this manual are based on Gowin Software 1.9.11.03 (64-bit). As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI website. You can find the related documents at www.gowinsemi.com:

- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1239, GW5AST series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)
- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1118, GW5ART series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
DE	Data Enable
FPGA	Field Programmable Gate Array
HS	Horizontal Sync
IP	Intellectual Property
SDI	Serial Digital Interface
SerDes	Serializer/Deserializer
SMPTE	Society of Motion Picture and Television Engineers
VESA	Video Electronics Standards Association
VS	Vertical Sync

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Overview

The Serial Digital Interface (SDI) is a member of the digital video interface family and is used for transmitting digital video signals. Gowin SDI Encoder IP can be operated under HD or 3G rate standards defined by the Society of Motion Picture and Television Engineers (SMPTE), and is capable of functioning as both a transmitter and a receiver simultaneously.

Table 2-1 Gowin SDI PHY IP Overview

Gowin SDI PHY IP	
Logic Resource	Please refer to 2.3 Resource Utilization.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.11 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Features

- Operates with 1 lane
- Supports link rates of 1.485/2.97 Gbps per lane
- Supports HD-SDI and 3G-SDI

2.3 Resource Utilization

Gowin SDI PHY IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW5AST series of FPGA as an instance, when the DRP Port is enabled, the resource utilization of Gowin SDI PHY IP is as shown in Table 2-2.

Table 2-2 Gowin SDI PHY IP Resource Utilization

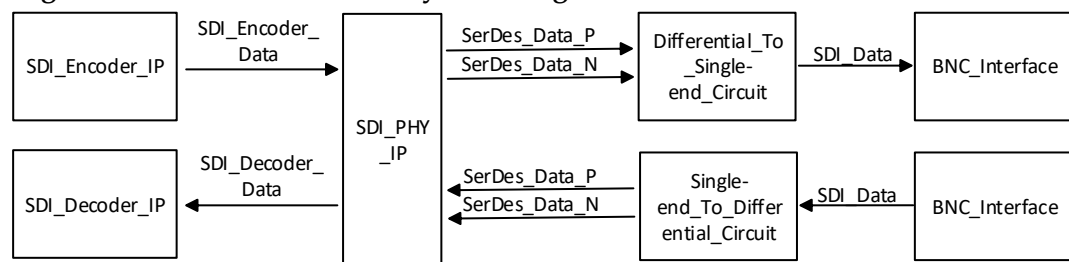
Device	GW5AST-60
Register	147
LUT	235

3 Functional Description

3.1 System Block Diagram

The function of Gowin SDI PHY IP TX is to convert parallel data into serial data. The function of Gowin SDI PHY IP RX is to convert serial data into parallel data. The system diagram of Gowin SDI PHY IP is shown in Figure 3-1.

Figure 3-1 Gowin SDI PHY IP System Diagram

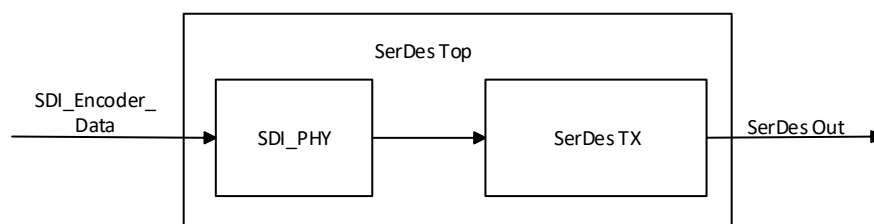


3.2 Function Modules

3.2.1 TX

The structure diagram of Gowin SDI PHY IP TX is shown in Figure 3-2.

Figure 3-2 Structure Diagram of Gowin SDI PHY IP TX



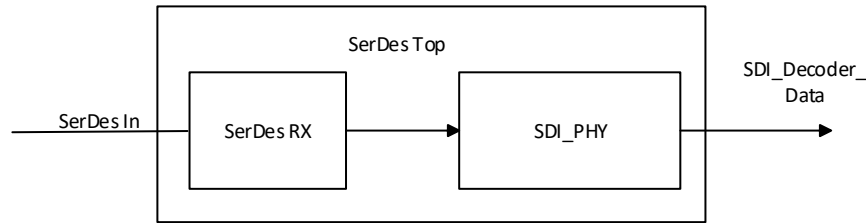
As shown above, SerDes Top TX consists of the following two modules:

- SDI PHY: Receives data from the SDI_Encoder.
- SerDes TX: Serializes the SDI encoded data for output.

3.2.2 RX

The structure diagram of Gowin SDI PHY IP RX is shown in Figure 3-3.

Figure 3-3 Structure Diagram of Gowin SDI PHY IP RX



As shown above, Gowin SDI PHY IP RX consists of the following two modules:

- SerDes RX: Receives serial data and converts it into parallel data for output.
- SDI PHY: Outputs the data to the SDI_Decoder.

3.2.3 SerDes Clock

SerDes transmit clock is generated by CPLL/QPLL. When configuring a lane, the user needs to configure the rate of the lane, the PLL (CPLL/QPLL) used, as well as the reference clock source and its frequency. Based on the above configuration, the IP configures SerDes PLL to generate a high-speed clock for data transmission. At the same time, SerDes divides the high-speed clock based on user configuration and outputs it as a fabric transmit clock.

The SerDes receive clock is recovered by CDR (Clock Data Recovery), and the CDR outputs the recovered serial data clock for the receive module. At the same time, SerDes divides the serial data clock according to the user configuration and outputs it as a fabric receive clock.

If the user configures the data rate to be 2.97Gbps, the parallel data width to be 20 bits, and Data Ratio to be 1:1, then the fabric transmit clock is $2.97\text{Gbps}/(20 \times 1) = 148.5\text{MHz}$.

If the user configures the data rate to be 2.97Gbps, the parallel data width to be 20 bits, and Data Ratio to be 1:2, then the fabric transmit clock is $2.97\text{Gbps}/(20 \times 2) = 74.25\text{MHz}$.

If the user configures the data rate to be 1.485Gbps, the parallel data width to be 20 bits, and Data Ratio to be 1:1, then the fabric transmit clock is $1.485\text{Gbps}/(20 \times 1) = 74.25\text{MHz}$.

3.2.4 SerDes Data

SerDes TX data transmission order: The least significant bit of txdata is transmitted first. SerDes RX data transmission order: The least significant bit of rxdata is received first.

3.3 Supported Format

Table 3-1 shows the formats supported by Gowin SDI PHY IP.

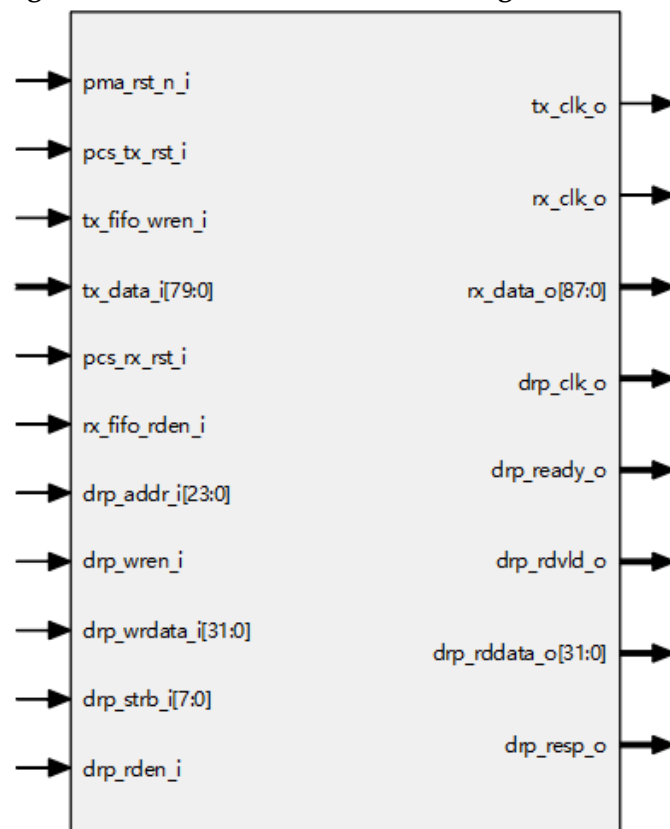
Table 3-1 Formats Supported by Gowin SDI PHY IP

Standard	HD-SDI and Level B DS					3G-SDI	
Hor Addr Pixel	1280	1280	1920	1920	1920	1920	1920
Ver Addr Line	720	720	1080	1080	1080	1080	1080
Hor Total Pixel	1650	1980	2200	2640	2750	2200	2640
Ver Total Line	750	750	1125	1125	1125	1125	1125
Scan Mode	Progressive	Progressive	Progressive	Progressive	Progressive	Progressive	Progressive
Frame Rate	60	50	30	25	24	60	50
Bit Per Word	20	20	20	20	20	20	20
Word Rate (Mhz)	74.25	74.25	74.25	74.25	74.25	148.5	148.5
Pixel Sample Rate (Mhz)	74.25	74.25	74.25	74.25	74.25	148.5	148.5
Structure	YC4:2:2	YC4:2:2	YC4:2:2	YC4:2:2	YC4:2:2	YC4:2:2	YC4:2:2
Pixel Depth	10	10	10	10	10	10	10

3.4 Port List

The IO port of Gowin SDI PHY IP is as shown in Figure 3-4.

Figure 3-4 Gowin SDI PHY IP Port Diagram



The IO ports vary slightly depending on the parameters. The details of IO port of Gowin SDI PHY IP are shown in Table 3-2.

Table 3-2 I/O List of Gowin SDI PHY IP

Signal Name	I/O	Data Width	Description
SDI_PHY_Top_pma_rst_n_i	I	1	The reset signal of SerDes PMA, active-low
SDI_PHY_TX			
SDI_PHY_Top_pcs_tx_rst_i	I	1	The TX reset signal of SerDes Pcs, active-high.
SDI_PHY_Top_tx_fifo_wren_i	I	1	Write enable of SDI_PHY
SDI_PHY_Top_tx_data_i	I	80	Input data of SDI_PHY TX
SDI_PHY_Top_tx_clk_o	O	1	The clock output of SDI_PHY TX Frequency = TX Line Rate/(TX Internal Data Width*N) TX Line Rate, Internal Data Width, and N(Tx External Data Ratio 1:N) are parameters configured in the IP.
SDI_PHY_RX			
SDI_PHY_Top_pcs_rx_rst_i	I	1	The RX reset signal of SerDes Pcs, active-high.
SDI_PHY_Top_rx_fifo_rden_i	I	1	Read enable of SDI_PHY
SDI_PHY_Top_rx_clk_o	O	1	Recovered Clock of SDI_PHY RX Frequency = RX Line Rate/(RX Internal Data Width*N) RX Line Rate, Internal Data Width, and N(Rx External Data Ratio 1:N) are parameters configured in the IP.
SDI_PHY_Top_rx_data_o	O	88	Output data of SDI_PHY RX
SDI_PHY_Top_drp_clk_o	O	1	DRP Port clock (connect according to the reference design; no user operation required)
SDI_PHY_Top_drp_wren_i	I	1	DRP Port write enable (connect according to the reference design; no user operation required)
SDI_PHY_Top_drp_addr_i	I	24	DRP Port configuration address (connect according to the reference design; no user operation required)
SDI_PHY_Top_drp_wrdata_i	I	32	DRP Port write data (connect according to the reference design; no user operation required)
SDI_PHY_Top_drp_rden_i	I	1	DRP Port read enable (connect according to the reference design; no user operation required)
SDI_PHY_Top_drp_rddata_o	O	32	DRP Port read data (connect according to the reference design; no user

Signal Name	I/O	Data Width	Description
			operation required)
SDI_PHY_Top_drp_rdvld_o	O	1	DRP Port read valid (connect according to the reference design; no user operation required)
SDI_PHY_Top_drp_ready_o	O	1	DRP Port read ready (connect according to the reference design; no user operation required)
SDI_PHY_Top_drp_strb_i	I	8	Write 0xff (connect according to the reference design; no user operation required)
SDI_PHY_Top_drp_resp_o	O	1	Reserved (connect according to the reference design; no user operation required)

3.5 Parameter Configuration

Table 3-3 Gowin SDI PHY IP Parameter

No.	Name	Range	Default	Description
PHY Configuration				
1	Quad Selection	Q0/Q1	Q0	SerDes Quad Selection
2	Channel Selection	Lane0 Lane1 Lane2 Lane3	Lane0	SerDes Lane Selection
3	Loopback Mode	OFF LB_NES LB_FES LB_ENC	OFF	OFF: No Loopback, normal operating mode LB_NES: Loopback Near-End Side LB_FES: Loopback Far-End Side LB_ENC: Loopback Encoder
4	Line Rate	1.485/2.97 Gbps	1.485	Configure transmit data rate
4	TX Internal Data Width	10/20	20	TX internal data width
5	TX External Data Ratio	1:1,1:2,1:4	1:1	TX clock ratio
6	SerDes internal data bit width	10/20	20	RX internal data width
7	RX External Data Ratio	1:1,1:2,1:4	1:1	RX clock ratio
8	TX PN Invert	Enable/Disable	Disable	TX PN inversion
9	RX PN Invert	Enable/Disable	Disable	RX PN inversion
11	Reference Clock Source	Q0 REFCLK0 Q0 REFCLK1	Q0 REFCLK0	Reference clock source selection

No.	Name	Range	Default	Description
PHY Configuration				
		Q1 REFCLK0 Q1 REFCLK1		
12	Reference Clock Frequency	50-500MHz	148.5	Configure reference clock source
13	PLL Selection	CPLL QPLL0 QPLL1	CPLL	Select PLL
14	DRP Port	Enable/Disable	Disable	Dynamically adjust SerDes parameters
AFE (Analog Front End)				
15	Differential Swing	180mV~900mV	900mV	Configure the swing of the TX differential signal Vdiffpp, Vdiffpp=2xVdiff
16	FFE Mode	Auto/Manual	Auto	Configure TX FFE mode Auto: Manual: Manual mode
17	Cm	0~19	0	Transmit FFE pre-cursor
18	C0	21~40	40	Transmit FFE main-cursor
19	C1	0~19	0	Transmit FFE post-cursor
20	SD Threshold	25mV~200mV	100mV	SD threshold for RX differential signal

3.6 Timing Description

This section describes the timing of Gowin SDI PHY IP.

The input timing diagram of Gowin SDI PHY TX video interface is as shown in Figure 3-5. The output timing diagram of Gowin SDI PHY RX video interface is as shown in Figure 3-6. The TX outputs a clock to Gowin SDI Encoder IP, which then outputs data to the PHY IP. The RX outputs both clock and data to Gowin SDI Decoder IP for decoding.

Figure 3-5 Timing Diagram of Video Input Interface

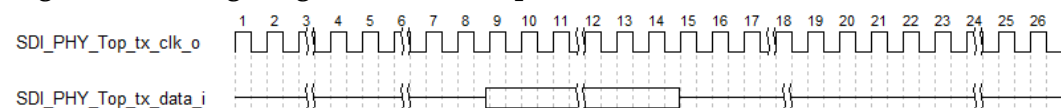
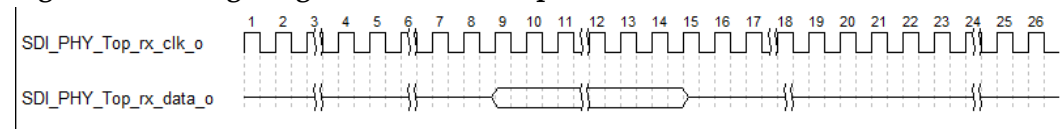


Figure 3-6 Timing Diagram of Video Output Interface



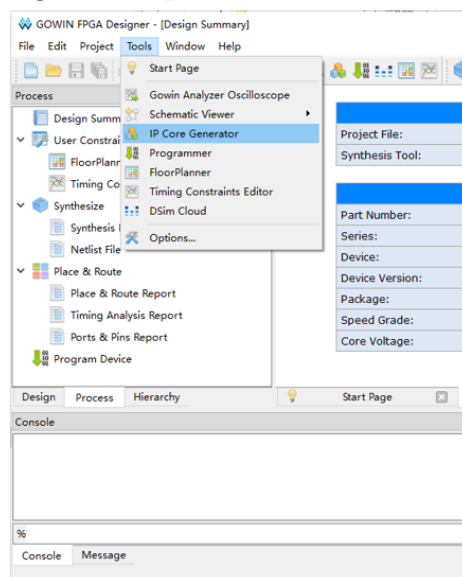
4 Interface Configuration

You can use IP core generator tool in Gowin Software to call and configure Gowin SDI PHY IP.

1. Open IP Core Generator

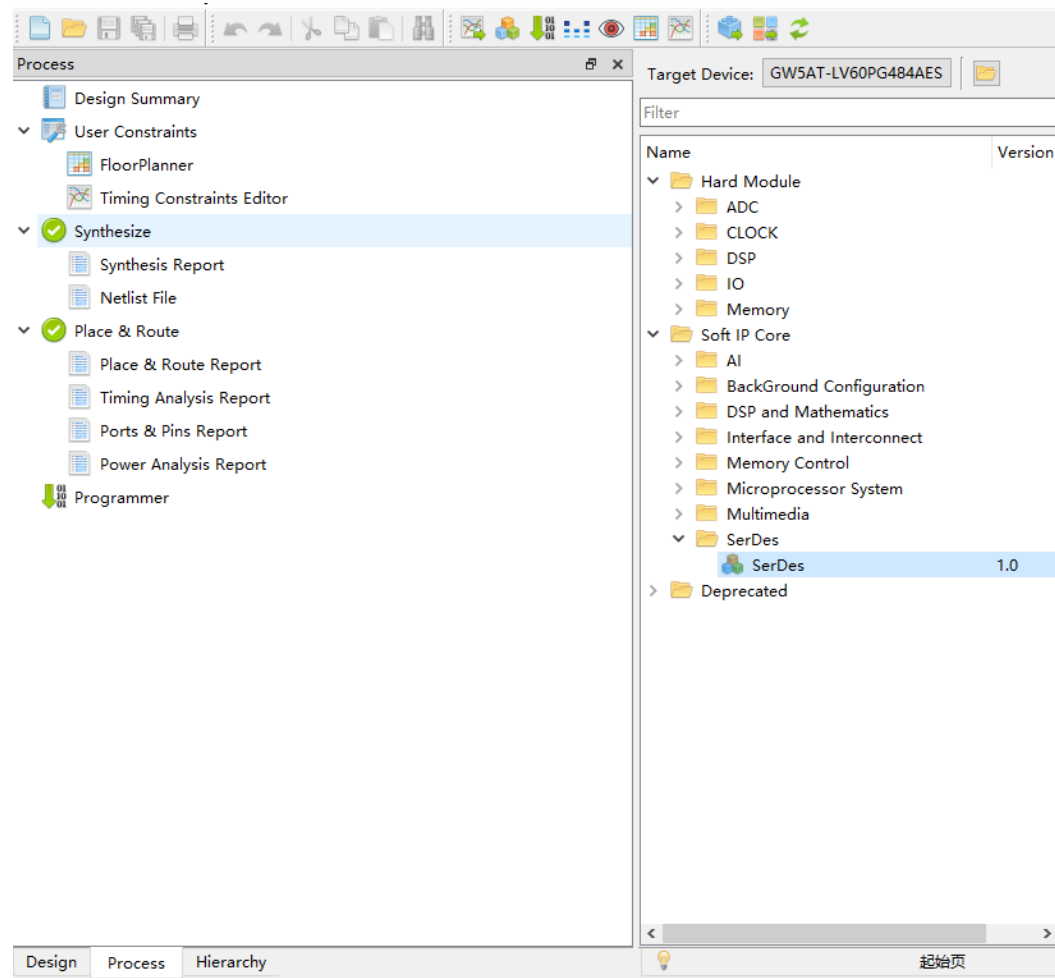
After creating the project, click the "Tools" tab in the upper left, click "IP Core Generator" from the drop-down list to open Gowin IP Core Generator, as shown in Figure 4-1.

Figure 4-1 Open IP Core Generator



2. Open SerDes IP Configuration Interface

Double click "SerDes" to open the SerDes IP core configuration interface, as shown in Figure 4-2.

Figure 4-2 Open SerDes IP Configuration Interface

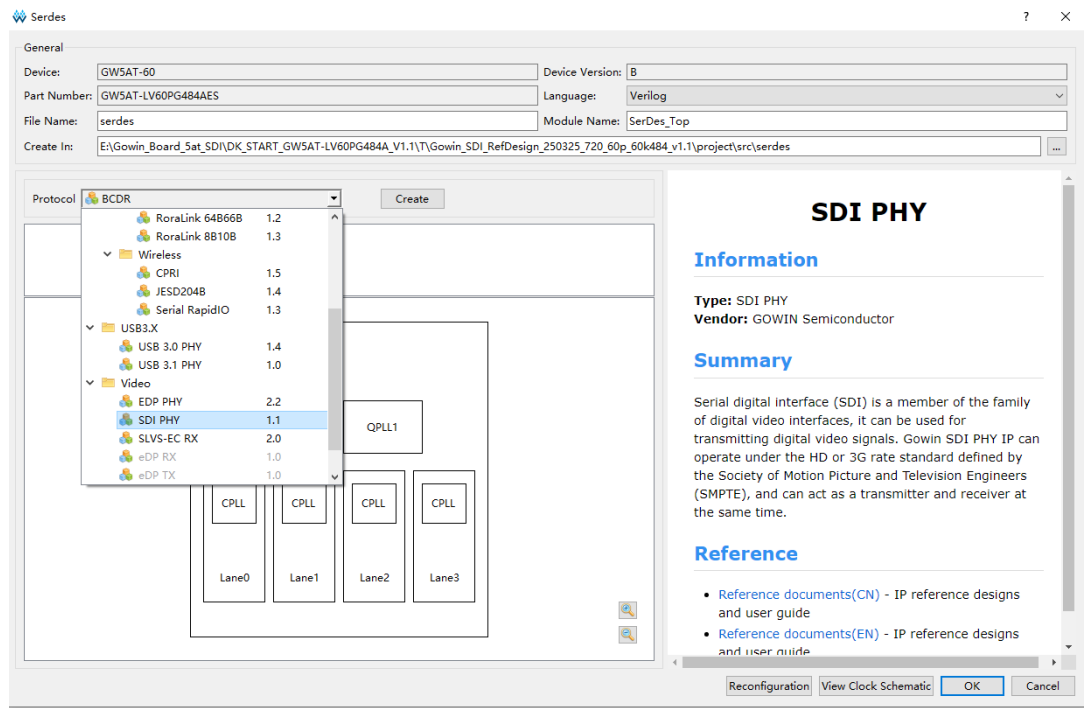
3. Open SDI configuration interface.

First configure "General" tab in the SerDes IP interface.

- Device, Device Version, Part Number: Part number settings, determined by the current project, and the user can not set it.
- Language: Supports Verilog and VHDL; choose the language as requirements, and the default is Verilog.
- File Name, Module Name, Create In: Displays SerDes file name, module name and the generated file path.

Then select the "SDI" option in the "Protocol" option of the SerDes IP configuration interface and click the "Create" button, as shown in Figure 4-3.

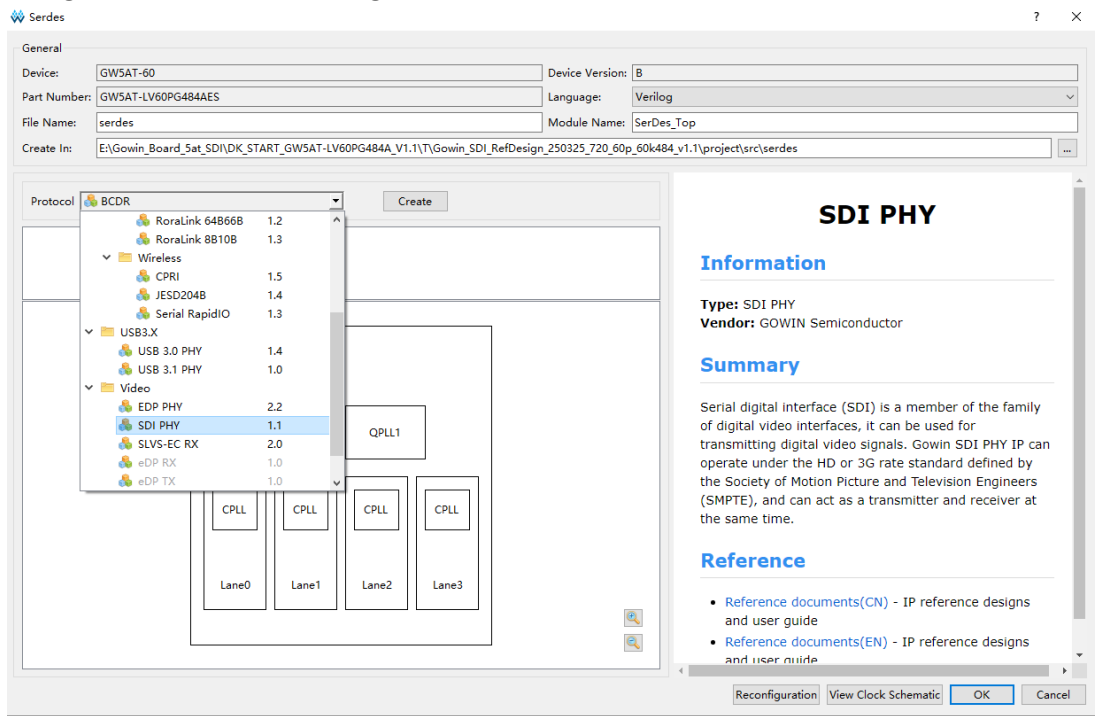
Figure 4-3 Open SDI PHY Configuration Interface



4. SDI PHY Configuration Interface

The configuration interface of SDI PHY IP is shown in Figure 4-4. The port diagram is on the left, and the parameter configuration options are on the right.

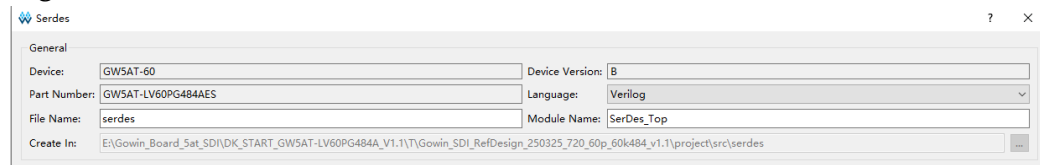
Figure 4-4 SDI PHY Configuration Interface



Configure general information as shown in Figure 4-5. You can see the project basic information in the upper section of the configuration interface.

The "Module Name" displays the top-level module name of the generated project, and the default is "SDI_PHY_Top"; you can modify the name. The "File Name" displays the folder generated by the IP, which contains the files required by SDI PHY IP, and the default is "sdi_phy", and you can modify the path.

Figure 4-5 General Tab



The screenshot shows the 'Serdes' configuration window with the 'General' tab selected. The fields are as follows:

Field	Value
Device	GW5AT-60
Device Version	B
Part Number	GW5AT-LV60PG484AES
Language	Verilog
File Name	serdes
Module Name	SerDes_Top
Create In	E:\Gowin_Board_Sat_SDI\DK_START_GW5AT-LV60PG484A_V1.1\T\Gowin_SDI_RefDesign_250325_720_60p_60k484_v1.1\project\src\serdes

Configure "PHY Configuration" tab as shown in Figure 4-6. There is a limitation between the line rate and the reference clock; make sure that the reference clock can generate the above line rate, which can also be detected through clicking "Calculate" button.

Figure 4-6 PHY Configuration Tab

General

Device: GW5AT-60 Device Version: B

Part Number: GW5AT-LV60PG484AES Language: Verilog

File Name: sdi_phy Module Name: SDI_PHY_Top

Create In: _SDI_RefDesign_250325_720_60p_60k484_v1.1\project\src\serdes\sdi_phy

PHY Configuration **AFE**

Quad Selection: Q0

Channel Selection: Lane2

Loopback Mode: OFF

Line Rate: 1.485 Gbps

TX Data Width

TX Internal Data Width: 20

TX External Data Ratio: 1:1

RX Data Width

RX Internal Data Width: 20

RX External Data Ratio: 1:1

☐ TX PN Invert ☐ RX PN Invert

Refclk Selection

Reference Clock Source: Q0 REFCLK0

Reference Clock Frequency: 148.500 MHz

PLL Selection: QPLL1

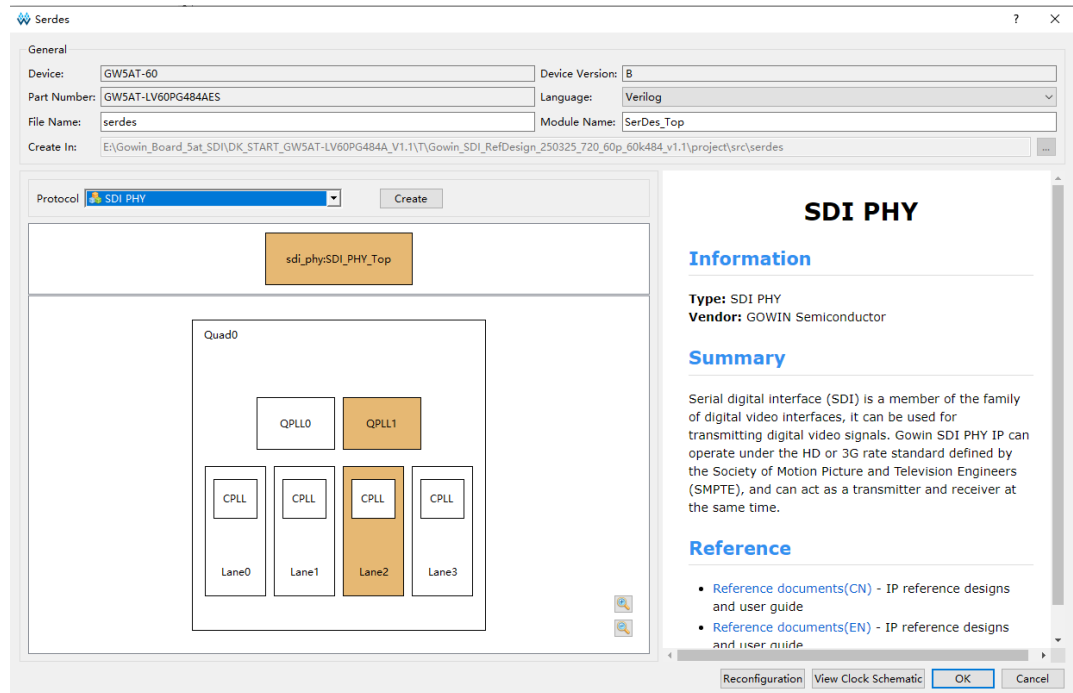
☒ DRP Port

Calculate

OK Cancel

5. IP Generation

After completing SDI PHY IP configuration, click “OK” button at the bottom right corner of the interface to generate files of the SDI PHY IP, and return to the SerDes IP configuration interface, and then the SerDes IP configuration interface displays the current generated IP and the corresponding Quad, PLL, and Lane usage, as shown in Figure 4-7.

Figure 4-7 SDI PHY IP in SerDes IP Configuration Interface

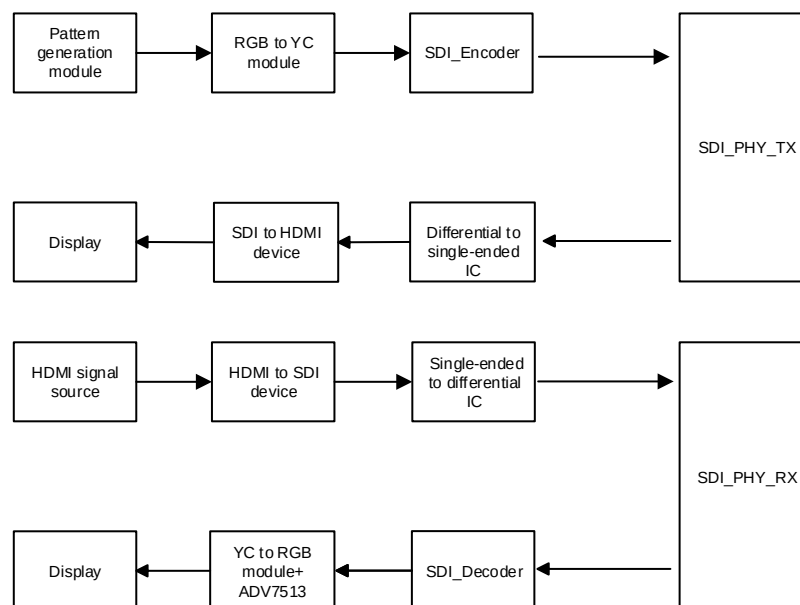
Then, click "OK" button at the bottom right corner of the interface to generate SerDes IP files and complete the whole SDI PHY IP generation.

5 Reference Design

This chapter is intended to introduce the example and using of Gowin SDI PHY IP [reference design](#). Please see the SDI PHY IP Reference Design for details at Gowinsemi website.

This reference design takes DK_START_GW5AT-LV60PG484A_V1.1 development board as an example. For more information about DK_START_GW5AT-LV60PG484A_V1.1 development board, please refer to Gowinsemi website. The block diagram of reference design is shown in Figure 5-1.

Figure 5-1 Block Diagram of Reference Design



The reference design adopts the approach that TX and RX are verified independently of each other. TX generates a test pattern video signal through the pattern generation module and outputs it to SDI_PHY_TX, then SerDes differentially outputs it to a differential-to-single-ended IC, further to the SDI physical interface, then outputs it to an SDI-to-HDMI device, and finally to the display. SDI_PHY_RX receives the video signal from the signal source through a single-ended-to-differential IC, then outputs it to ADV7513, and ultimately to the display.

6 File Delivery

The delivery files for Gowin SDI PHY IP includes the documents, the design source code, and the reference design.

6.1 Documentation

Table 6-1 Document List

Name	Description
IPUG1206, Gowin SDI PHY IP User Guide	Gowin SDI PHY IP User Guide, namely this one

6.2 Design Source Code (Encryption)

The encrypted code file contains the SDI PHY IP RTL encrypted code which is used for GUI in order to cooperate with Gowin Software to generate the IP core required by users.

Table 6-2 File List of Gowin SDI PHY IP

Name	Description
sdi_phy.v	SDI PHY IP File, encrypted
SerDes.v	The top-level file of SerDes-related IP, which provides users with interface information.

6.3 Reference Design

The RefDesign folder contains the netlist files, user reference designs, constraints files, top-level files, and project files for Gowin SDI PHY IP, Gowin SDI Encoder IP, and Gowin SDI Decoder IP.

Table 6-3 Gowin SDI PHY IP RefDesign Folder Content List

Name	Description
video_top.v	The top module of reference design
testpattern.v	Test pattern generation module
dk_video.cst	Project physical constraints file
dk_video.sdc	Project timing constraints file
key_debounceN.v	Key debouncing
adv7513_iic_init.v	adv7513 configuration file
yc_to_rgb	yc_to_rgb folder

Name	Description
rgb_to_yc	rgb_to_yc folder
i2c_master	i2c_master folder, encrypted.
sdi_decoder	sdi_decoder folder, encrypted.
sdi_encoder	sdi_encoder folder, encrypted.
serdes	SerDes project folder, encrypted.
gowin_pll	gowin_pll folder
sdi_audio_buffer_pro	sdi_audio_buffer_pro folder
i2s_interface	i2s_interface folder

