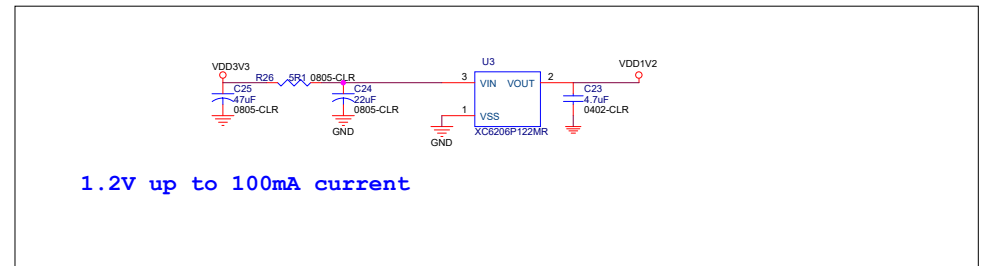
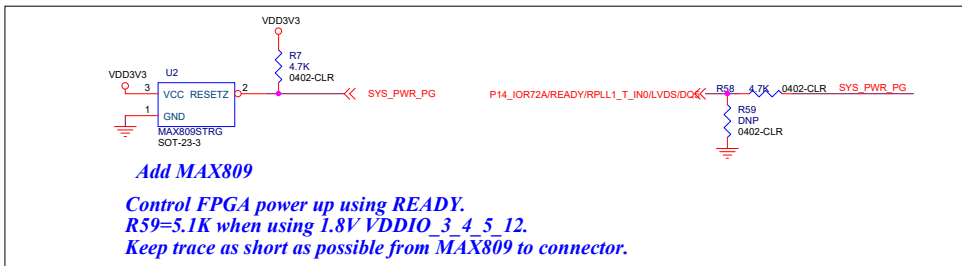
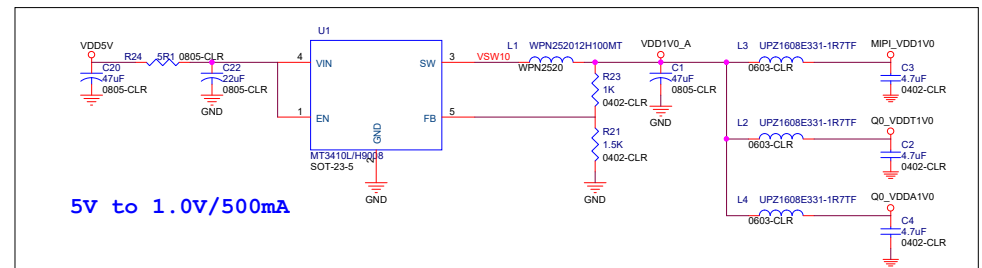
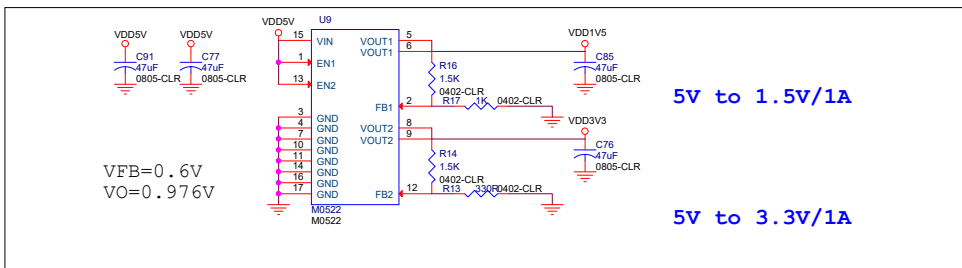
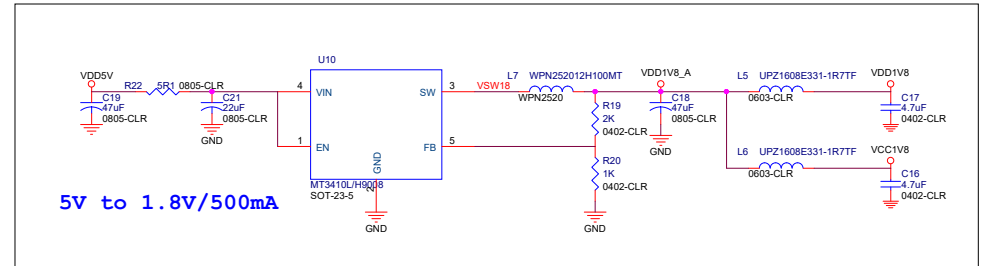
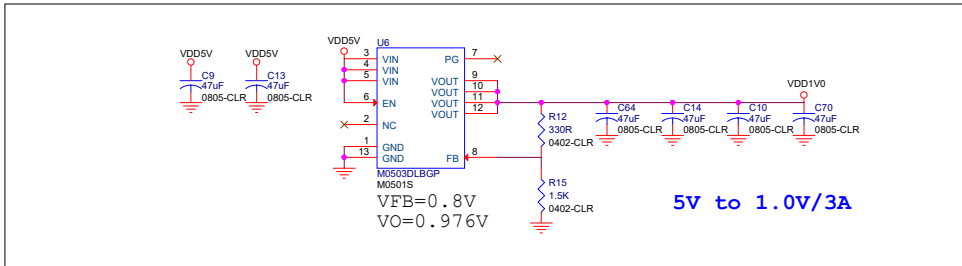


V2

1. Added 1.2V for Bank 1 & 2.
2. Fix DDR CK P/N Swap issue. The clock pair on DDR3 chip is swapped accidentally.
3. Add 3.3V LED.
4. Removed 809 connection to RECONFIG. Connects to READY.
5. Changed flash to SO-8 150mil part.

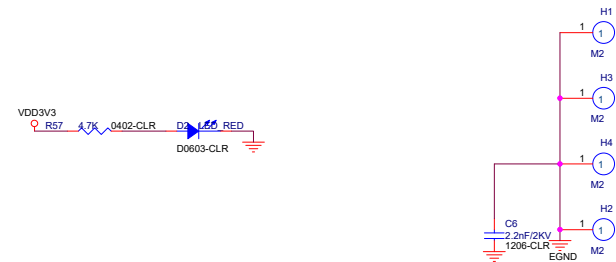
SOM POWER



Power Tree

```

5V -----> 3.3V 1A DCDC (Shared M0522) (IO) --> 1.2V 200mA LDO (XC6206) (MIPI LP)
|
|--> 1.5V 1A DCDC (Shared M0522) (DDR3) --> 0.75V VTT (SGM2054)
|
|--> 1.0V 3A DCDC (M0503) (Core)
|
|--> 1.8V 500mA DCDC (MT3410L Low Ripple) (SERDES / MIPI)
|
|--> 1.0V 500mA DCDC (MT3410L Low Ripple) (SERDES)
    
```



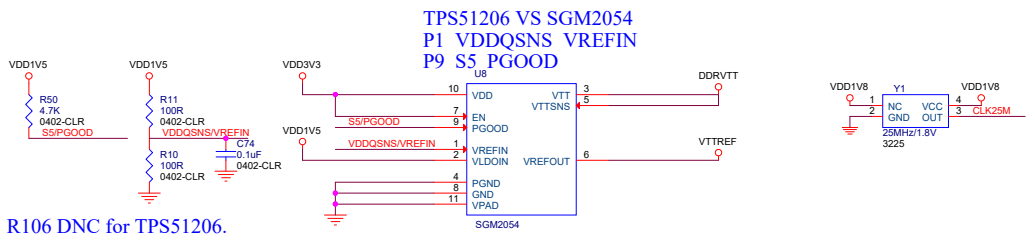
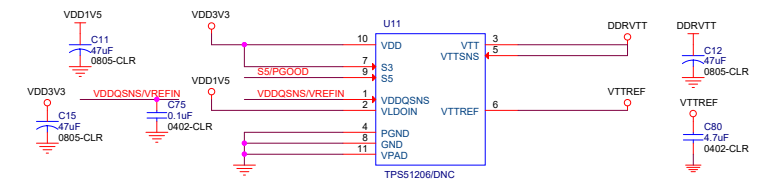
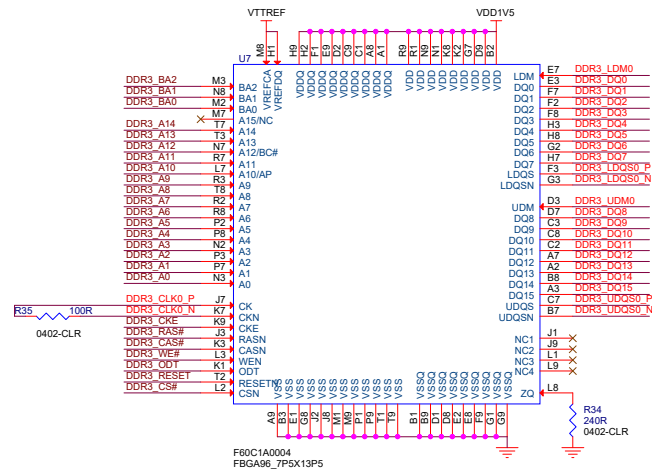
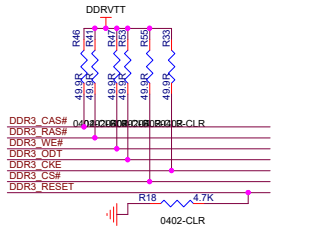
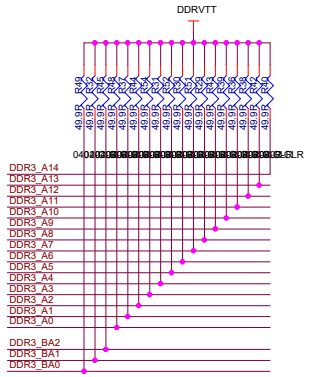
DDR3

Bank 8		
DDR3 A6	L9	IOB75A/LVDS/DQ8
DDR3 A3	K8	IOB75B/LVDS/DQ8
DDR3 A0	R10	IOB77A/LVDS/DQ8
DDR3 A5	P11	IOB77B/LVDS/DQ8
DDR3 A1	N11	IOB79A/LVDS/DQ8
DDR3 B2	R12	IOB79B/LVDS/DQ8
DDR3 A3	M10	IOB81A/GCLKT_11/LVDS/DQ8
DDR3 A4	N10	IOB81B/GCLKT_11/LVDS/DQ8
DDR3 A7	R13	IOB85A/LVDS/DQS8
DDR3 A2	R12	IOB85B/LVDS/DQS8
DDR3 A5	M11	IOB87A/GCLKT_10/LVDS/DQ8
DDR3 A12	L10	IOB87B/GCLKT_10/LVDS/DQ8
DDR3 A10	K10	IOB89A/LVDS/DQ8
DDR3 A6	R14	IOB89B/LVDS/DQ8
DDR3 A7	P13	IOB91A/LVDS/DQ8
		IOB91B/LVDS/DQ8

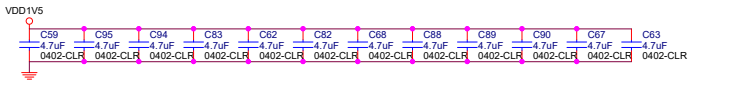
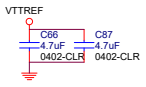
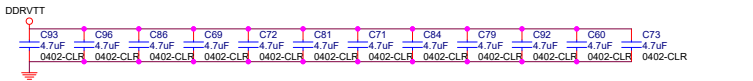
GWSAT-LV60UG225
BGA225-0P8-13X13

Bank 9		
DDR3 DQ11	L1	IOB1A/LVDS/DQ12
DDR3 UDM0	L2	IOB1B/LVDS/DQ12
DDR3 DQ13	M3	IOB3A/BPLL0_T_IN1/LVDS/DQ12
DDR3 DQ9	M1	IOB3B/BPLL0_C_IN1/LVDS/DQ12
DDR3 CS#	N2	IOB5A/BPLL0_T_IN2/LVDS/DQ12
DDR3 OD1	N1	IOB7A/LVDS/DQ12
DDR3 WE#	P1	IOB7B/LVDS/DQ12
DDR3 CAS#	R2	IOB7C/LVDS/DQ12
DDR3 RAS#	P2	IOB9B/LVDS/DQ12
DDR3 UDO50 P	R3	IOB12A/LVDS/DQS12
DDR3 UDO50 N	P3	IOB12B/LVDS/DQS12
DDR3 DQ12	N4	IOB12C/LVDS/DQS12
DDR3 DQ8	M4	IOB14A/LVDS/DQ12
DDR3 DQ14	P5	IOB14B/LVDS/DQ12
DDR3 DQ10	N5	IOB16A/LVDS/DQ12
DDR3 DQ2	M5	IOB16B/LVDS/DQ12
DDR3 DQ4	L5	IOB18A/GCLKT_12/LVDS/DQ11
DDR3 DQ0	R4	IOB18B/GCLKT_12/LVDS/DQ11
DDR3 LDM0	R5	IOB20A/LVDS/DQ11
DDR3 DQ3	R6	IOB20B/LVDS/DQ11
DDR3 DQ0	R7	IOB22A/LVDS/DQ11
DDR3 DQ6	N6	IOB22B/LVDS/DQ11
DDR3 DQ5	M6	IOB24A/LVDS/DQ11
DDR3 LDQ50 P	R8	IOB24B/LVDS/DQ11
DDR3 LDQ50 N	R9	IOB25A/LVDS/DQS11
DDR3 DQ7	P7	IOB25B/LVDS/DQS11
DDR3 BA1	N7	IOB29A/LVDS/DQ11
DDR3 CLK0 P	N8	IOB29B/LVDS/DQ11
DDR3 CLK0 N	M8	IOB31A/GCLKT_14/LVDS/DQ11
DDR3 A13	P9	IOB31B/GCLKT_14/LVDS/DQ11
DDR3 RESET	N9	IOB33A/GCLKT_15/LVDS/DQ11
DDR3 A1	L6	IOB33B/GCLKT_15/LVDS/DQ11
DDR3 A11	L7	IOB35A/LVDS/DQ10
DDR3 A9	M9	IOB35B/LVDS/DQ11
DDR3 A8	L8	IOB38A/GCLKT_13/LVDS/DQ10
DDR3 A14		IOB38B/GCLKT_13/LVDS/DQ10

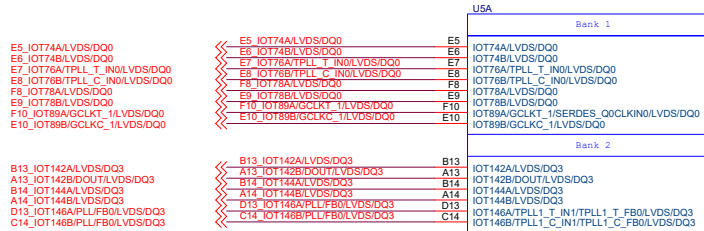
GWSAT-LV60UG225
BGA225-0P8-13X13



R106 DNC for TPS51206.



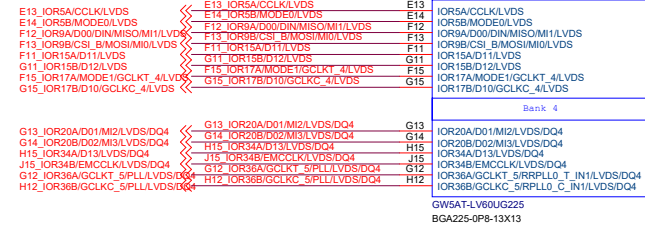
FPGA IO



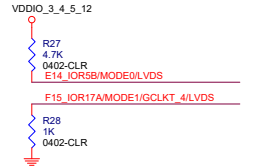
E5/E6/E7/E8/F8/E9/F10/E10 BANK1
B13/A13/B14/A14/D13/C14 BANK2

E13/E14/F12/F13/F11/G11/F15/G15 BANK3

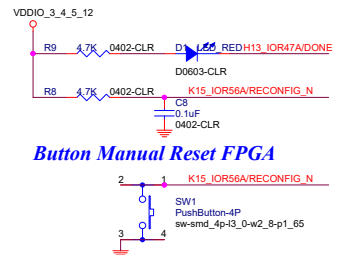
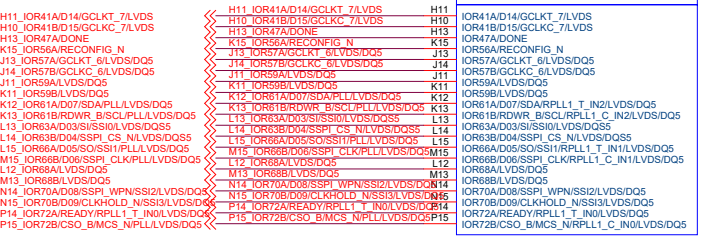
G13/G14/H15/J15/G12/H12 BANK4



Mode[1:0]=2'b01

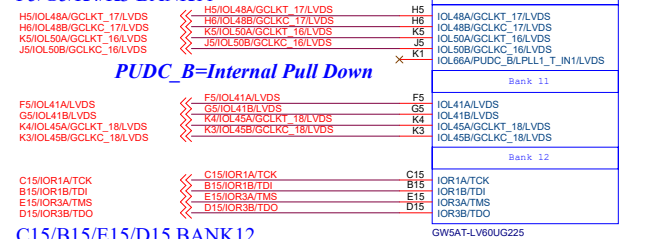


DONE/RECONFIG_N=Internal Pull Up



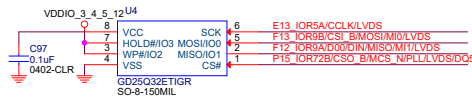
H5/H6/K5/J5 BANK10

F5/G5/K4/K3 BANK11



PUDC_B=Internal Pull Down

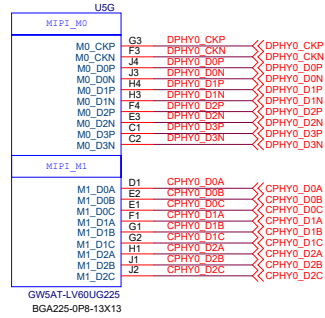
Dual SPI mode only.



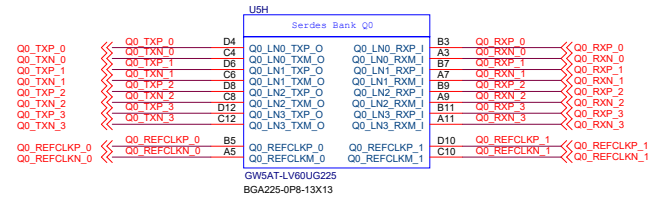
When 1.8V selected, SPI flash must be changed to 1.8V parts.

MIPI & SERDES

DPHY & CPHY

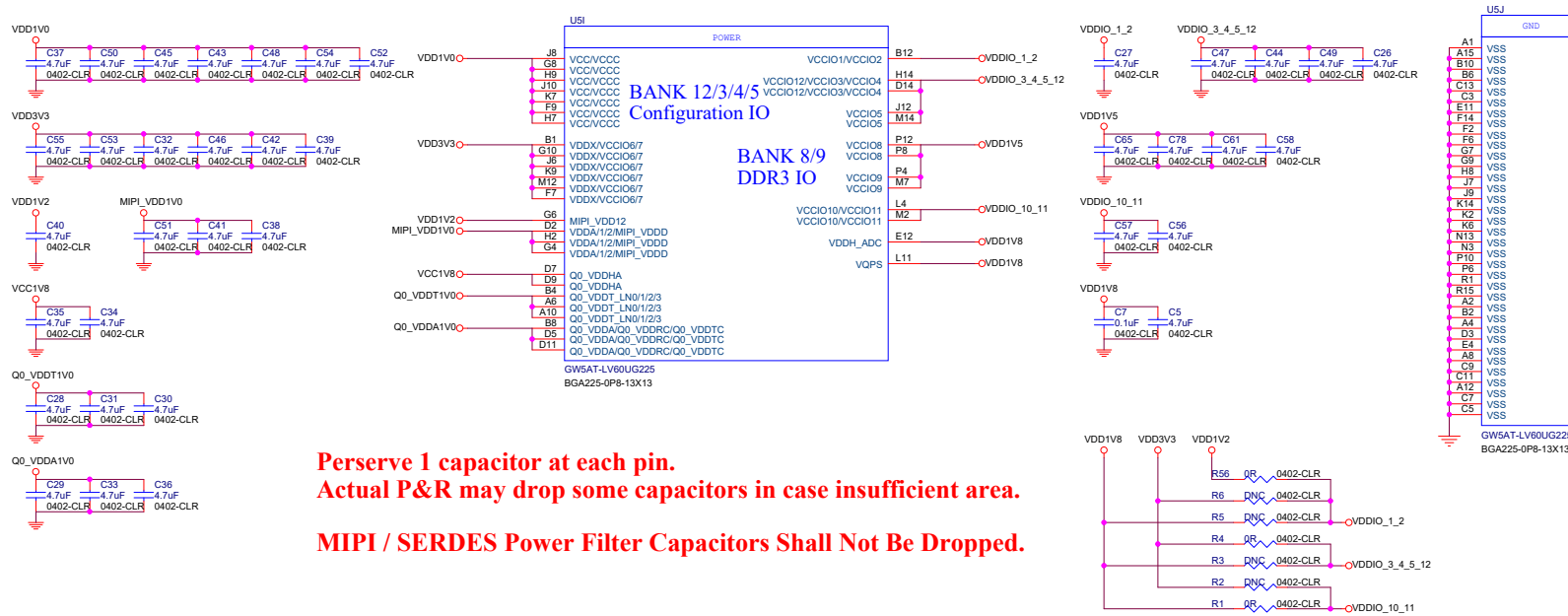


SERDES



Capacitors must be placed at bottom board.

FPGA Power

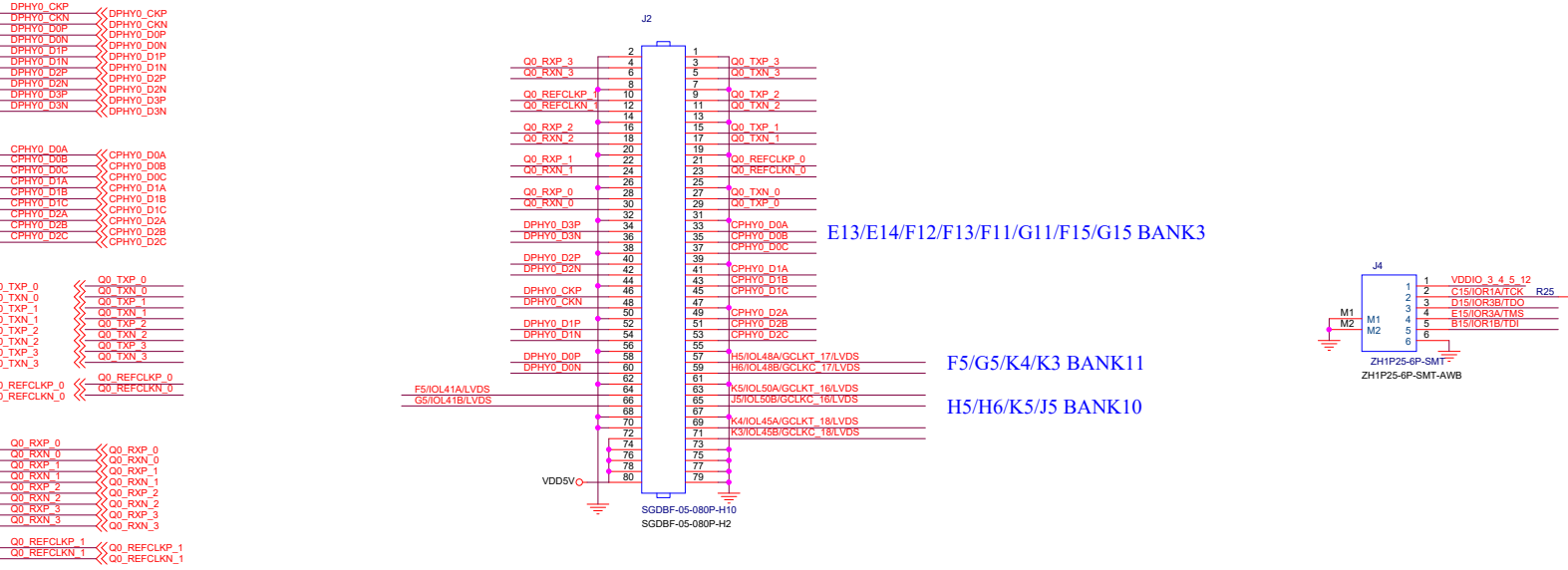
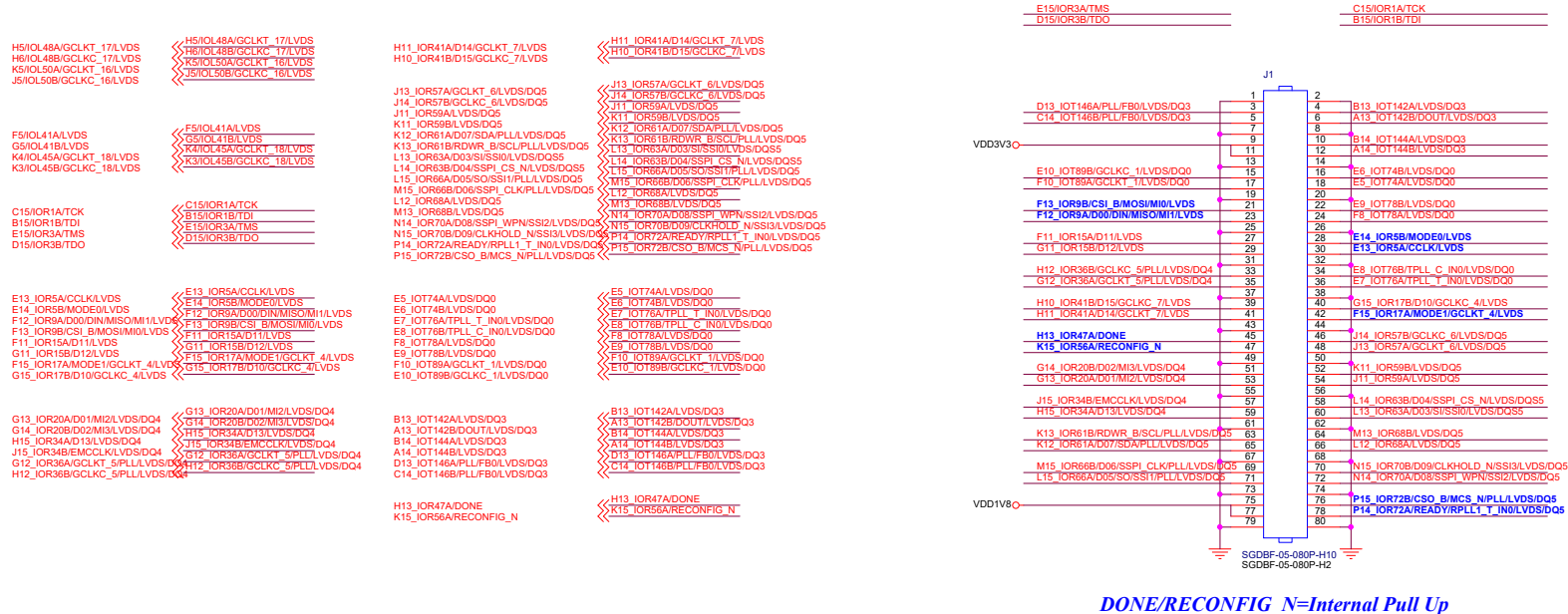


**Perserve 1 capacitor at each pin.
Actual P&R may drop some capacitors in case insufficient area.**

MIPI / SERDES Power Filter Capacitors Shall Not Be Dropped.

Bank 1 & 2: 1.2V By Default.
Bank 10 & 11: 1.8V By Default.
Bank 3 & 4 & 5 & 12: 3.3V By Default.

Interface



Removed C15/B15/E15/D15 BANK12 (JTAG)

B13/A13/B14/A14/D13/C14 BANK2

E5/E6/E7/E8/F8/E9/F10/E10 BANK1

E13/E14/F12/F13/F11/G11/F15/G15 BANK3

G13/G14/H15/J15/G12/H12 BANK4

E13/E14/F12/F13/F11/G11/F15/G15 BANK3

F5/G5/K4/K3 BANK11

H5/H6/K5/J5 BANK10

DONE/RECONFIG_N=Internal Pull Up

1. Restricted usage on E14/F15. MODE0 must be pulled high, F15 must be pulled low. Incorrect states are not allowed.
2. Configuration Flash Pins E13, F12, F13, P15 are not recommended to be used.
3. P14 may be used without restriction.