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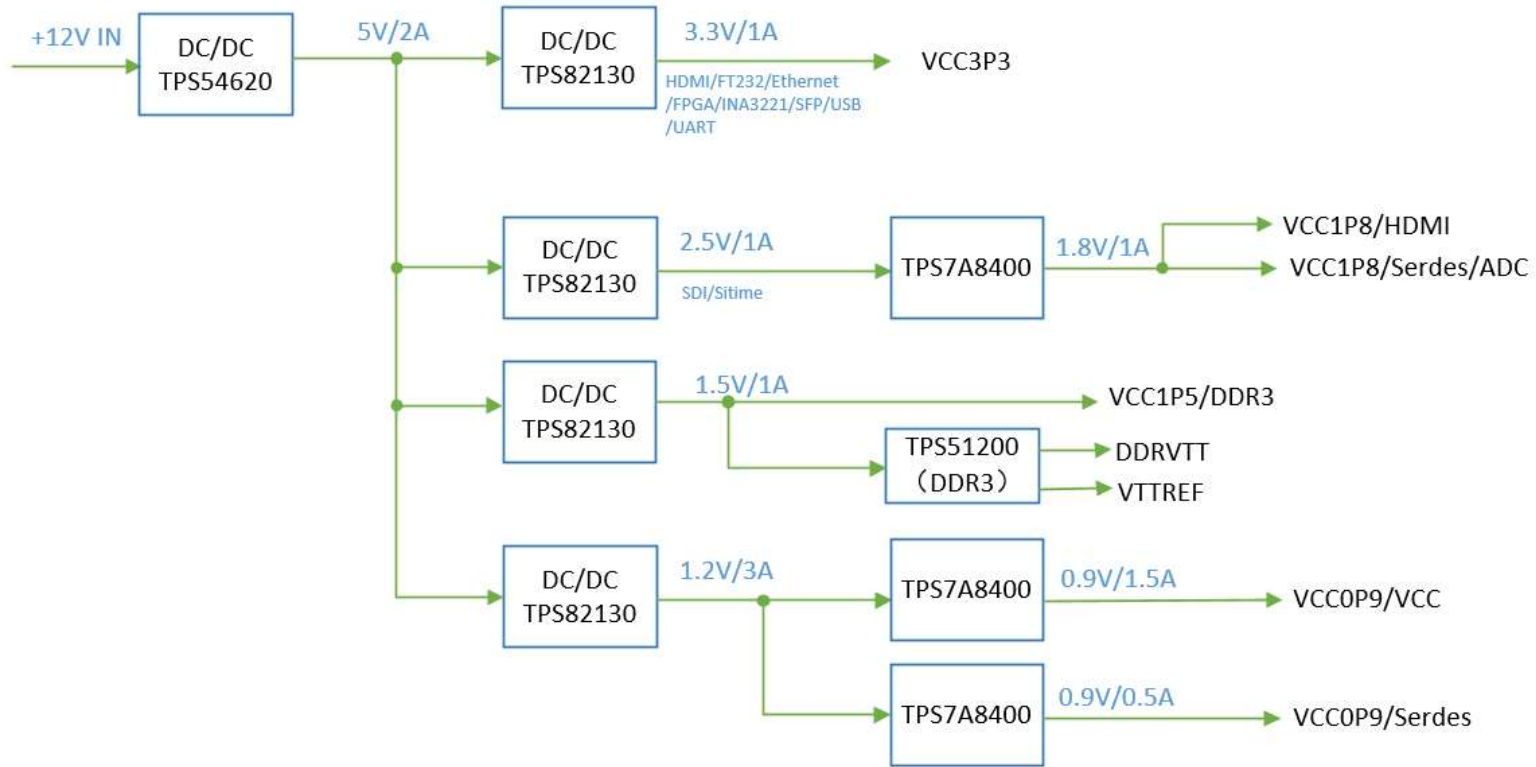
SCHEMATIC	CONTENT	PAGE
COVER PAGE	COVER PAGE	01
DIAGRAM	PCB DIAGRAM	02
POWER	VCC5P0, VCC3P3, VCC2P5, VCC1P8, VCC1P2, VCC1P5, VCC0P9	03~05
FPGA	FPGA	06~08
SFP	2*SFP	09
HDMI	HDMI-RX, HDMI-TX	10
SDI	SDI-IN, SDI-OUT	11
ETHERNET	2*ETHERNET PHY	12
DDR3	DDR3	13
OTHERS	MIPI, LVDS, USB-JTAG, UART	14

# PCB DIAGRAM



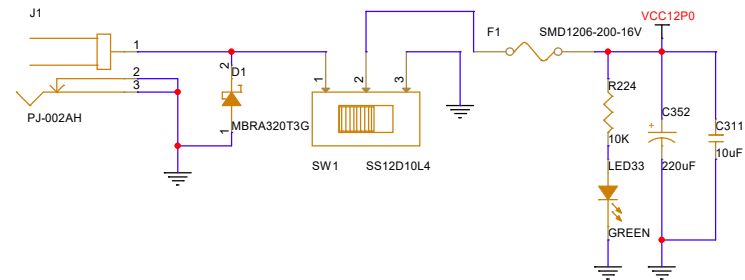
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DK_START_GW5AT-LV60PG484A_V1.1		
Size	Document Number	Rev
A3	DIAGRAM	V1.1
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# POWER TREE

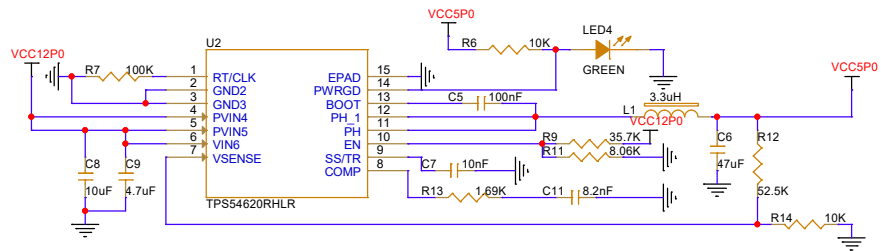


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Size	Document Number	Rev
A3	POWER TREE	V1.1
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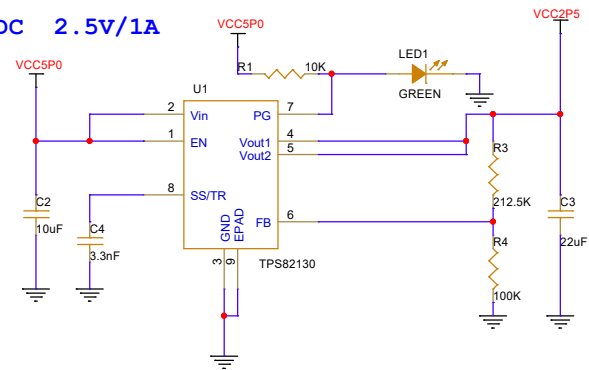
12V INPUT



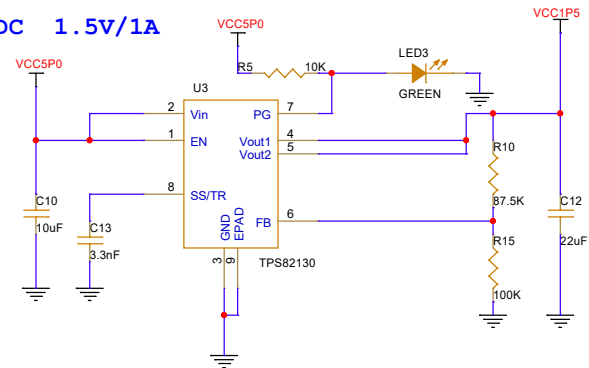
DC/DC 5V/2A



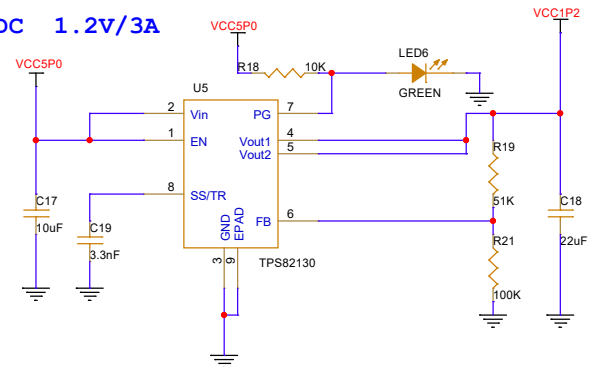
DC/DC 2.5V/1A



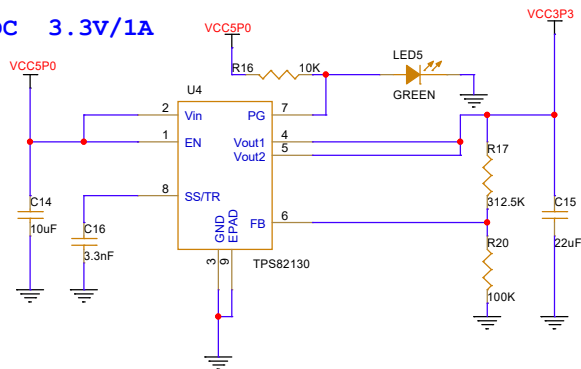
DC/DC 1.5V/1A



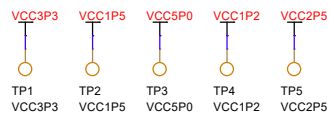
DC/DC 1.2V/3A



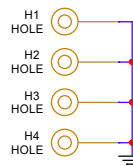
DC/DC 3.3V/1A



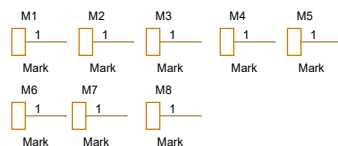
Power Test Hole



Mounting Hole

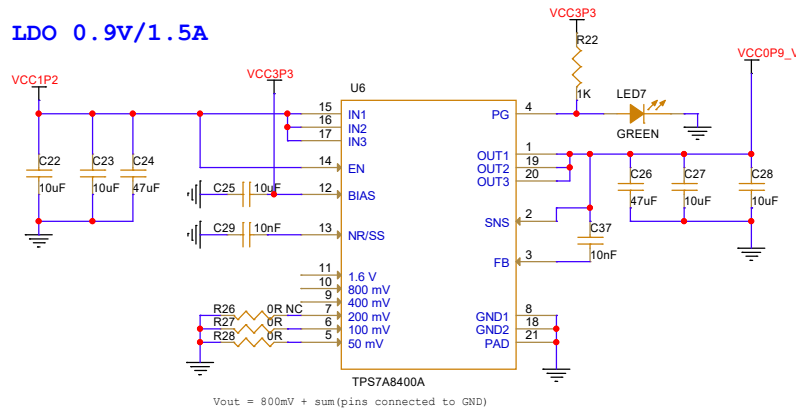


Mark

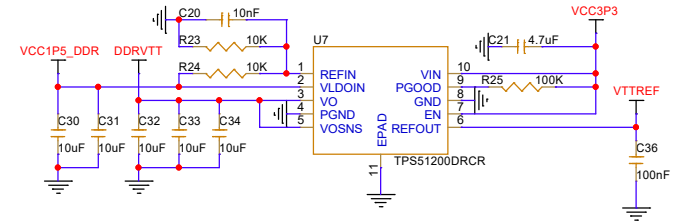


File		
DK_START_GW5AT-LV60PG484A_V1.1		
Size	Document Number	Rev
A3	POWER I	V1.1
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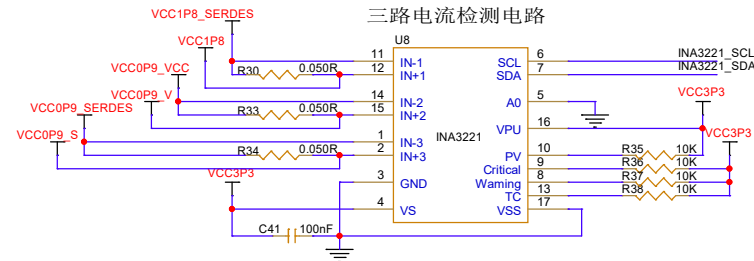
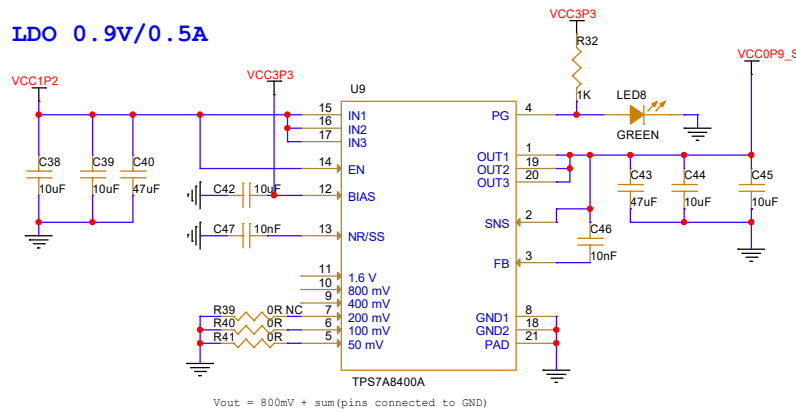
### LDO 0.9V/1.5A



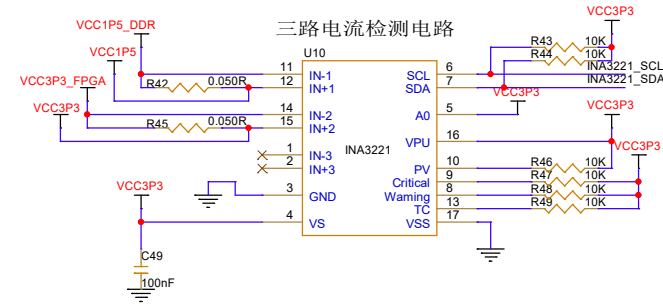
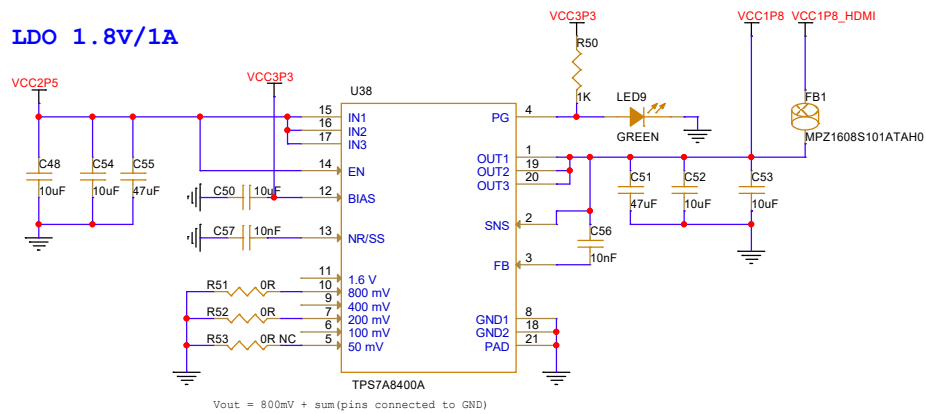
### DDR Power For VTT/VREF



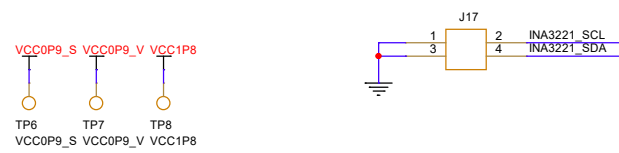
### LDO 0.9V/0.5A



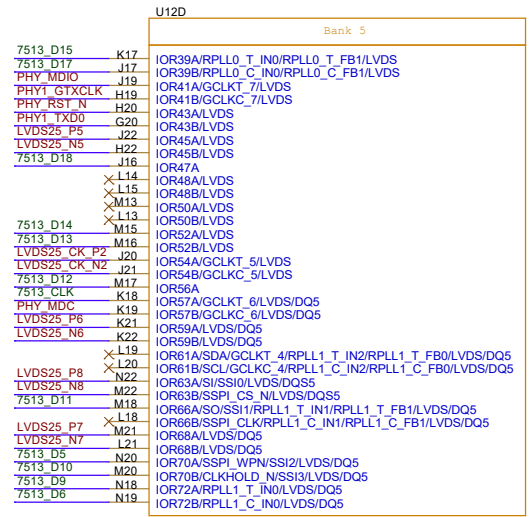
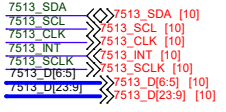
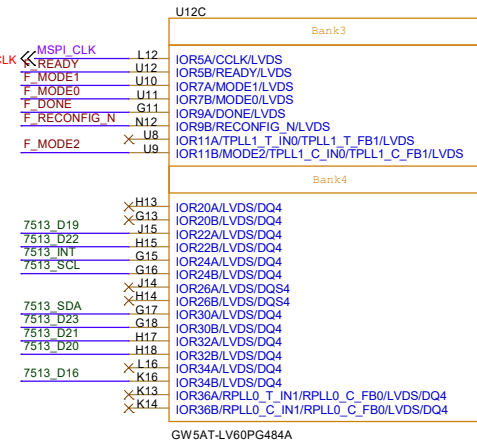
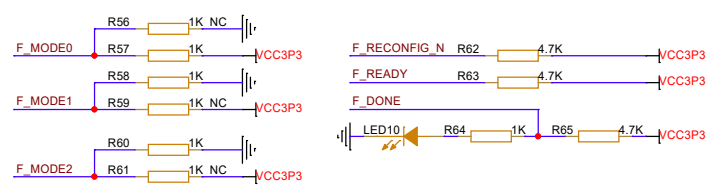
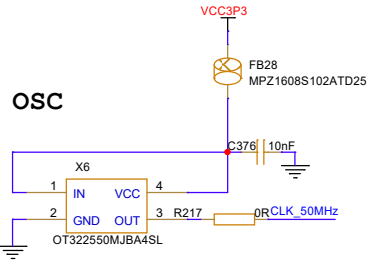
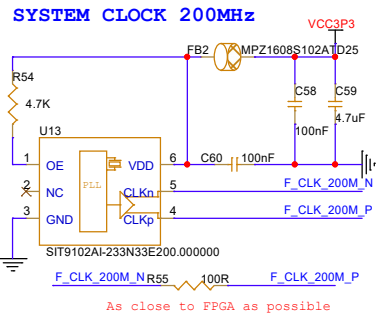
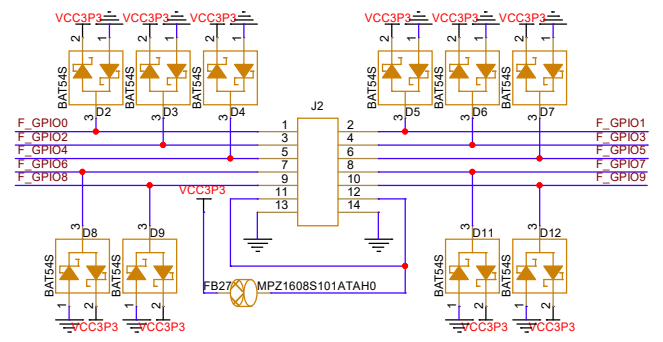
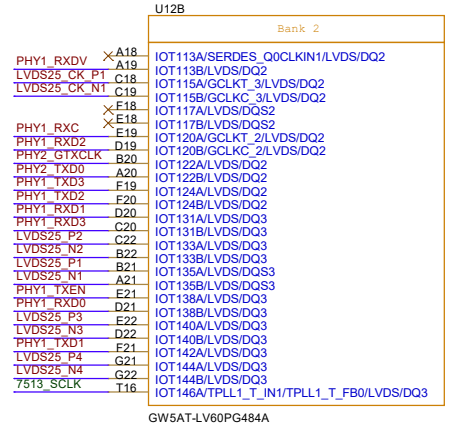
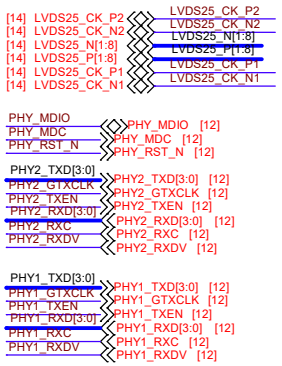
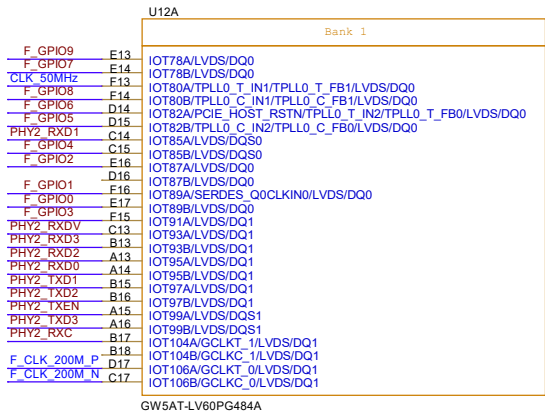
### LDO 1.8V/1A

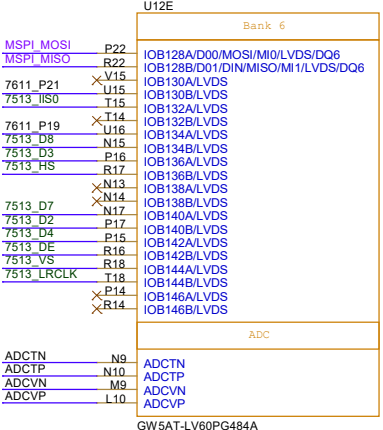
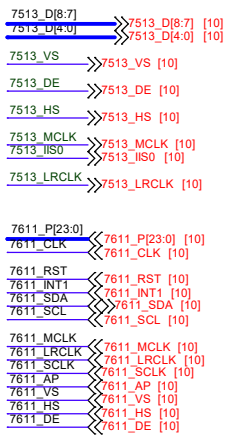


### Power Test Hole

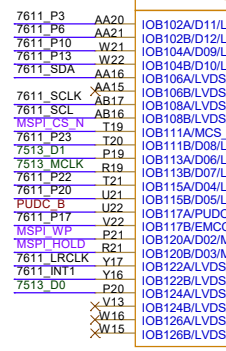


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Size	Document Number	Rev
A3	POWER II	V1.1
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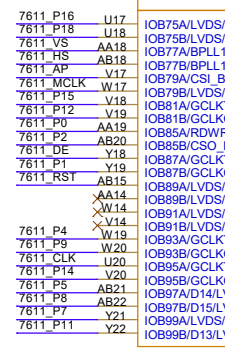




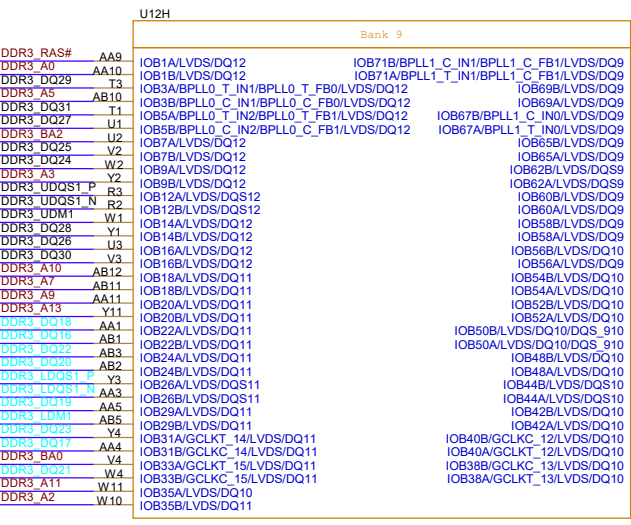
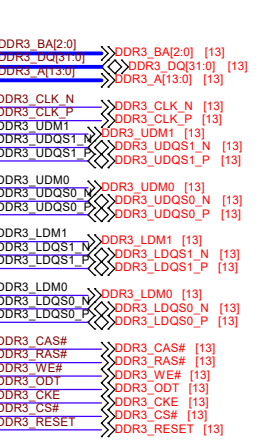
GW5AT-LV60PG484A



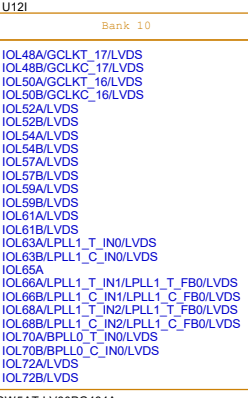
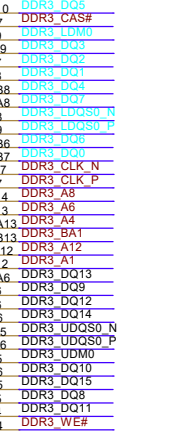
GW5AT-LV60PG484A



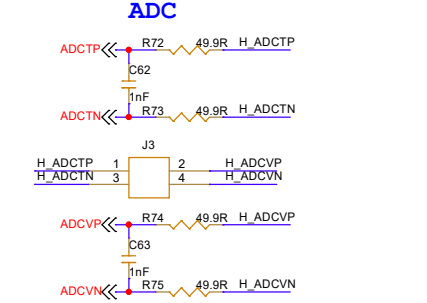
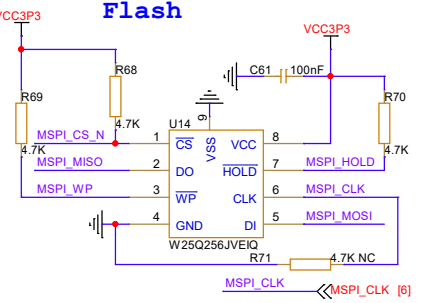
GW5AT-LV60PG484A



GW5AT-LV60PG484A



GW5AT-LV60PG484A







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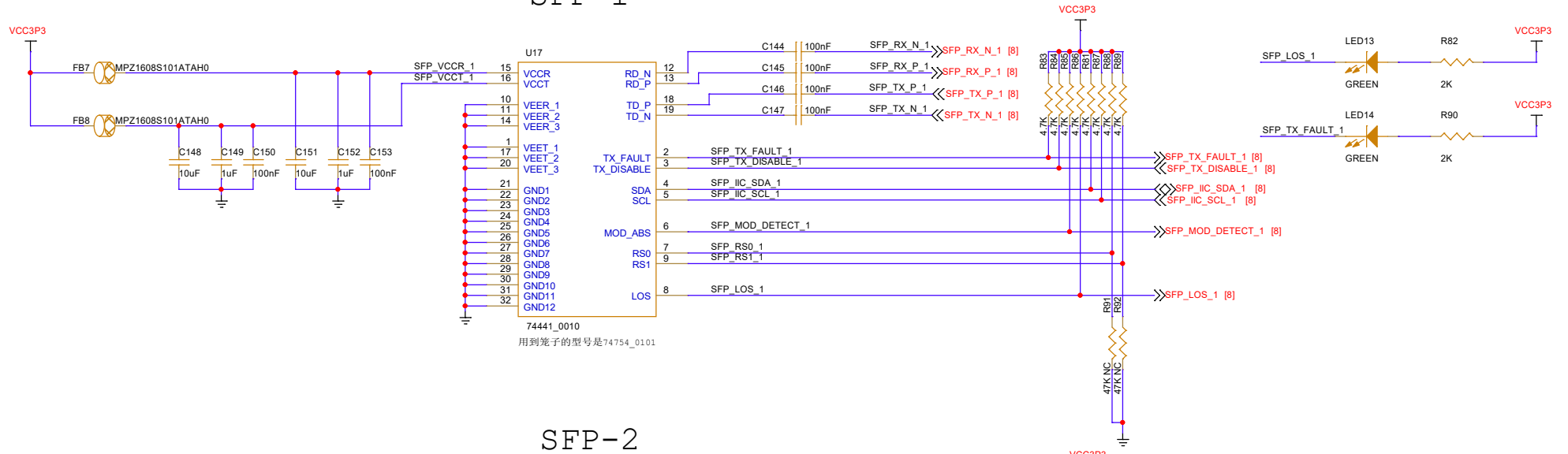
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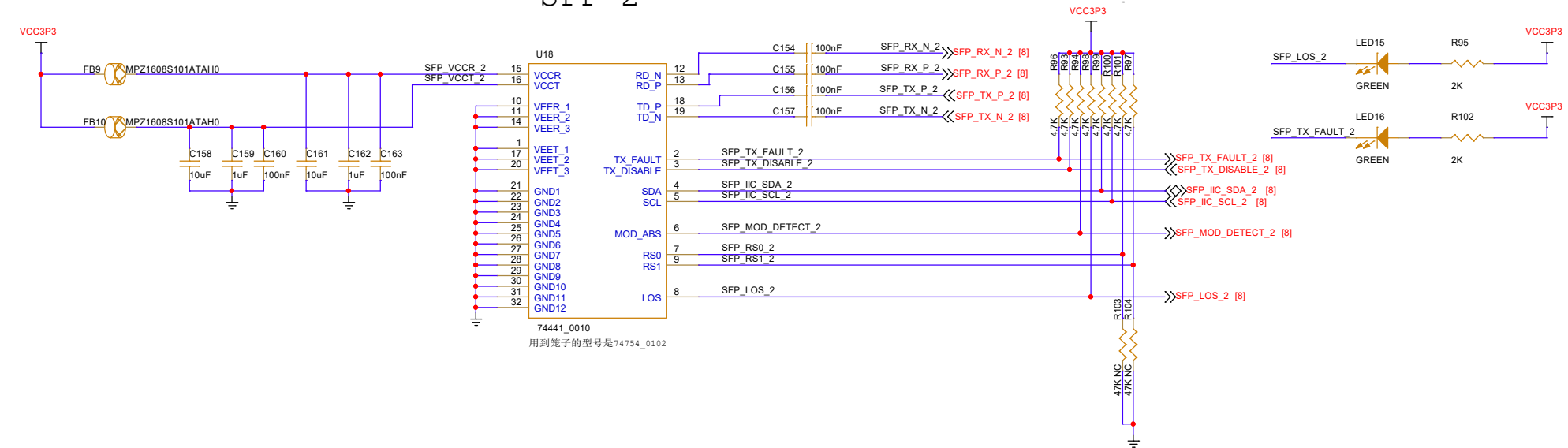
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A

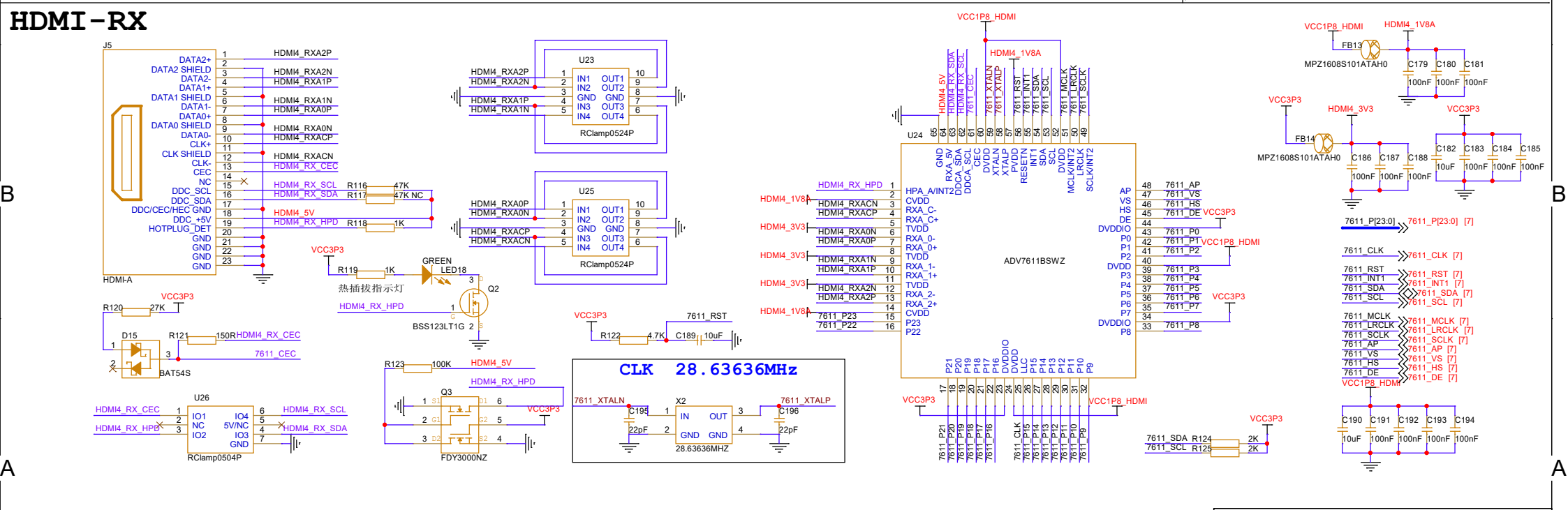
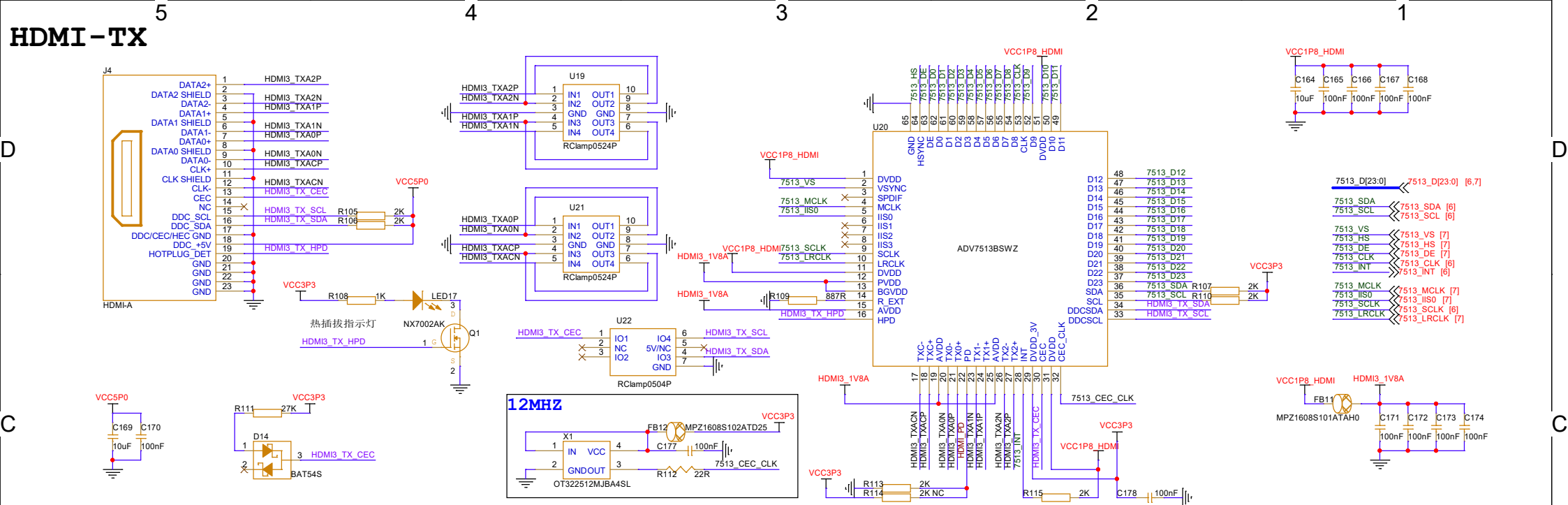
### SFP-1



### SFP-2

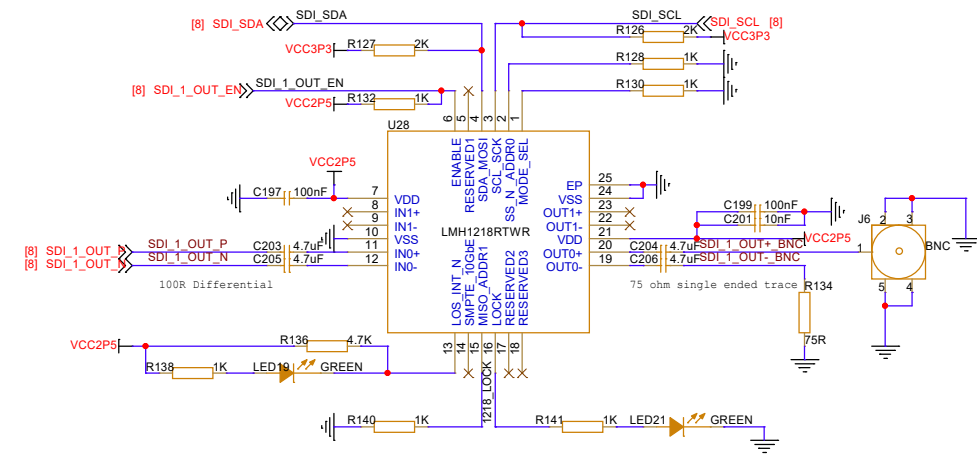


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Size	Document Number	Rev
A3	SFP	V1.1
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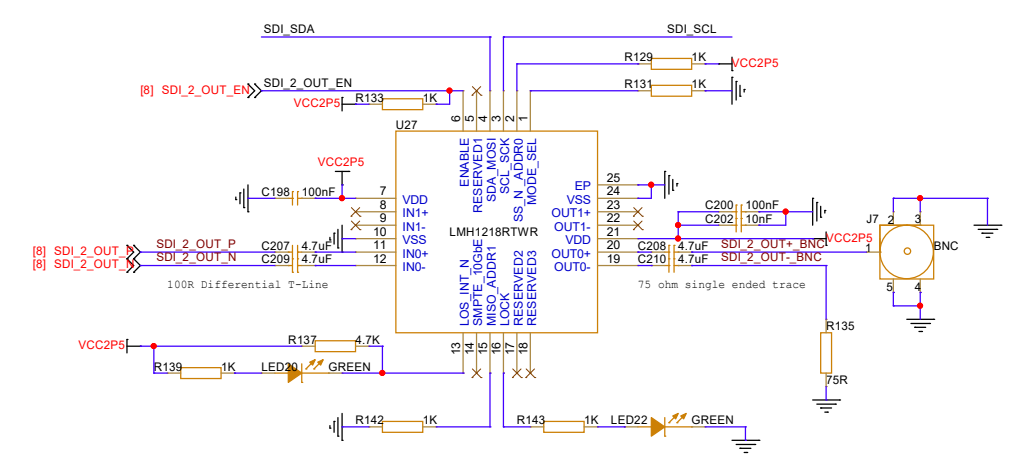


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Size	A3	Document Number	HDMI
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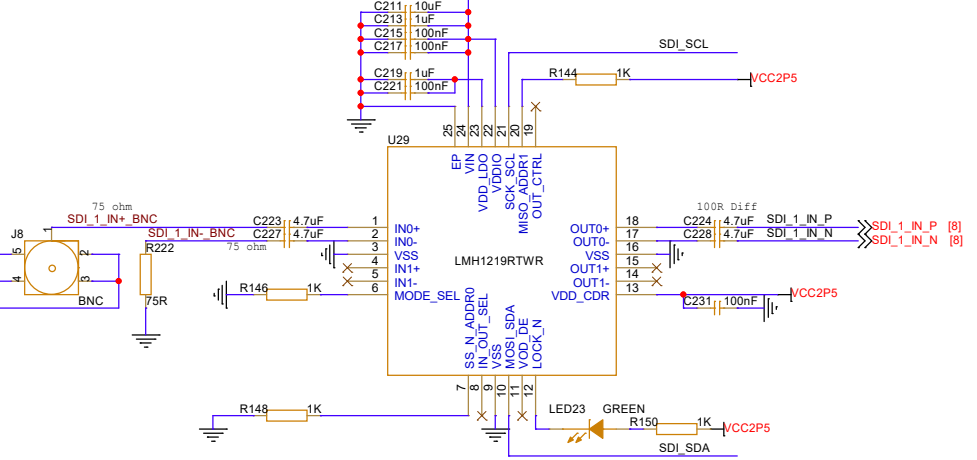
SDI-OUT-1



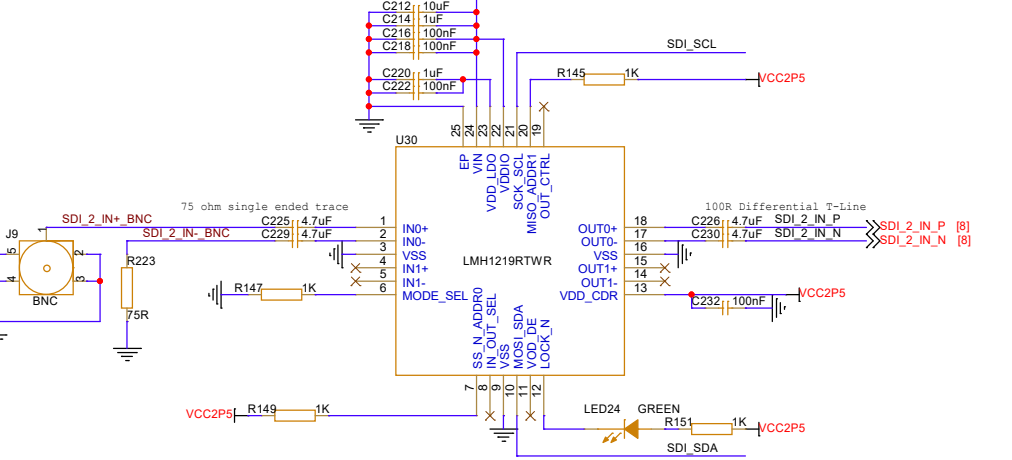
SDI-OUT-2



SDI-IN-1

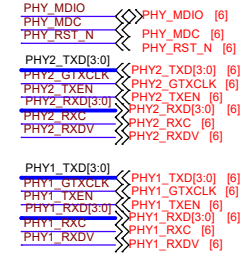
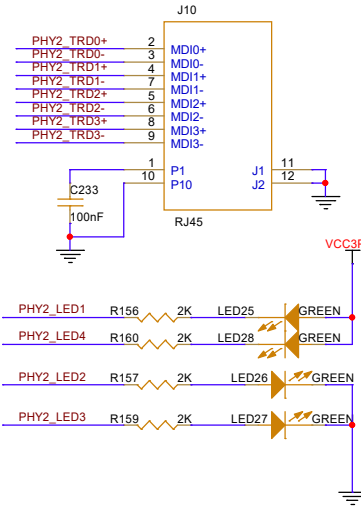
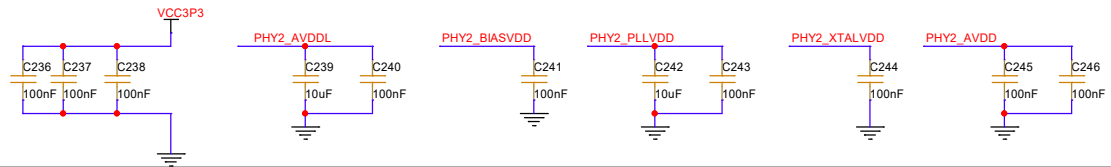
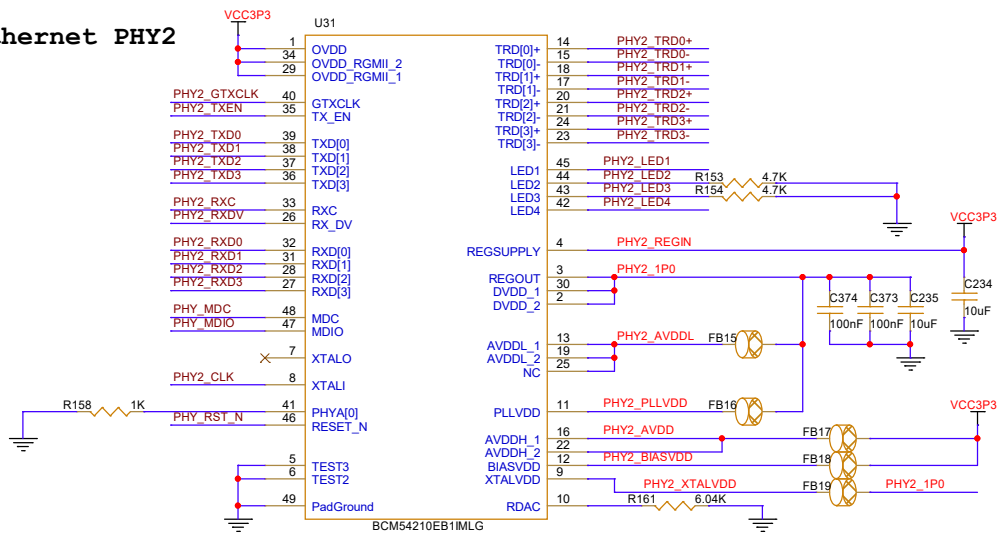


SDI-IN-2

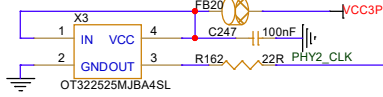


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Size	Document Number	Rev
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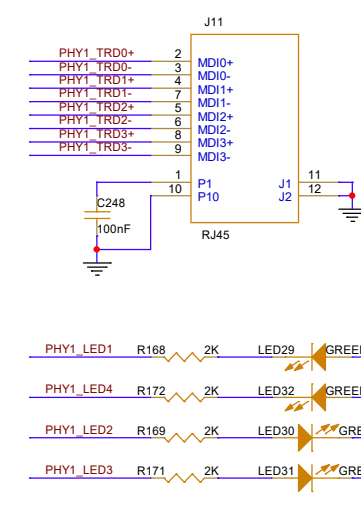
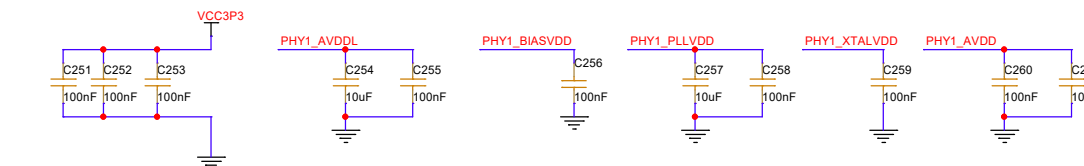
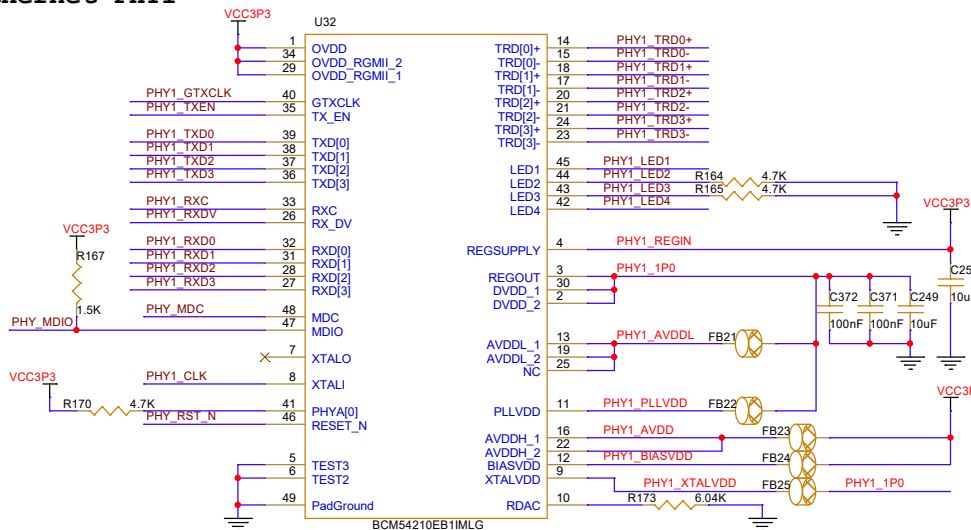
# Ethernet PHY2



# OSC 25MHZ



# Ethernet PHY1

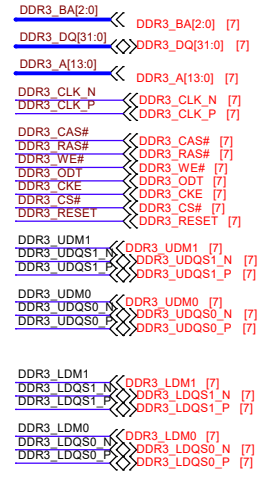
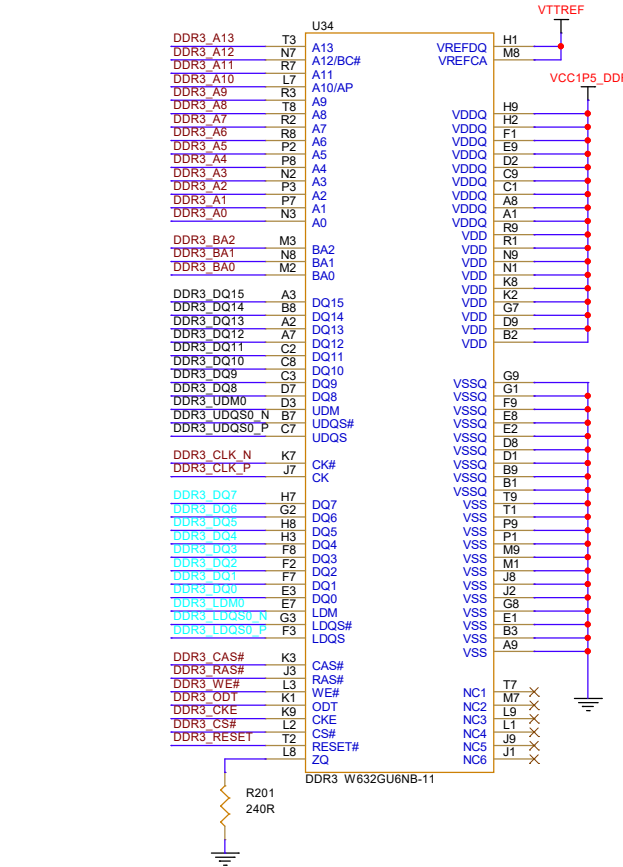
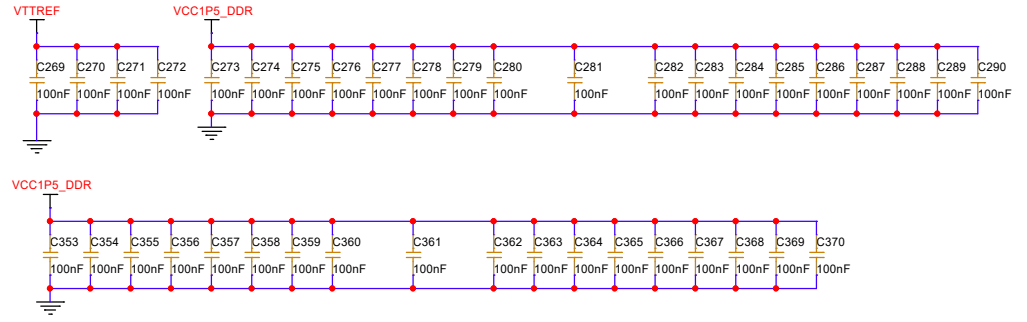
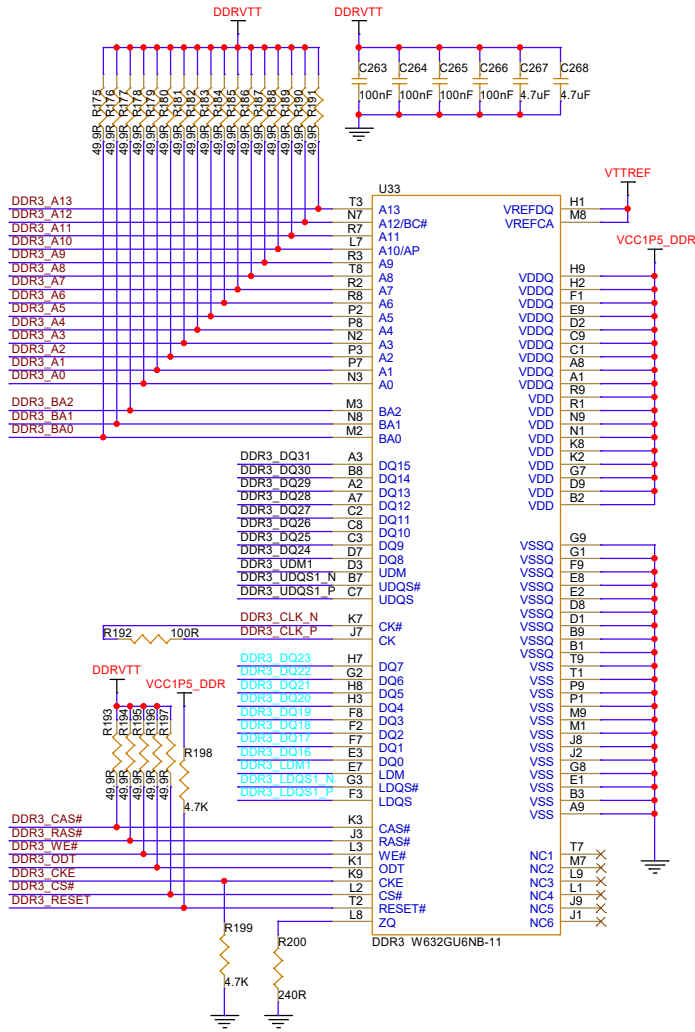


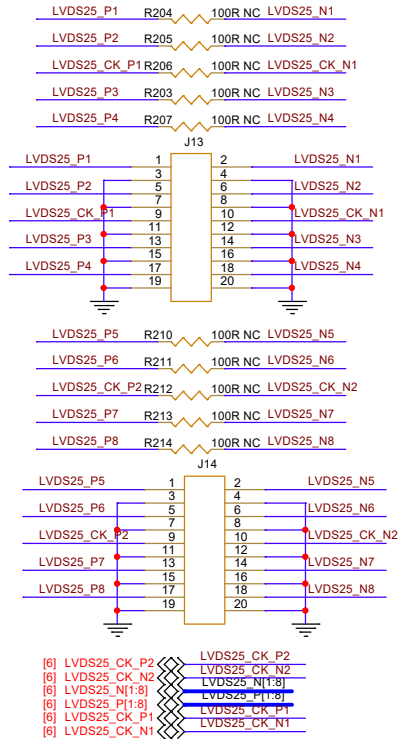
Default-LED Mode (Non-LOM-LED mode):

Status	LED[2]	LED[1]
100BASE-T	ON	ON
10BASE-T	ON	OFF
10BASE-T	OFF	ON
No link	OFF	OFF

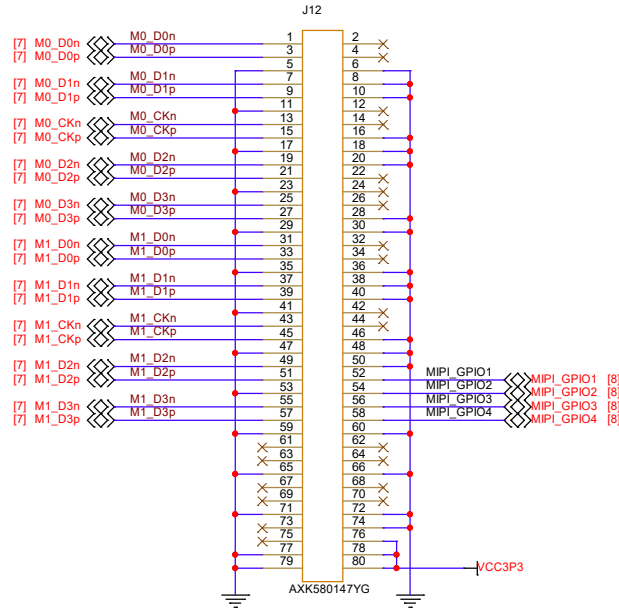
Set PHY Address as required.  
 TEST3/TEST2 = 00, PHY[A] = 0: PHY address = 00000.  
 TEST3/TEST2 = 00, PHY[A] = 1: PHY address = 00001.

# DDR3

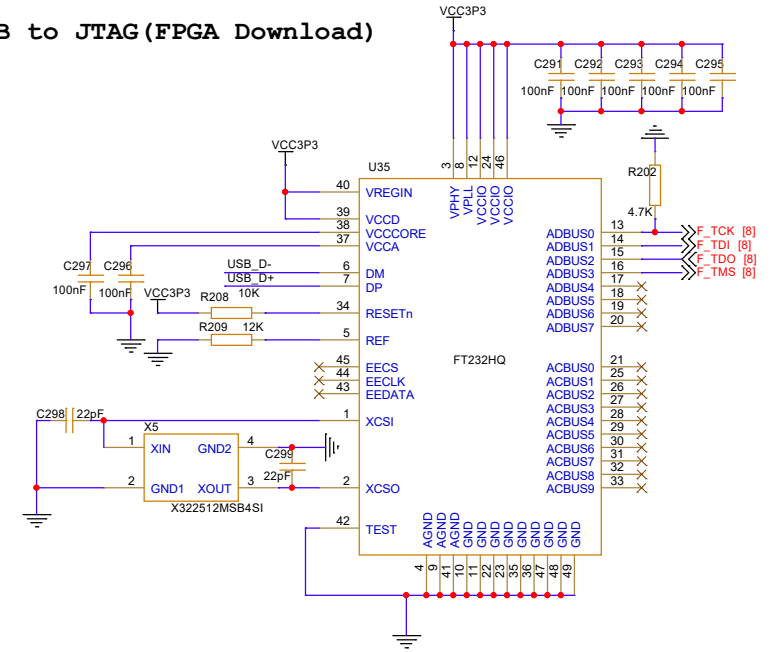




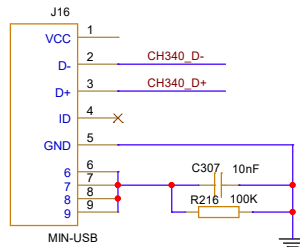
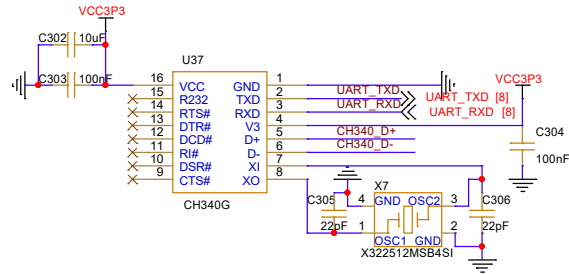
### MIPI



### USB to JTAG (FPGA Download)



### UART



File		
DK_START_GW5AT-LV60PG484A_V1.1		
Size	Document Number	Rev
A3	LVDS MIPI UART USB-JTAG	V1.1
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