DK_USB_GW5AT-LV60UG225_V1.0

User Guide

DBUG1280-1.0.1E, 02/14/2025

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Revision History

Date	Version	Description
11/15/2024	1.0E	Initial version published.
02/14/2025	1.0.1E	The title of “Table 3-9 Pin Distribution of LED” updated.

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1 About This Guide

1.1 Purpose

The DK_USB_GW5AT-LV60UG225_V1.0 development board (hereinafter referred to as “the development board”) user guide consists of following three parts:

- A brief introduction to the features of the development board.
- An introduction to the development board system architecture and hardware resources.
- An introduction to the hardware circuits, functions and pin distribution.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- DS981, GW5AT series of FPGA Products Data Sheet
- UG1222, GW5AT-60 Pinout
- UG983, GW5AT series of FPGA Products Package and Pinout User Guide
- UG718, Arora V 60K FPGA Products Programming and Configuration User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
DDR	Double Data Rate
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable Input/Output
I2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
LDO	Low Dropout Regulator
MIPI	Mobile Industry Processor Interface
SDI	Serial Digital Interface

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

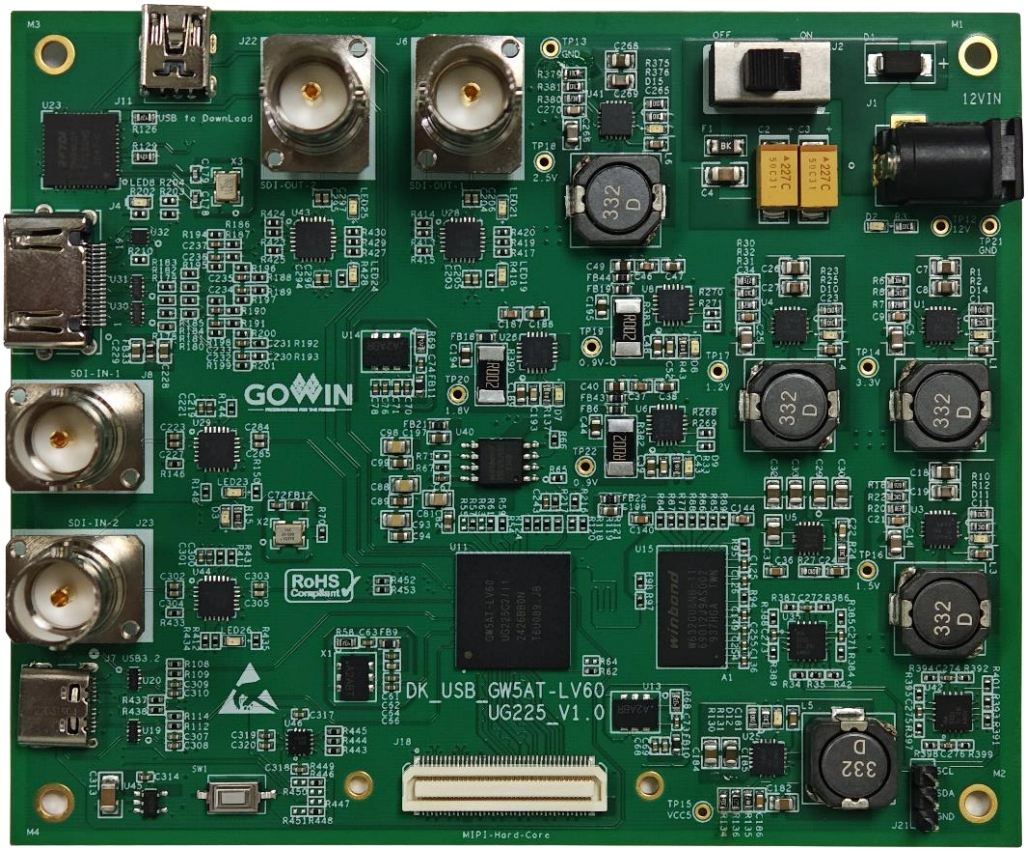
Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Development Board Introduction

2.1 Overview

Figure 2-1 DK_USB_GW5AT-LV60UG225_V1.0 Development Board



Gowin GW5AT series of FPGA products are the 5 series products of Arora family, with abundant internal resources, high-performance DSP with a new architecture that supports AI operations, high-speed LVDS interface and abundant BSRAM resources. At the same time, it integrates self-developed DDR3 and SerDes supporting multiple protocols and provides a variety of packages. It is suitable for applications such as low power, high

performance and compatibility design.

DK_USB_GW5AT-LV60UG225_V1.0 development board applies to DDR3 high-speed storage, SDI and MIPI high-speed communication, integrates SDI-IN, SDI-OUT, MIPI CPHY, MIPI DPHY, HDMI, Type-C interfaces, supporting FPGA's MIPI C-PHY, MIPI D-PHY, USB 3.0, and 3G/6G SDI function evaluation, hardware verification, and software learning and debugging, etc.

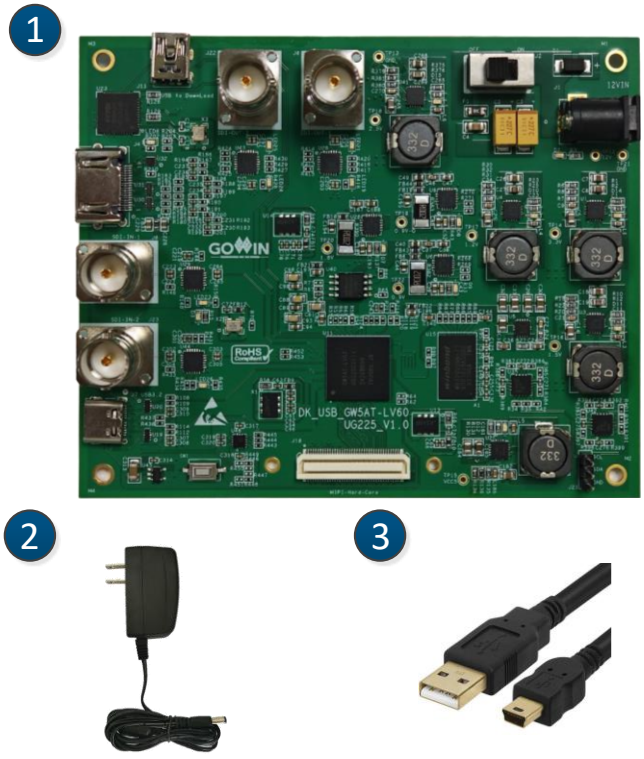
The development board adopts Gowin GW5AT-LV60UG225 FPGA device. For the internal resources of the chip, see *DS981, GW5AT series of FPGA Products Data Sheet*.

2.2 A Development Board Kit

The development board kit includes the following items:

1. DK_USB_GW5AT-LV60UG225_V1.0 development board
2. 12V power (Input: AC 100-240V~50/60Hz 0.6A, output: DC12V 2A)
3. Mini USB-B Cable

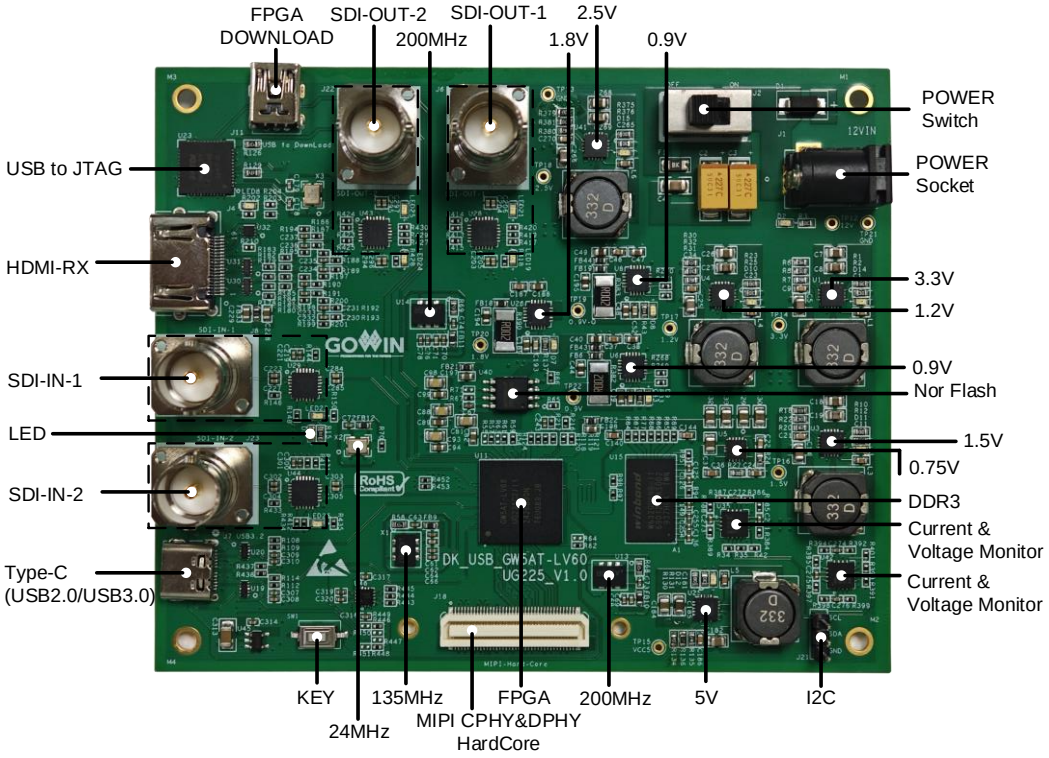
Figure 2-2 A Development Board Kit



① DK_USB_GW5AT-LV60UG225_V1.0 development board
② 12V power supply adapter
③ Mini USB-B Cable

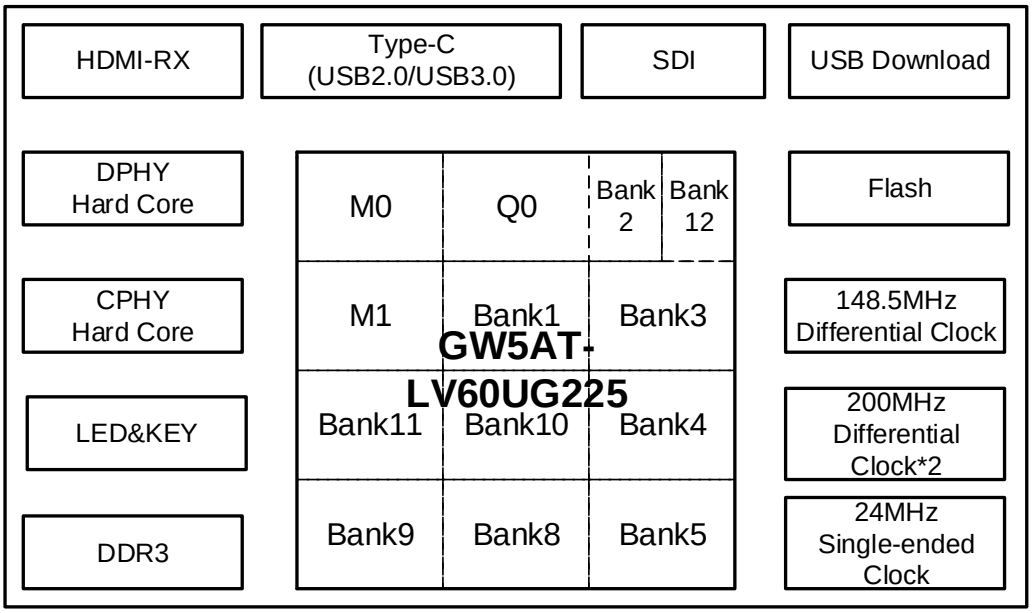
2.3 PCB Components

Figure 2-3 PCB Components



2.4 System Block Diagram

Figure 2-4 System Block Diagram



2.5 Features

The key features are as follows:

- FPGA Device
  - Gowin GW5AT-LV60UG225 FPGA
- Download and Boot
  - Integrate USB download circuit on the development board, download through Mini USB-B interface
  - External SPI Flash for storing FPGA configuration file
- Power
  - External DC12V/2A Power
  - The Power light is on after power on.
  - The board generates 5V, 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, 0.9V, 0.75V power.
- Clock System
  - One 24MHz clock
  - One 148.5MHz clock
  - Two 200MHz clocks
- Memory Device
  - 2Gbit DDR3 SDRAM
  - 128Mbit NOR Flash
- HDMI Interface
  - One HDMI-RX interface
- MIPI Interface
  - One CPHY hard core interface, including 3lane
  - One DPHY hard core interface, including 4 data (data) + 1 lane (clk)
  - Eight GPIOs reserved
- Type-C Interface
  - Support USB 2.0 and USB 3.0 protocols
- SDI Interface
  - Two SDI-IN interfaces
  - Two SDI-OUT interfaces
  - Support 3G and 6G SDI interfaces
- I2C Interface
  - One I2C interface
- Key & Indicator
  - 1 Key
  - 1 LED indicator

3 Development Board Circuit

3.1 FPGA

3.1.1 Overview

For the resources of GW5AT series of FPGA Products, refer to *DS981, GW5AT series of FPGA Products Data Sheet*.

3.1.2 I/O BANK Description

For the I/O BANK, package, and pinout information, see *UG983, GW5AT series of FPGA Products Package and Pinout User Guide* for more details.

3.2 Power Supply

3.2.1 Introduction

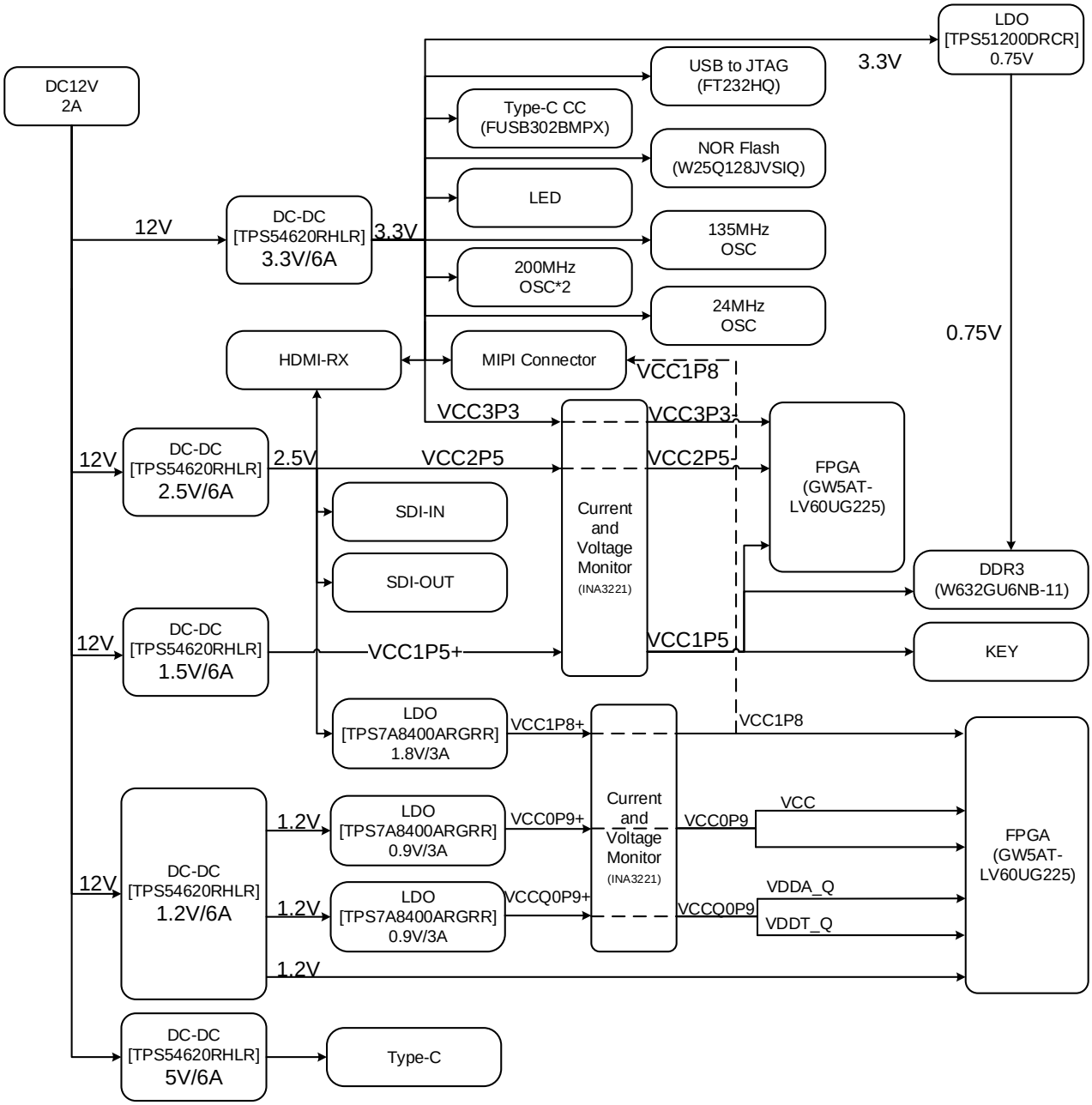
The development board needs to be powered by a 12V power adapter.

The input parameter of the adapter is AC 100-240V~50/60MHz 0.6A, and the output parameter is DC 12V 2A.

The input 12V power is regulated by the PMIC on the development board to generate 5V, 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, 0.9V, and 0.75V power supplies, thus meeting the power supply requirements of the development board.

3.2.2 Power Distribution

Figure 3-1 Power Distribution Diagram



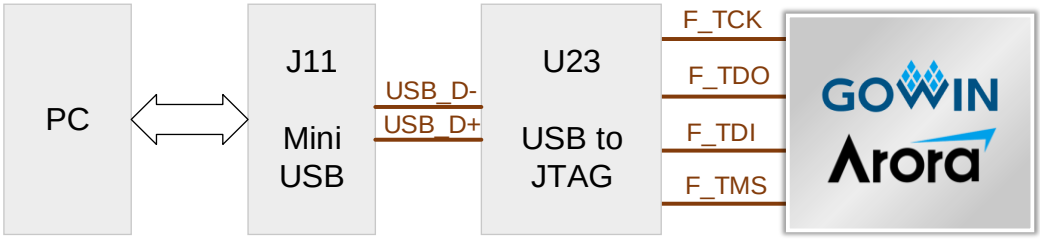
3.3 Download Module

3.3.1 Introduction

The development board has a Mini USB-B download port (J11) designed to program the programs to external SPI FLASH or download them to SRAM.

The download connection diagram is show in Figure 3-2.

Figure 3-2 Connection Diagram of Download



3.3.2 Pin Distribution

Table 3-1 JTAG Pin Distribution

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_TCK	C15	12	3.3V	JTAG signal
F_TDO	D15	12	3.3V	
F_TDI	B15	12	3.3V	
F_TMS	E15	12	3.3V	

3.4 Clock

3.4.1 Introduction

The development board provides multiple FPGA clock sources, including one 24 MHz single-ended clock, one 148.5 MHz differential clock, and two 200 MHz differential clocks. Among them, the 148.5 MHz differential clock and one of the 200MHz differential clocks are connected the FPGA SerDes high-speed clock pins. The clock pin distribution is shown in Figure 3-3.

Figure 3-3 Clock Connection Diagram

3.4.2 Pin Distribution

Table 3-2 Clock Pin Distribution

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_CLK_24M	H5	10	1.8V	50MHz single-ended clock
F_CLK_200M_P	K5	10	1.8V	200MHz differential clock
F_CLK_200M_N	J5	10	1.8V	200MHz differential clock
Q0_148.5MHz_P	B5	Q0	-	148.5MHz differential clock
Q0_148.5MHz_N	A5	Q0	-	148.5MHz differential clock
Q0_200MHz_P	D10	Q0	-	200MHz differential clock
Q0_200MHz_N	C10	Q0	-	200MHz differential clock

3.5 DDR3

3.5.1 Introduction

The development board includes one 2Gbit DDR3 chip. The signal of DDR3 chip is connected to the BANK8 and BANK9 of FPGA. The specific configurations of DDR3 are as shown in Table 3-3.

Table 3-3 DDR3 Configuration

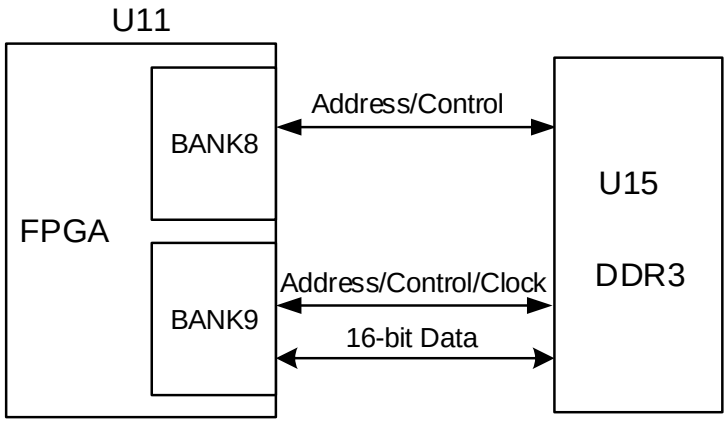
Designator	Capacity
U15	128M x 16bit

DDR3 hardware design requires strict consideration of signal integrity.

In the design of circuit and PCB, matching resistor/termination resistor, impedance control and equal length control of traces have been fully considered to ensure DDR3 works stably at high speed.

The hardware connection diagram of DDR3 is as show in Figure 3-4.

Figure 3-4 Hardware Connection Diagram of DDR3



3.5.2 Pin Distribution

Table 3-4 DDR3 Pin Distribution

Signal Name	FPGA (U1) Pin No.	BANK	I/O Level	Description
DDR3_A0	L7	9	1.5V	Address
DDR3_A1	M11	8	1.5V	Address
DDR3_A2	N11	8	1.5V	Address
DDR3_A3	N10	8	1.5V	Address
DDR3_A4	L10	8	1.5V	Address
DDR3_A5	M10	8	1.5V	Address
DDR3_A6	L8	9	1.5V	Address
DDR3_A7	N12	8	1.5V	Address
DDR3_A8	M9	9	1.5V	Address
DDR3_A9	R13	8	1.5V	Address
DDR3_A10	P13	8	1.5V	Address
DDR3_A11	K10	8	1.5V	Address
DDR3_A12	R14	8	1.5V	Address
DDR3_A13	P9	9	1.5V	Address
DDR3_BA0	N2	9	1.5V	Bank address

Signal Name	FPGA (U1) Pin No.	BANK	I/O Level	Description
DDR3_BA1	P11	8	1.5V	Bank address
DDR3_BA2	L6	9	1.5V	Bank address
DDR3_CS#	P2	9	1.5V	Chip select
DDR3_CAS#	R2	9	1.5V	Column address strobe
DDR3_CKE	R12	8	1.5V	Clock Enable
DDR3_ODT	N1	9	1.5V	On-Die Termination Enable
DDR3_RAS#	N7	9	1.5V	Row address strobe
DDR3_RESET	N9	9	1.5V	Reset
DDR3_WE#	P1	9	1.5V	Write enable
DDR3_CLK0_P	N8	9	1.5V	Differential clock
DDR3_CLK0_N	M8	9	1.5V	Differential clock
DDR3_DQ0	M6	9	1.5V	Data
DDR3_DQ1	R4	9	1.5V	Data
DDR3_DQ2	M5	9	1.5V	Data
DDR3_DQ3	R6	9	1.5V	Data
DDR3_DQ4	L5	9	1.5V	Data
DDR3_DQ5	R7	9	1.5V	Data
DDR3_DQ6	N6	9	1.5V	Data
DDR3_DQ7	P7	9	1.5V	Data
DDR3_DQ8	M4	9	1.5V	Data
DDR3_DQ9	M1	9	1.5V	Data
DDR3_DQ10	N5	9	1.5V	Data
DDR3_DQ11	L1	9	1.5V	Data
DDR3_DQ12	N4	9	1.5V	Data
DDR3_DQ13	L3	9	1.5V	Data
DDR3_DQ14	P5	9	1.5V	Data
DDR3_DQ15	L2	9	1.5V	Data
DDR3_LDM0	R5	9	1.5V	Data input mask
DDR3_UDM0	M3	9	1.5V	Data input mask

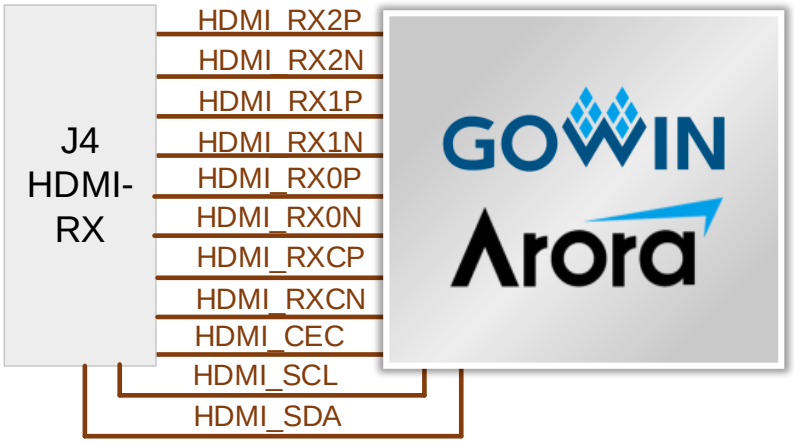
Signal Name	FPGA (U1) Pin No.	BANK	I/O Level	Description
DDR3_LDQS0_P	R8	9	1.5V	Data Clock
DDR3_LDQS0_N	R9	9	1.5V	Data Clock
DDR3_UDQS0_P	R3	9	1.5V	Data Clock
DDR3_UDQS0_N	P3	9	1.5V	Data Clock

3.6 HDMI-RX Interface

3.6.1 Introduction

The development board provides an HDMI receiver interface for the reception of HDMI signals through an internal FPGA IP. The connection diagram of the DP interfaces is as follows.

Figure 3-5 Connection Diagram of HDMI-RX Interface



3.6.2 Pin Distribution

Table 3-5 Pin Distribution of DP-RX Interface

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
HDMI_RXCP	D13	2	2.5V	HDMI differential clock
HDMI_RXCN	C14	2	2.5V	HDMI differential clock
HDMI_RX0P	B14	2	2.5V	HDMI receiving data
HDMI_RX0N	A14	2	2.5V	HDMI receiving data
HDMI_RX1P	B13	2	2.5V	HDMI receiving data
HDMI_RX1N	A13	2	2.5V	HDMI receiving data

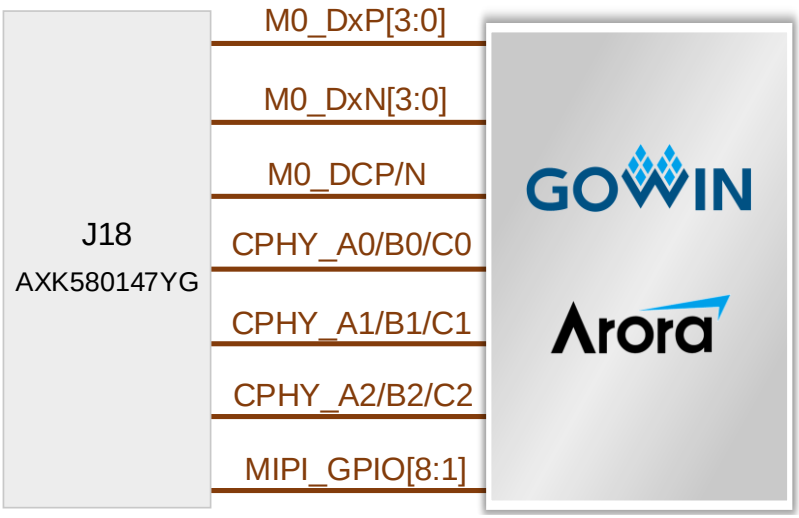
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
HDMI_RX2P	E5	1	2.5V	HDMI receiving data
HDMI_RX2N	E6	1	2.5V	HDMI receiving data
HDMI_CEC	H6	10	3.3V	CEC
HDMI_SCL	M13	5	3.3V	I2C serial clock
HDMI_SDA	L12	5	3.3V	I2C serial data

3.7 MIPI Interface

3.7.1 Introduction

The development board leads one MIPI CPHY hard core interface and one MIPI DPHY hard core interface from the FPGA. The MIPI CPHY hard core interface, MIPI DPHY hard core interface, and eight 3.3V GPIOs are led to 80P AXK580147YG connector with 0.5mm pitch. The connection diagram is as follows.

Figure 3-6 Connection Diagram of MIPI CPHY & DPHY Hard Core Interfaces



3.7.2 Pin Distribution

Table 3-6 Pin Distribution of MIPI CPHY & DPHY Hard core Interface

J18 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	M0_D3N	C2	MIPI	-	MIPI DPHY data signal
2	NC	-	-	-	Floating
3	M0_D3P	C1	MIPI	-	MIPI DPHY data signal
4	NC	-	-	-	Floating
5	GND	-	-	-	GND
6	GND	-	-	-	GND
7	M0_D2N	E3	MIPI	-	MIPI DPHY data signal
8	GND	-	-	-	GND
9	M0_D2P	F4	MIPI	-	MIPI DPHY data signal
10	GND	-	-	-	GND
11	GND	-	-	-	GND
12	NC	-	-	-	Floating
13	M0_DCN	F3	MIPI	-	MIPI DPHY clock signal
14	NC	-	-	-	Floating
15	M0_DCP	G3	MIPI	-	MIPI DPHY clock signal
16	GND	-	-	-	GND
17	GND	-	-	-	GND
18	GND	-	-	-	GND
19	M0_D1N	H3	MIPI	-	MIPI DPHY data signal
20	GND	-	-	-	GND
21	M0_D1P	H4	MIPI	-	MIPI DPHY data signal
22	VCC1P8	-	-	1.8V	Power
23	GND	-	-	-	GND
24	VCC1P8	-	-	1.8V	Power
25	M0_D0N	J3	MIPI	-	MIPI DPHY data signal
26	VCC1P8	-	-	1.8V	Power

J18 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
27	M0_D0P	J4	MIPI	-	MIPI DPHY data signal
28	GND	-	-	-	GND
29	GND	-	-	-	GND
30	GND	-	-	-	GND
31	GND	-	-	-	GND
32	NC	-	-	-	Floating
33	GND	-	-	-	GND
34	NC	-	-	-	Floating
35	GND	-	-	-	GND
36	GND	-	-	-	GND
37	GND	-	-	-	GND
38	GND	-	-	-	GND
39	GND	-	-	-	GND
40	GND	-	-	-	GND
41	M1_D0A	D1	MIPI	-	MIPI CPHY data signal
42	NC	-	-	-	Floating
43	M1_D0B	E2	MIPI	-	MIPI CPHY data signal
44	NC	-	-	-	Floating
45	M1_D0C	E1	MIPI	-	MIPI CPHY data signal
46	GND	-	-	-	GND
47	GND	-	-	-	GND
48	GND	-	-	-	GND
49	GND	-	-	-	GND
50	GND	-	-	-	GND
51	M1_D1A	F1	MIPI	-	MIPI CPHY data signal
52	MIPI_GPIO1	G5	11	3.3V	GPIO reserved
53	M1_D1B	G1	MIPI	-	MIPI CPHY data signal
54	MIPI_GPIO2	H12	4	3.3V	GPIO reserved
55	M1_D1C	G2	MIPI	-	MIPI CPHY data signal

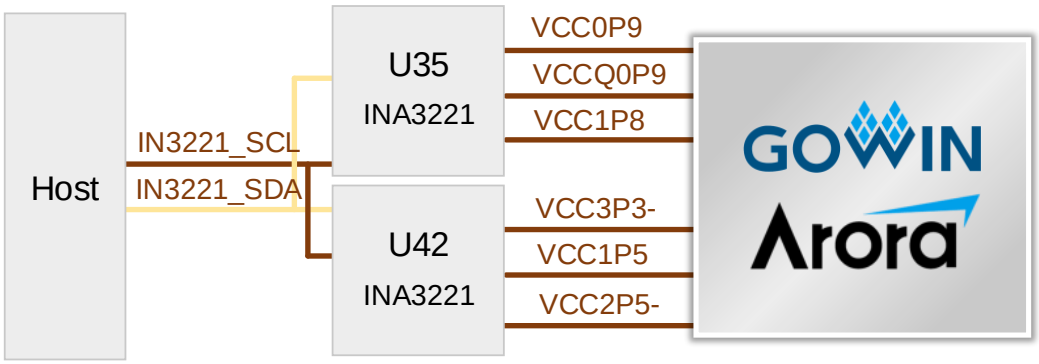
J18 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
56	MIPI_GPIO3	H15	4	3.3V	GPIO reserved
57	GND	-	-	-	GND
58	MIPI_GPIO4	J15	4	3.3V	GPIO reserved
59	GND	-	-	-	GND
60	GND	-	-	-	GND
61	M1_D2A	H1	MIPI	-	MIPI CPHY data signal
62	MIPI_GPIO5	F5	11	3.3V	GPIO reserved
63	M1_D2B	J1	MIPI	-	MIPI CPHY data signal
64	MIPI_GPIO6	K3	11	3.3V	GPIO reserved
65	M1_D2C	J2	MIPI	-	MIPI CPHY data signal
66	GND	-	-	-	GND
67	GND	-	-	-	GND
68	MIPI_GPIO7	K4	11	3.3V	GPIO reserved
69	GND	-	-	-	GND
70	MIPI_GPIO8	G12	4	3.3V	GPIO reserved
71	GND	-	-	-	GND
72	GND	-	-	-	GND
73	GND	-	-	-	GND
74	GND	-	-	-	GND
75	GND	-	-	-	GND
76	VCC3P3	-	-	3.3V	Power
77	GND	-	-	-	GND
78	VCC3P3	-	-	3.3V	Power
79	GND	-	-	-	GND
80	VCC3P3	-	-	3.3V	Power

3.8 I2C Interface

3.8.1 Introduction

The development board includes one I2C interface as the host communication interface. The host can monitor the voltages of FPGA VCC, MIPI, VCCX, SerDes, and each BANK through this interface. The connection diagram of I2C interface is shown in Figure 3-7.

Figure 3-7 Connection Diagram of I2C Interface



3.8.2 Pin Distribution

Table 3-7 J21 Pin Distribution of I2C Interface

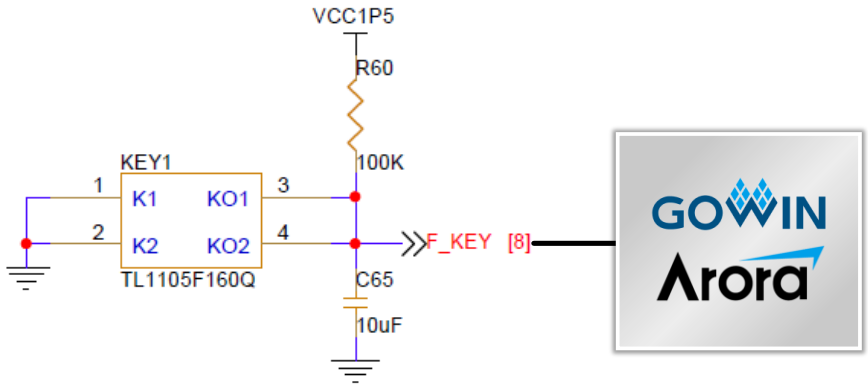
J21 Pin No.	Signal Name	I/O Level	Description
1	IN3221_SCL	3.3V	Serial bus clock line
2	IN3221_SDA	3.3V	Serial bus data line
3	GND	-	GND

3.9 Key & LED

3.9.1 Introduction

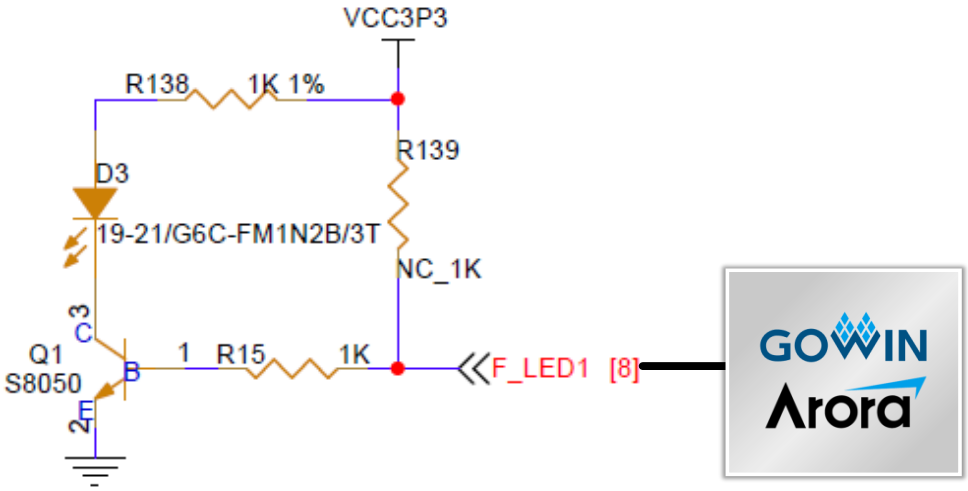
There is one user key on the development board. The user key is connected to the general IO of FPGA BANK8. The corresponding IO input voltage of the FPGA is low when the key is pressed while high when the key is not pressed. The connection diagram is shown in Figure 3-8.

Figure 3-8 Connection Diagram of Key



The development board includes one user LED. The user LED is connected to the IO of FPGA BANK8 and can be switched on and off via the program. The user LEDs will be on when the IO voltage is high. The user LEDs will be off when the IO voltage is low. The connection diagram is shown in Figure 3-8.

Figure 3-9 Connection Diagram of LED



3.9.2 Pin Distribution

Table 3-8 Pin Distribution of Key

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_KEY	R10	8	1.5V	Key

Table 3-9 Pin Distribution of LED

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_LED1	R11	8	1.5V	LED indicator

3.10 Type-C Interface

3.10.1 Introduction

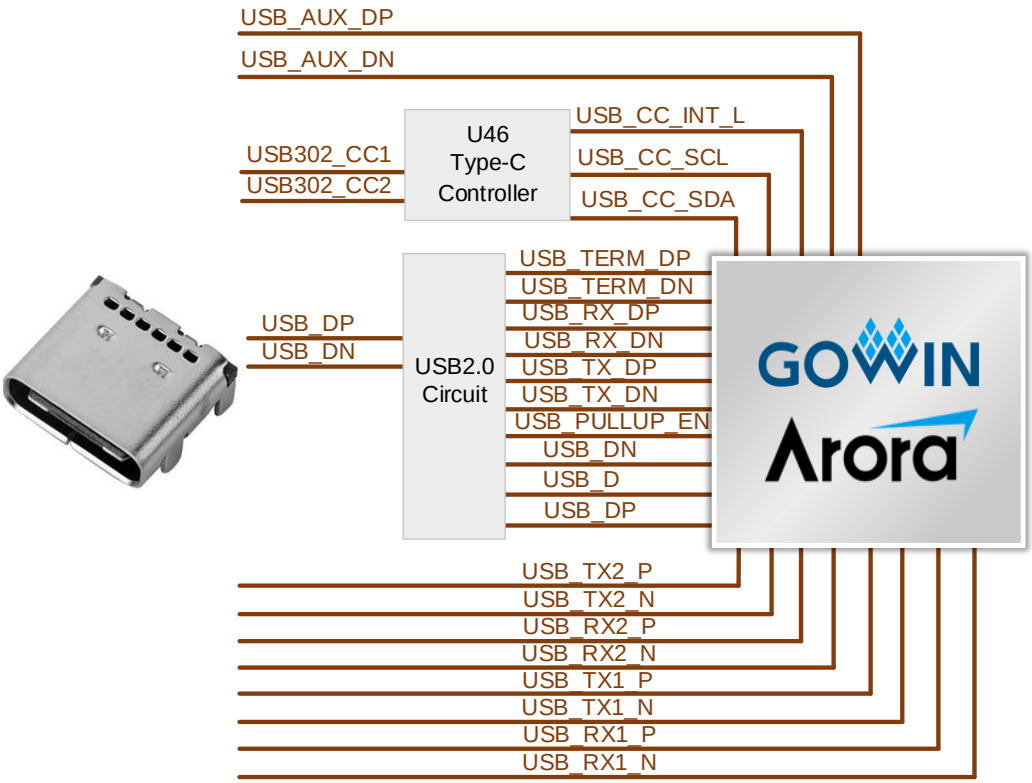
The development board leads a Type-C interface, supporting USB 2.0 and USB 3.0 data transmission. The USB 2.0 is implemented using the Gowin USB 2.0 SoftPHY IP solution, connected to the FPGA through an RC circuit. For detailed information on the peripheral circuitry, please refer to *IPUG781, Gowin USB 2.0 SoftPHY IP user guide*.

The Type-C interface on the development board connects two SerDes signals to the FPGA, USB 3.0 is implemented with the Gowin USB 3.0 PHY IP. As of November 2024, IP V1.2 supports one SerDes lane signal and only allows single-sided plug on the Type-C interface. Future updates will add support for reversible plug.

Note!

The CC circuit on the development board has not been verified. Use with caution!

Figure 3-10 Connection Diagram of Type-C Interface



3.10.2 Pin Distribution

Table 3-10 Pin Distribution of Type-C Interface

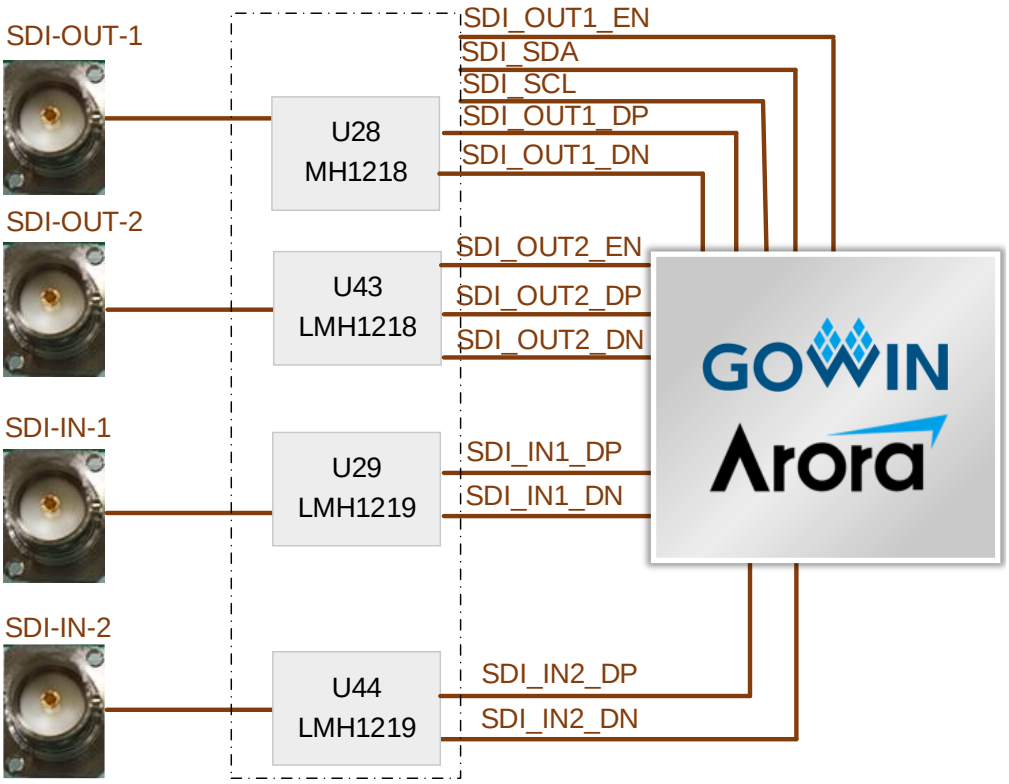
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
USB_TX2_P	D4	SerDes Q0	-	Type-C TX2+
USB_TX2_N	C4	SerDes Q0	-	Type-C TX2-
USB_RX2_P	B3	SerDes Q0	-	Type-C RX2+
USB_RX2_N	A3	SerDes Q0	-	Type-C RX2-
USB_TX1_P	D6	SerDes Q0	-	Type-C TX1+
USB_TX1_N	C6	SerDes Q0	-	Type-C TX1-
USB_RX1_P	B7	SerDes Q0	-	Type-C RX1+
USB_RX1_N	A7	SerDes Q0	-	Type-C RX1-
USB_AUX_DP	E7	1	2.5V	Type-C SUB1 channel
USB_AUX_DN	E8	1	2.5V	Type-C SUB2 channel
F_USB_CC1	F8	1	2.5V	Type-C CC1
F_USB_CC2	E9	1	2.5V	Type-C CC2
USB_PWR_EN	J11	5	3.3V	VBUS supply enable
USB_CC_INT_L	G15	3	3.3V	FUSB302BMPX control signals
USB_CC_SCL	G11	3	3.3V	
USB_CC_SDA	F11	3	3.3V	
USB_TX_DP	L15	5	3.3V	USB2.0 Signals
USB_TX_DN	M15	5	3.3V	
USB_RX_DP	L13	5	3.3V	
USB_RX_DN	L14	5	3.3V	
USB_TERM_DP	K12	5	3.3V	
USB_TERM_DN	K13	5	3.3V	
USB_DP	J13	5	3.3V	
USB_D	J14	5	3.3V	
USB_DN	N14	5	3.3V	
USB_D	N15	5	3.3V	
USB_PULLUP_EN	K11	5	3.3V	

3.11 SDI Interface

3.11.1 Introduction

The development board includes two SDI-IN interfaces and two SDI-OUT interfaces, and the interface connectors are BNC, which can meet the performance evaluation needs of the 3G SDI and 6G SDI interfaces.

Figure 3-11 Connection Diagram of SDI Interface



3.11.2 Pin Distribution

Table 3-11 Pin Distribution of SDI Interface

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
SDI_OUT1_EN	F10	1	2.5V	U28 (LMH1218) output enable
SDI_OUT2_EN	E10	1	2.5V	U43 (LMH1218) output enable
SDI_SDA	H11	5	3.3V	I2C control signal of LMH1218/LMH1219
SDI_SCL	H10	5	3.3V	
SDI_OUT2_DP	D8	SerDes Q0	-	LMH1218 IN0+

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
SDI_OUT2_DN	C8	SerDes Q0	-	LMH1218 IN0-
SDI_OUT1_DP	D12	SerDes Q0	-	LMH1218 IN0+
SDI_OUT1_DN	C12	SerDes Q0	-	LMH1218 IN0-
SDI_IN2_DP	B9	SerDes Q0	-	LMH1219 OUT0+
SDI_IN2_DN	A9	SerDes Q0	-	LMH1219 OUT0-
SDI_IN1_DP	B11	SerDes Q0	-	LMH1219 OUT0+
SDI_IN1_DN	A11	SerDes Q0	-	LMH1219 OUT0-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