DK_EDP_GW5AT-LV15MG132_V1.0

User Guide

DBUG1277-1.0E, 10/18/2024

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Revision History

Date	Version	Description
10/18/2024	1.0E	Initial version published.

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1 About This Guide

1.1 Purpose

The DK_EDP_GW5AT-LV15MG132_V1.0 development board (hereinafter referred to as “the development board”) user guide consists of following three parts:

- A brief introduction to the features of the development board
- An introduction to the development board system architecture and hardware resources
- An introduction to the hardware circuits, functions and pin distribution

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- DS1118, Arora V 15K FPGA Products Data Sheet
- UG1224, GW5AT-15 Pinout
- UG983, GW5AT series of FPGA Products Package and Pinout User Guide
- UG720, Arora V 15K FPGA Products Programming and Configuration User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable Input/Output
JTAG	Joint Test Action Group
LDO	Low Dropout Regulator
MIPI	Mobile Industry Processor Interface
SPI	Serial Peripheral Interface
EDP	Embedded Display Port

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

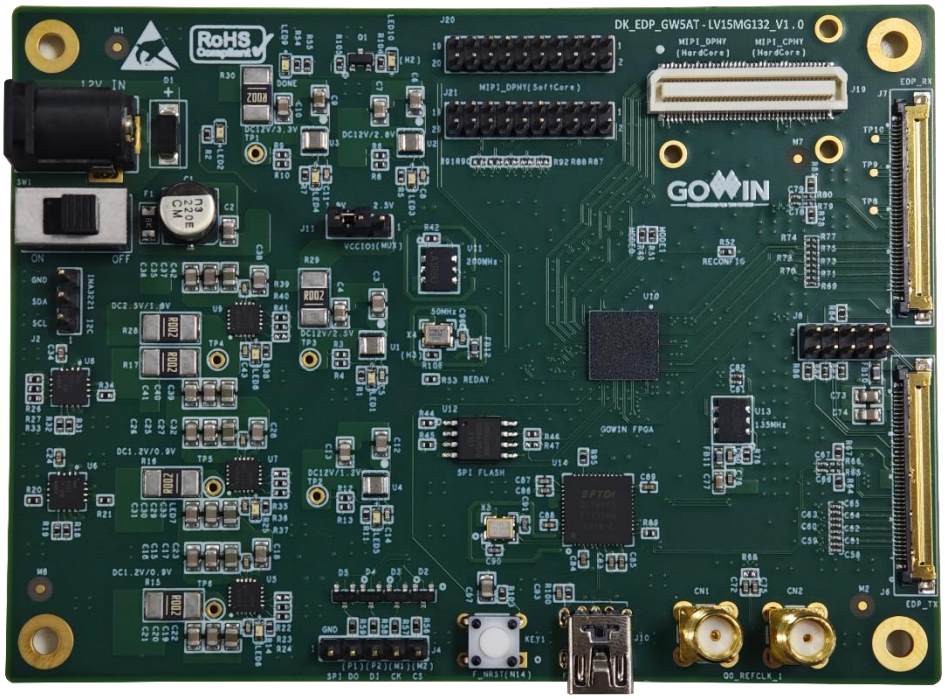
Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Development Board Introduction

2.1 Overview

Figure 2-1 DK_EDP_GW5AT-LV15MG132_V1.0 Development Board



Gowin GW5AT series of FPGA products are the 5 series products of Arora family, with abundant internal resources, high-performance DSP with a new architecture that supports AI operations, high-speed LVDS interface and abundant BSRAM resources. At the same time, it integrates self-developed DDR3, and provides a variety of packages. It is suitable for applications such as low power, high performance and compatibility design.

DK_EDP_GW5AT-LV15MG132_V1.0 development board applies to

MIPI high-speed communication, integrates EDP, LVDS, and SPI interfaces, supporting FPGA's MIPI C-PHY and MIPI D-PHY function evaluation, hardware verification, and software learning and debugging, etc.

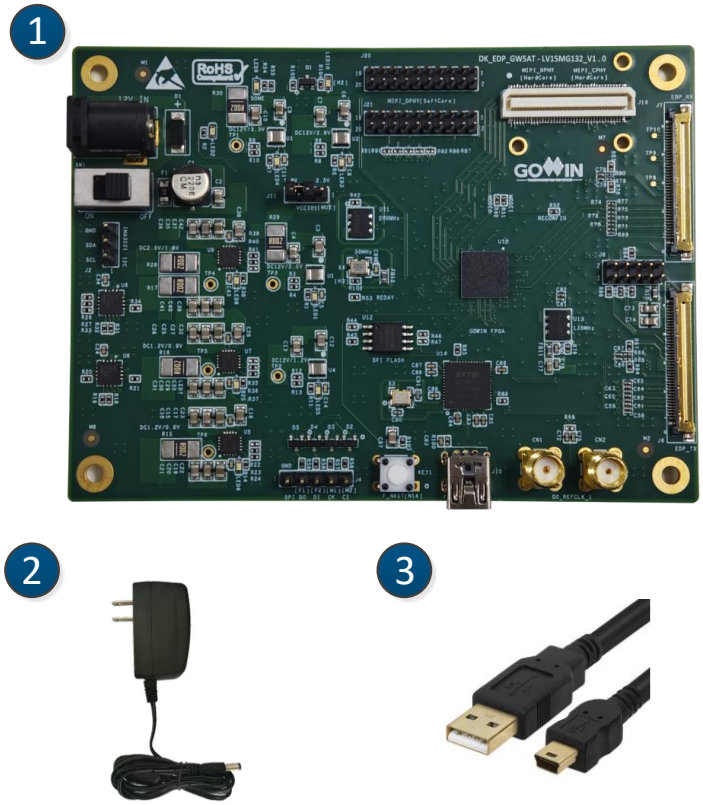
The development board adopts Gowin GW5AT-LV15MG132 FPGA device. For the internal resources of the chip, see *DS1118, Arora V 15K FPGA Products Data Sheet*.

2.2 A Development Board Kit

The development board kit includes the following items:

1. DK_EDP_GW5AT-LV15MG132_V1.0 development board
2. 12V power (Input: AC 100-240V~50/60Hz 0.6A, output: DC12V 2A)
3. Mini USB-B download cable

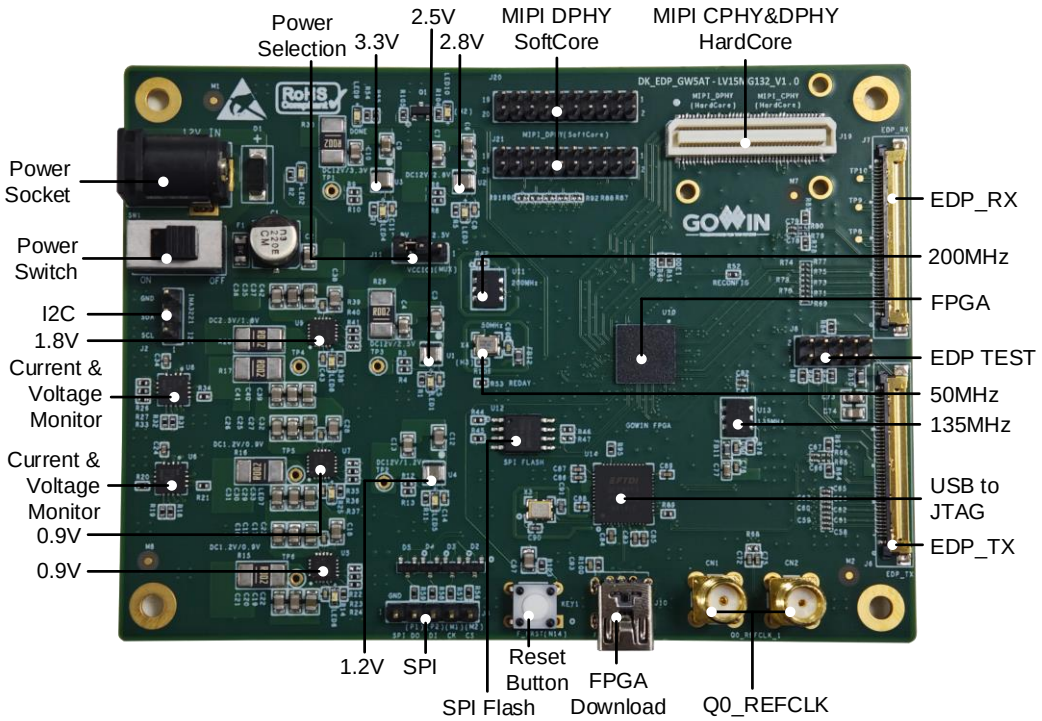
Figure 2-2 A Development Board Kit



① DK_EDP_GW5AT-LV15MG132_V1.0 development board
② 12V power supply adapter
③ Mini USB-B Cable

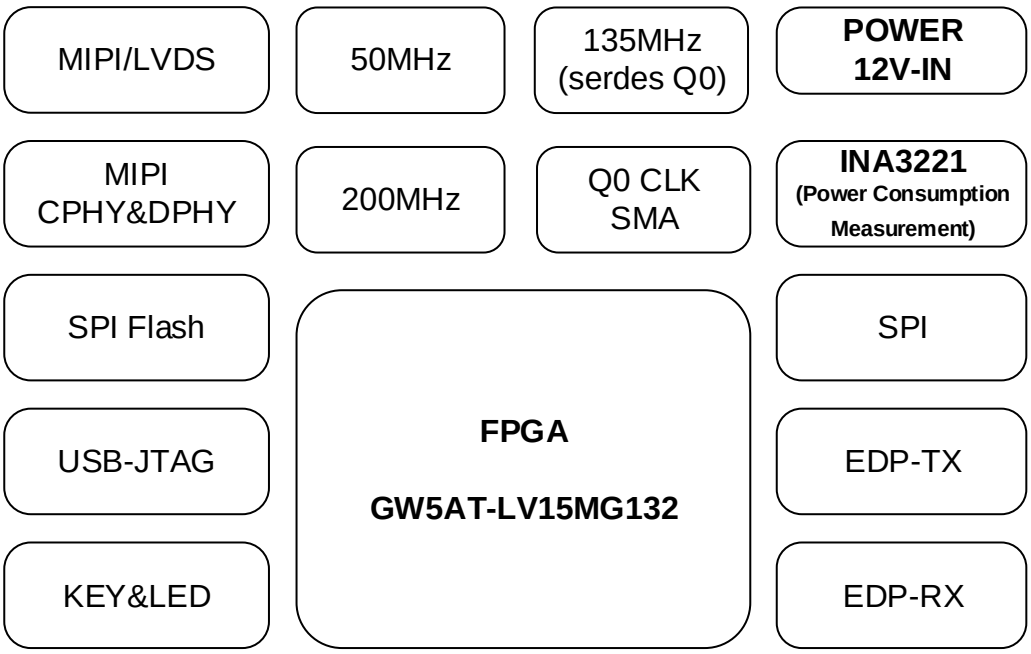
2.3 PCB Components

Figure 2-3 PCB Components



2.4 System Block Diagram

Figure 2-4 System Block Diagram



2.5 Features

The key features are as follows:

- FPGA Device
  - Gowin GW5AT-LV15MG132 FPGA
  - Max. user I/O: 53
- Download and Boot
  - Integrate USB download circuit on the development board, download through Mini USB-B interface
  - External SPI Flash Boot
- Power
  - External DC 12V 2A Power
  - The Power light is on after power on.
  - The board generates 3.3V, 2.8V, 2.5V, 1.8V, 1.2V, 0.9V power.
- Clock system
  - 50MHz single-ended clock
  - 135MHz differential clock
  - 200MHz differential clock
  - Receiving differential clock signal through SMA interface
- Memory device
  - 64Mbit NOR Flash
- EDP Interface
  - 1-channel EDP-TX interface
  - 1-channel EDP-RX interface
- MIPI Interface
  - 1-channel CPHY hard core interface, including 3-trios data lanes
  - 1-channel DPHY hard core interface, including 4 data lanes + 1 clk lane
  - 1-channel DPHY soft core interface can be used as LVDS interface, including 4 data lanes + 1 clk lane
- SPI Interface
  - 1-channel SPI interface
  - Support remote upgrades
- I2C Interface
  - 1-channel I2C interface
- Key & Indicator
  - 1 low-level reset key
  - 1 LED indicator

3 Development Board Circuit

3.1 FPGA

Overview

For the resources of GW5AT series of FPGA Products, refer to *DS1118, Arora V 15K FPGA Products Data Sheet*.

I/O BANK Description

For the I/O BANK, package, and pinout information, see *UG983, GW5AT series of FPGA Products Package and Pinout User Guide* for more details.

3.2 Power Supply

3.2.1 Introduction

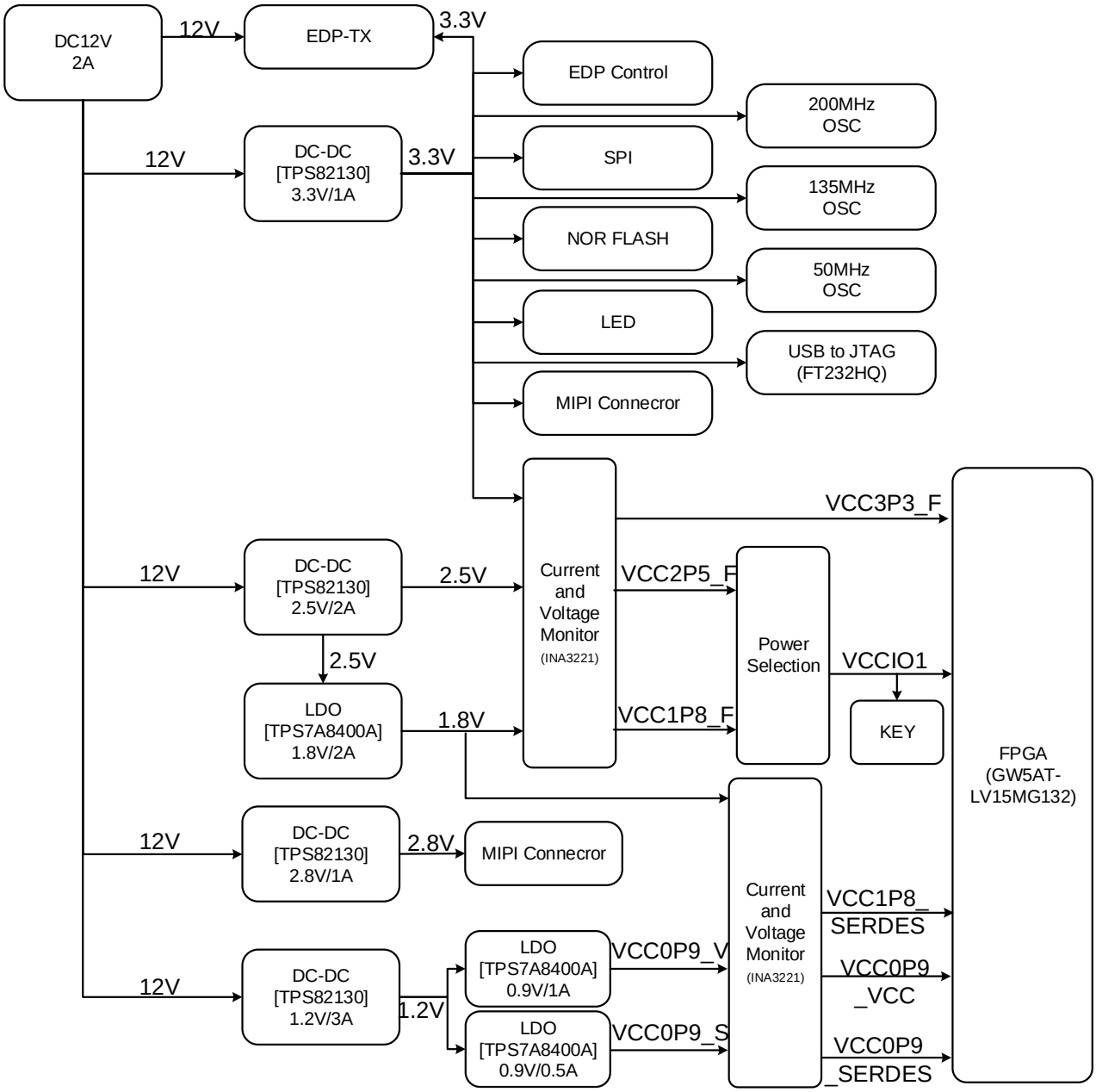
The development board needs to be powered by a 12V power adapter.

The input parameter of the adapter is AC 100-240V~50/60MHz 0.6A, and the output parameter is DC 12V 2A.

The input 12V power is regulated by the PMIC on the development board to generate 3.3V, 2.8V, 2.5V, 1.8V, 1.2V, and 0.9V power supplies.

3.2.2 Power Distribution

Figure 3-1 Power Distribution Diagram



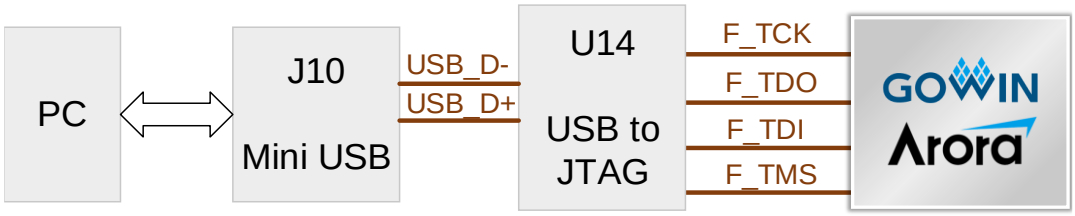
3.3 Download Module

3.3.1 Introduction

The development board includes a Mini USB-B download port (J10) designed to program the programs to external SPI FLASH or SRAM.

The download connection diagram is show in Figure 3-2.

Figure 3-2 Connection Diagram of Download



3.3.2 Pin Distribution

Table 3-1 JTAG Pin Distribution

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_TCK	G2	4	3.3V	JTAG signal
F_TDO	J2	4	3.3V	
F_TDI	J3	4	3.3V	
F_TMS	G3	4	3.3V	

3.4 Clock

3.4.1 Introduction

The development board includes multiple FPGA clock sources, including 1-channel 50 MHz single-ended clock, 1-channel 200 MHz differential clock, 1-channel 135 MHz differential clocks, and 1-channel SMA input differential clock. The 135MHz differential clock signal and SMA input differential clock signal are connected to FPGA's SerDes high-speed clock pin. The clock pin distribution is shown in Figure 3-3.

Figure 3-3 Clock Connection Diagram

3.4.2 Pin Distribution

Table 3-2 Clock Pin Distribution

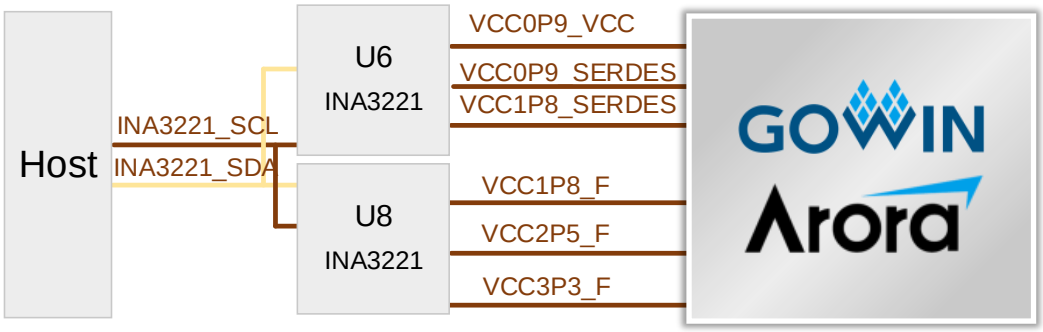
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
CLK_50M	H3	4	3.3V	50MHz single-ended clock
F_CLK_200M_P	K3	4	3.3V	200MHz differential clock
F_CLK_200M_N	K2	4	3.3V	200MHz differential clock
Q0_135MHz_P	A8	Q0	-	135MHz differential clock
Q0_135MHz_N	A7	Q0	-	135MHz differential clock
Q0_CLK_P	C10	Q0	-	SMA input differential clock
Q0_CLK_N	B10	Q0	-	SMA input differential clock

3.5 I2C Interface

3.5.1 Introduction

The development board includes 1-channel I2C interface as the host communication interface. The host can monitor the voltages of FPGA VCC, MIPI, VCCX, SerDes, and each BANK through this interface. The connection diagram of I2C interface is shown in Figure 3-4.

Figure 3-4 Connection Diagram of I2C Interface



3.5.2 Pin Distribution

Table 3-3 Pin Distribution of I2C Interface

J2 Pin No.	Signal Name	I/O Level	Description
1	INA3221_SCL	3.3V	Serial bus clock line
2	INA3221_SDA	3.3V	Serial bus data line
3	GND	-	GND

3.6 MIPI Interface

3.6.1 Introduction

The development board leads 1-channel MIPI CPHY hard core interface (3-trios data lanes), 1-channel MIPI DPHY hard core interface (4 data lanes + 1 clk lane), 1-channel MIPI DPHY soft core interface (8 data lanes + 2 clk lanes) from FPGA. The MIPI CPHY hard core interface, MIPI DPHY hard core interface, and five GPIOs are led to 80P AXK580147YG connector with 0.5mm pitch. The MIPI DPHY soft core interface is led to two 2*10P pin header with 2mm pitch. The MIPI DPHY soft core interfaces can be used as LVDS interfaces. The connection diagram of MIPI is as follows.

Figure 3-5 Connection Diagram of MIPI CPHY & DPHY Hard Core Interfaces

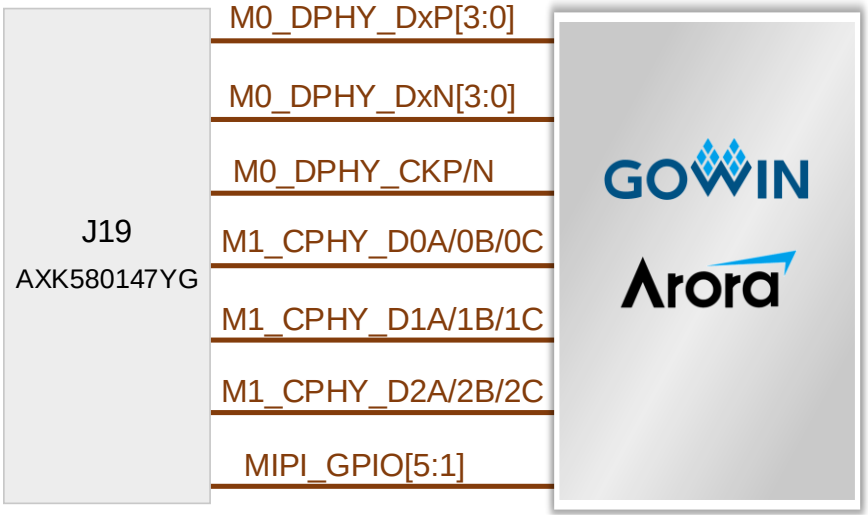


Figure 3-6 Connection Diagram of MIPI DPHY Soft Core/LVDS Interface

3.6.2 Pin Distribution

Table 3-4 Pin Distribution of MIPI CPHY & DPHY Hard core Interface

J19 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	M0_DPHY_D0N	P7	MIPI	-	MIPI DPHY data signal
2	VCC2P8	-	-	2.8V	Power
3	M0_DPHY_D0P	N7	MIPI	-	MIPI DPHY data signal
4	VCC2P8	-	-	2.8V	Power
5	GND	-	-	-	GND
6	GND	-	-	-	GND

J19 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
7	M0_DPHY_D1N	P6	MIPI	-	MIPI DPHY data signal
8	GND	-	-	-	GND
9	M0_DPHY_D1P	N6	MIPI	-	MIPI DPHY data signal
10	GND	-	-	-	GND
11	GND	-	-	-	GND
12	NC	-	-	-	Floating
13	M0_DPHY_CKN	P5	MIPI	-	MIPI DPHY clock signal
14	NC	-	-	-	Floating
15	M0_DPHY_CKP	N5	MIPI	-	MIPI DPHY clock signal
16	GND	-	-	-	GND
17	GND	-	-	-	GND
18	GND	-	-	-	GND
19	M0_DPHY_D2N	P4	MIPI	-	MIPI DPHY data signal
20	GND	-	-	-	GND
21	M0_DPHY_D2P	N4	MIPI	-	MIPI DPHY data signal
22	NC	-	-	-	Floating
23	GND	-	-	-	GND
24	NC	-	-	-	Floating
25	M0_DPHY_D3N	P3	MIPI	-	MIPI DPHY data signal
26	NC	-	-	-	Floating
27	M0_DPHY_D3P	N3	MIPI	-	MIPI DPHY data signal
28	GND	-	-	-	GND
29	GND	-	-	-	GND

J19 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
30	GND	-	-	-	GND
31	GND	-	-	-	GND
32	NC	-	-	-	Floating
33	GND	-	-	-	GND
34	NC	-	-	-	Floating
35	GND	-	-	-	GND
36	GND	-	-	-	GND
37	GND	-	-	-	GND
38	GND	-	-	-	GND
39	GND	-	-	-	GND
40	GND	-	-	-	GND
41	M1_CPHY_D1A	L1	MIPI	-	MIPI CPHY data signal
42	NC	-	-	-	Floating
43	M1_CPHY_D1B	K1	MIPI	-	MIPI CPHY data signal
44	NC	-	-	-	Floating
45	M1_CPHY_D1C	J1	MIPI	-	MIPI CPHY data signal
46	GND	-	-	-	GND
47	GND	-	-	-	GND
48	GND	-	-	-	GND
49	GND	-	-	-	GND
50	GND	-	-	-	GND
51	M1_CPHY_D0A	F2	MIPI	-	MIPI CPHY data signal
52	MIPI_GPIO1	M8	1	1.8V/2.5V	GPIO
53	M1_CPHY_D0B	F1	MIPI	-	MIPI CPHY data signal
54	MIPI_GPIO2	P14	1	1.8V/2.5V	GPIO

J19 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
55	M1_CPHY_D0C	G1	MIPI	-	MIPI CPHY data signal
56	MIPI_GPIO3	J12	1	1.8V/2.5V	GPIO
57	GND	-	-	-	GND
58	MIPI_GPIO4	H13	1	1.8V/2.5V	GPIO
59	GND	-	-	-	GND
60	GND	-	-	-	GND
61	M1_CPHY_D2A	C1	MIPI	-	MIPI CPHY data signal
62	MIPI_GPIO5	G13	1	1.8V/2.5V	GPIO
63	M1_CPHY_D2B	D2	MIPI	-	MIPI CPHY data signal
64	NC	-	-	-	Floating
65	M1_CPHY_D2C	D1	MIPI	-	MIPI CPHY data signal
66	GND	-	-	-	GND
67	GND	-	-	-	GND
68	NC	-	-	-	Floating
69	GND	-	-	-	GND
70	NC	-	-	-	Floating
71	GND	-	-	-	GND
72	GND	-	-	-	GND
73	GND	-	-	-	GND
74	GND	-	-	-	GND
75	GND	-	-	-	GND
76	VCC3P3	-	-	3.3V	Power
77	GND	-	-	-	GND
78	VCC3P3	-	-	3.3V	Power
79	GND	-	-	-	GND
80	VCC3P3	-	-	3.3V	Power

Table 3-5 Pin Distribution of MIPI DPHY Soft Core/LVDS Interface

J20 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	DPHY_LVDS_D3P	N8	1	1.8V/2.5V	MIPI/LVDS data
2	DPHY_LVDS_D3N	P8	1	1.8V/2.5V	MIPI/LVDS data
3	GND	-	-	-	GND
4	GND	-	-	-	GND
5	DPHY_LVDS_D2P	P10	1	1.8V/2.5V	MIPI/LVDS data
6	DPHY_LVDS_D2N	N10	1	1.8V/2.5V	MIPI/LVDS data
7	GND	-	-	-	GND
8	GND	-	-	-	GND
9	DPHY_LVDS_CK0P	N11	1	1.8V/2.5V	MIPI/LVDS clock
10	DPHY_LVDS_CK0N	P11	1	1.8V/2.5V	MIPI/LVDS clock
11	GND	-	-	-	GND
12	GND	-	-	-	GND
13	DPHY_LVDS_D1P	N12	1	1.8V/2.5V	MIPI/LVDS data
14	DPHY_LVDS_D1N	P12	1	1.8V/2.5V	MIPI/LVDS data
15	GND	-	-	-	GND
16	GND	-	-	-	GND
17	DPHY_LVDS_D0P	P13	1	1.8V/2.5V	MIPI/LVDS data
18	DPHY_LVDS_D0N	N13	1	1.8V/2.5V	MIPI/LVDS data
19	GND	-	-	-	GND
20	GND	-	-	-	GND

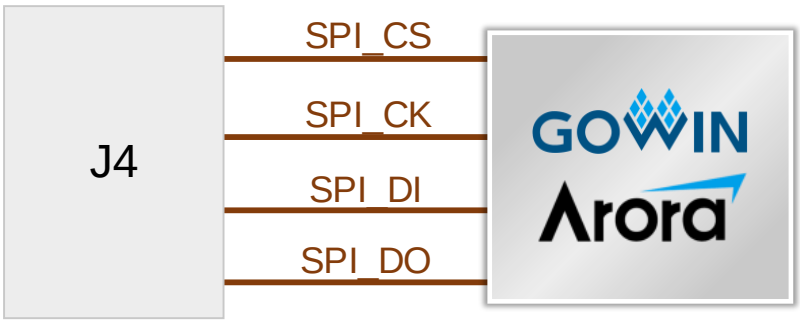
J21 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	DPHY_LVDS_D4P	D13	1	1.8V/2.5V	MIPI/LVDS data
2	DPHY_LVDS_D4N	C13	1	1.8V/2.5V	MIPI/LVDS data
3	GND	-	-	-	GND
4	GND	-	-	-	GND
5	DPHY_LVDS_D5P	D14	1	1.8V/2.5V	MIPI/LVDS data
6	DPHY_LVDS_D5N	C14	1	1.8V/2.5V	MIPI/LVDS data
7	GND	-	-	-	GND
8	GND	-	-	-	GND
9	DPHY_LVDS_CK1P	F13	1	1.8V/2.5V	MIPI/LVDS clock
10	DPHY_LVDS_CK1N	E13	1	1.8V/2.5V	MIPI/LVDS clock
11	GND	-	-	-	GND
12	GND	-	-	-	GND
13	DPHY_LVDS_D6P	J13	1	1.8V/2.5V	MIPI/LVDS data
14	DPHY_LVDS_D6N	J14	1	1.8V/2.5V	MIPI/LVDS data
15	GND	-	-	-	GND
16	GND	-	-	-	GND
17	DPHY_LVDS_D7P	F14	1	1.8V/2.5V	MIPI/LVDS data
18	DPHY_LVDS_D7N	E14	1	1.8V/2.5V	MIPI/LVDS data
19	GND	-	-	-	GND
20	GND	-	-	-	GND

3.7 SPI Interface

3.7.1 Introduction

The development board introduces an SPI interface for remote upgrades. The connection diagram is shown in Figure 3-7.

Figure 3-7 Connection Diagram of SPI Interface



3.7.2 Pin Distribution

Table 3-6 Pin Distribution of SPI Interface

J4 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	GND	-	-	-	GND
2	SPI_DO	P1	3	3.3V	Data output
3	SPI_DI	P2	3	3.3V	Data input
4	SPI_CK	M1	3	3.3V	Clock signal
5	SPI_CS	M2	3	3.3V	Chip select signal

3.8 EDP Interface

3.8.1 Introduction

The development board leads 1-channel EDP-TX interface and 1-channel EDP-RX interface. The EDP control signal is led externally through J8 interface. The connection diagram of EDP interface is shown in Figure 3-8.

Figure 3-8 Connection Diagram of EDP-TX Interface

Figure 3-9 Connection Diagram of EDP-RX Interface

3.8.2 Pin Distribution

Table 3-7 Pin Distribution of EDP-TX Interface

J6 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	EDP_TX_G_Sync	-	-	-	GPU Synchronization
2	GND	-	-	-	GND
3	EDP_TX3_N	B12	Q0	-	Transmit data
4	EDP_TX3_P	C12	Q0	-	Transmit data
5	GND	-	-	-	GND
6	EDP_TX2_N	C8	Q0	-	Transmit data
7	EDP_TX2_P	B8	Q0	-	Transmit data
8	GND	-	-	-	GND
9	EDP_TX1_N	C6	Q0	-	Transmit data
10	EDP_TX1_P	B6	Q0	-	Transmit data
11	GND	-	-	-	GND
12	EDP_TX0_N	C3	Q0	-	Transmit data
13	EDP_TX0_P	B3	Q0	-	Transmit data

J6 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
14	GND	-	-	-	GND
15	EDP_TX_AUX_P	N9	1	1.8V/2.5V	Auxiliary channel
16	EDP_TX_AUX_N	P9	1	1.8V/2.5V	Auxiliary channel
17	GND	-	-	-	GND
18	VCC3P3	-	-	3.3V	Power
19	VCC3P3	-	-	3.3V	Power
20	VCC3P3	-	-	3.3V	Power
21	VCC3P3	-	-	3.3V	Power
22	EDP_TX_BIST	-	-	-	Self-test enable
23	GND	-	-	-	GND
24	GND	-	-	-	GND
25	GND	-	-	-	GND
26	GND	-	-	-	GND
27	EDP_TX_HPD	-	-	-	Hot plug detect
28	GND	-	-	-	GND
29	GND	-	-	-	GND
30	GND	-	-	-	GND
31	GND	-	-	-	GND
32	EDP_TX_BL_EN	-	-	-	Backlight enable
33	EDP_TX_BL_PWM	-	-	-	Backlight PWM control
34	NC	-	-	-	Floating
35	NC	-	-	-	Floating
36	VCC12P0	-	-	12V	Power
37	VCC12P0	-	-	12V	Power
38	VCC12P0	-	-	12V	Power
39	VCC12P0	-	-	12V	Power
40	NC	-	-	-	Floating

Table 3-8 Pin Distribution of EDP-TX Interface

J7 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	EDP_RX_G_Sync	-	-	-	GPU Synchronization
2	GND	-	-	-	GND
3	EDP_RX3_N	A14	Q0	-	Transmit data
4	EDP_RX3_P	A13	Q0	-	Transmit data
5	GND	-	-	-	GND
6	EDP_RX2_N	A11	Q0	-	Transmit data
7	EDP_RX2_P	A10	Q0	-	Transmit data
8	GND	-	-	-	GND
9	EDP_RX1_N	A5	Q0	-	Transmit data
10	EDP_RX1_P	A4	Q0	-	Transmit data
11	GND	-	-	-	GND
12	EDP_RX0_N	A1	Q0	-	Transmit data
13	EDP_RX0_P	A2	Q0	-	Transmit data
14	GND	-	-	-	GND
15	EDP_RX_AUX_P	H14	1	1.8V/2.5V	Auxiliary channel
16	EDP_RX_AUX_N	G14	1	1.8V/2.5V	Auxiliary channel
17	GND	-	-	-	GND
18	NC	-	-	-	Floating
19	NC	-	-	-	Floating
20	NC	-	-	-	Floating
21	NC	-	-	-	Floating
22	EDP_RX_BIST	-	-	-	Self-test enable
23	GND	-	-	-	GND
24	GND	-	-	-	GND
25	GND	-	-	-	GND
26	GND	-	-	-	GND
27	EDP_RX_HPD	-	-	-	Hot plug detect

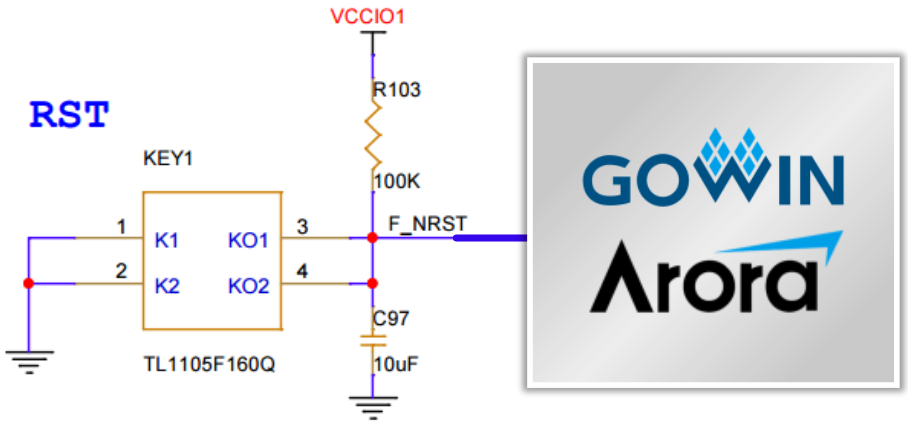
J7 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
28	NC	-	-	-	Floating
29	NC	-	-	-	Floating
30	NC	-	-	-	Floating
31	NC	-	-	-	Floating
32	NC	-	-	-	Floating
33	NC	-	-	-	Floating
34	NC	-	-	-	Floating
35	NC	-	-	-	Floating
36	NC	-	-	-	Floating
37	NC	-	-	-	Floating
38	NC	-	-	-	Floating
39	NC	-	-	-	Floating
40	NC	-	-	-	Floating

3.9 Key & LED

3.9.1 Introduction

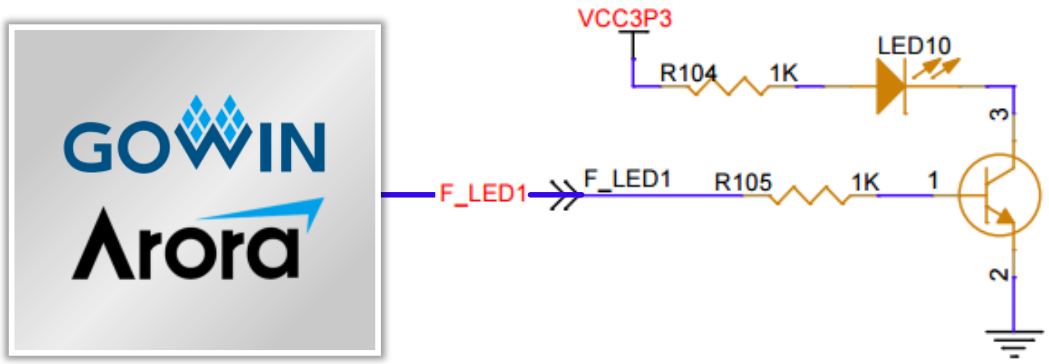
The development board includes one reset key , which is connected to the general IO of FPGA BANK1. The corresponding IO input voltage of the FPGA is low when the key is pressed while high when the key is not pressed. The connection diagram is shown in Figure 3-10.

Figure 3-10 Connection Diagram of Key



The development board includes one user LED. The user LED is connected to the IO of FPGA BANK4 and can be switched on and off via the program. When the IO voltage is high, it will be on; When the IO voltage is low, it will be off . The connection diagram is shown in Figure 3-11.

Figure 3-11 Connection Diagram of LED



3.9.2 Pin Distribution

Table 3-9 Pin Distribution of Key

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_NRST	N14	1	1.8V/2.5V	Reset Key

Table 3-10 Pin Distribution of Indicator

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_LED1	H2	4	3.3V	LED indicator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