




DK_DP_GW5AT-LV60UG225_V1.0

User Guide

DBUG1274-1.0.1E, 02/07/2025

Copyright © 2025 Guangdong Gowin Semiconductor Corporation. All Rights Reserved.

 is the trademark of Guangdong Gowin Semiconductor Corporation and is registered in China, the U.S. Patent and Trademark Office, and other countries. All other words and logos identified as trademarks or service marks are the property of their respective holders. No part of this document may be reproduced or transmitted in any form or by any means, electronic, mechanical, photocopying, recording or otherwise, without the prior written consent of GOWINSEMI.

Disclaimer

GOWINSEMI assumes no liability and provides no warranty (either expressed or implied) and is not responsible for any damage incurred to your hardware, software, data, or property resulting from usage of the materials or intellectual property except as outlined in the GOWINSEMI Terms and Conditions of Sale. GOWINSEMI may make changes to this document at any time without prior notice. Anyone relying on this documentation should contact GOWINSEMI for the current documentation and errata.

Revision History

Date	Version	Description
10/18/2024	1.0E	Initial version published.
02/07/2025	1.0.1E	The bank information in “Table 3-5 Pin Distribution of DP-TX Interface” and “Table 3-6 Pin Distribution of DP-RX Interface” updated.

Contents

Contents	iv
List of Figures	vi
List of Tables	vii
1 About This Guide.....	1
1.1 Purpose	1
1.2 Related Documents	1
1.3 Terminology and Abbreviations.....	2
1.4 Support and Feedback	2
2 Development Board Introduction.....	3
2.1 Overview	3
2.2 A Development Board Kit.....	4
2.3 PCB Components	5
2.4 System Block Diagram	5
2.5 Features.....	6
3 Development Board Circuit	7
3.1 FPGA	7
3.2 Power Supply for more details.....	7
3.2.1 Introduction	7
3.2.2 Power Distribution.....	8
3.3 Download Module	9
3.3.1 Introduction	9
3.3.2 Pin Distribution.....	9
3.4 Clock.....	9
3.4.1 Introduction	9
3.4.2 Pin Distribution.....	10

3.5 DDR3	11
3.5.1 Introduction	11
3.5.2 Pin Distribution.....	12
3.6 DP Interface	14
3.6.1 Introduction	14
3.6.2 Pin Distribution.....	15
3.7 MIPI Interface	17
3.7.1 Introduction	17
3.7.2 Pin Distribution.....	18
3.8 I2C Interface	22
3.8.1 Introduction	22
3.8.2 Pin Distribution.....	23
3.9 Key & LED	23
3.9.1 Introduction	23
3.9.2 Pin Distribution.....	24
3.10 GPIO	25
3.10.1 Introduction	25
3.10.2 Pin Distribution.....	25

List of Figures

Figure 2-1 DK_DP_GW5AT-LV60UG225_V1.0 Development Board.....	3
Figure 2-2 A Development Board Kit	4
Figure 2-3 PCB Components.....	5
Figure 2-4 System Block Diagram	5
Figure 3-1 Power Distribution Diagram	8
Figure 3-2 Connection Diagram of Download	9
Figure 3-3 Clock Connection Diagram	10
Figure 3-4 Hardware Connection Diagram of DDR3.....	11
Figure 3-5 Connection Diagram of DP-TX Interface	14
Figure 3-6 Connection Diagram of DP-RX Interface	14
Figure 3-7 Connection Diagram of MIPI CPHY & DPHY Hard Core Interfaces	17
Figure 3-8 Connection Diagram of MIPI DPHY Soft Core Interface.....	17
Figure 3-9 Connection Diagram of I2C Interface.....	22
Figure 3-10 Connection Diagram of Key	23
Figure 3-11 Connection Diagram of LED.....	24
Figure 3-12 Connection Diagram of GPIO	25

List of Tables

Table 1-1 Terminology and Abbreviations	2
Table 3-1 JTAG Pin Distribution	9
Table 3-2 Clock Pin Distribution	10
Table 3-3 DDR3 Configuration	11
Table 3-4 DDR3 Pin Distribution	12
Table 3-5 Pin Distribution of DP-TX Interface	15
Table 3-6 Pin Distribution of DP-RX Interface	15
Table 3-7 Pin Distribution of MIPI CPHY & DPHY Hard core Interface	18
Table 3-8 Pin Distribution of MIPI DPHY Soft Core Interface	21
Table 3-9 J21 Pin Distribution of I2C-1 Interface	23
Table 3-10 Pin Distribution of Key	24
Table 3-11 Pin Distribution of LED	24
Table 3-12 Pin Distribution of GPIO Interface	25

1 About This Guide

1.1 Purpose

The DK_DP_GW5AT-LV60UG225_V1.0 development board (hereinafter referred to as “the development board”) user guide consists of following three parts:

- A brief introduction to the features of the development board
- An introduction to the development board system architecture and hardware resources
- An introduction to the hardware circuits, functions and pin distribution

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [UG1222, GW5AT-60 Pinout](#)
- [UG983, GW5AT series of FPGA Products Package and Pinout User Guide](#)
- [UG718, Arora V 60K FPGA Products Programming and Configuration User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable Input/Output
MIPI	Mobile Industry Processor Interface
DP	Display Port
DDR	Double Data Rate
JTAG	Joint Test Action Group
I2C	Inter-Integrated Circuit
LDO	Low Dropout Regulator

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

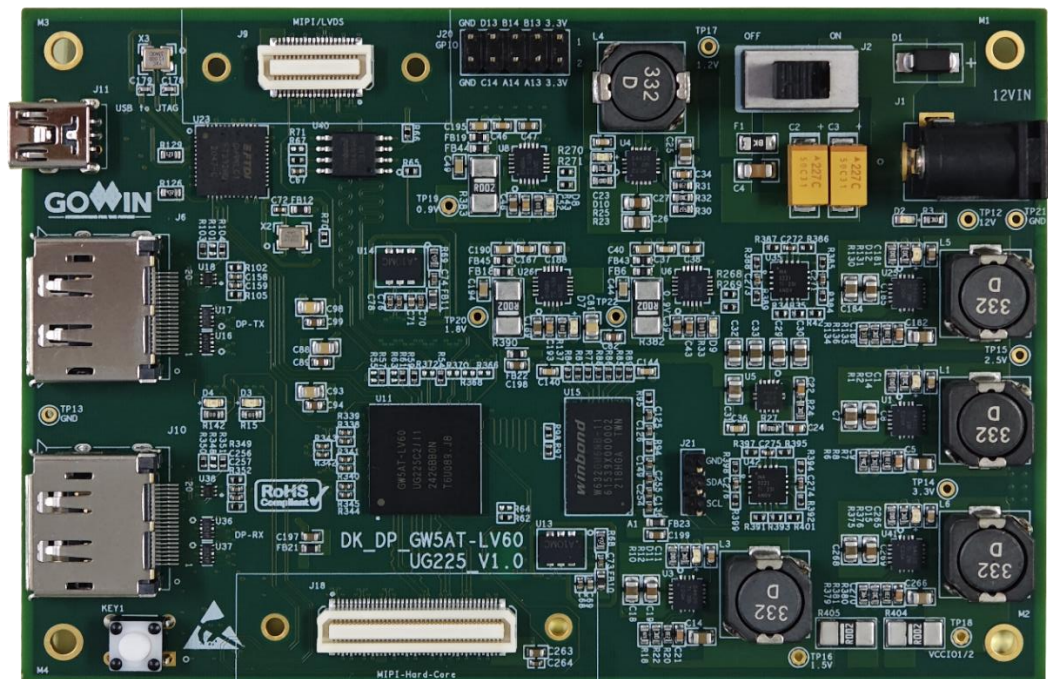
Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Development Board Introduction

2.1 Overview

Figure 2-1 DK_DP_GW5AT-LV60UG225_V1.0 Development Board



Gowin GW5AT series of FPGA products are the 5 series products of Arora family, with abundant internal resources, high-performance DSP with a new architecture that supports AI operations, high-speed LVDS interface and abundant BSRAM resources. At the same time, it integrates self-developed DDR3, and provides a variety of packages. It is suitable for applications such as low power, high performance and compatibility design.

DK_DP_GW5AT-LV60UG225_V1.0 development board can be applied to DDR3 high-speed storage, DP and MIPI high-speed

communication, integrates DP-RX, DP-TX, MIPI CPHY, MIPI DPHY, and GPIO interfaces, supporting FPGA's MIPI C-PHY and MIPI D-PHY function evaluation, hardware verification, and software learning and debugging, etc.

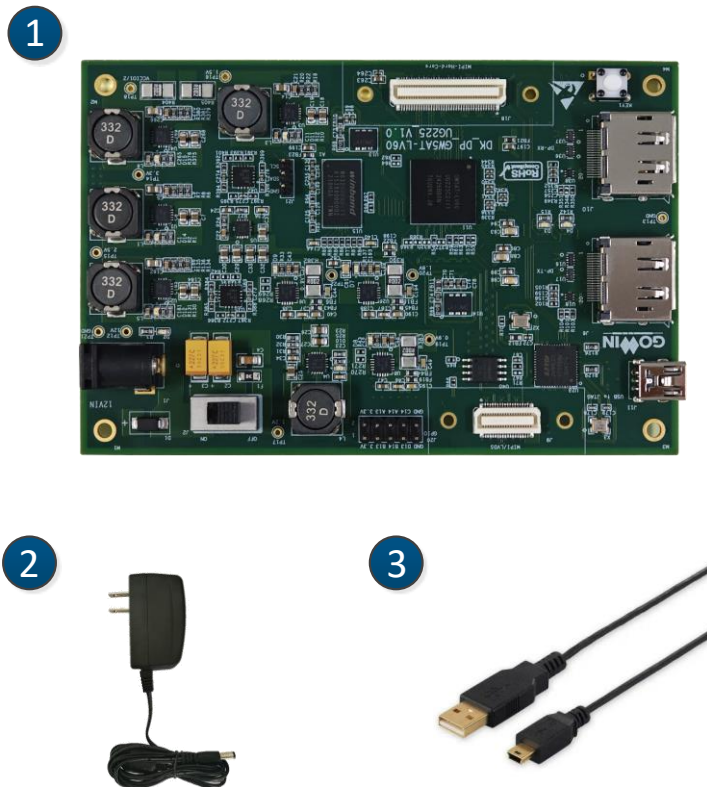
The development board adopts Gowin GW5AT-LV60UG225 FPGA device. For the internal resources of the chip, see [DS981, GW5AT series of FPGA Products Data Sheet](#).

2.2 A Development Board Kit

The development board kit includes the following items:

1. DK_DP_GW5AT-LV60UG225_V1.0 development board
2. 12V power (Input: AC 100-240V~50/60Hz 0.6A, output: DC12V 2A)
3. Mini USB-B Cable

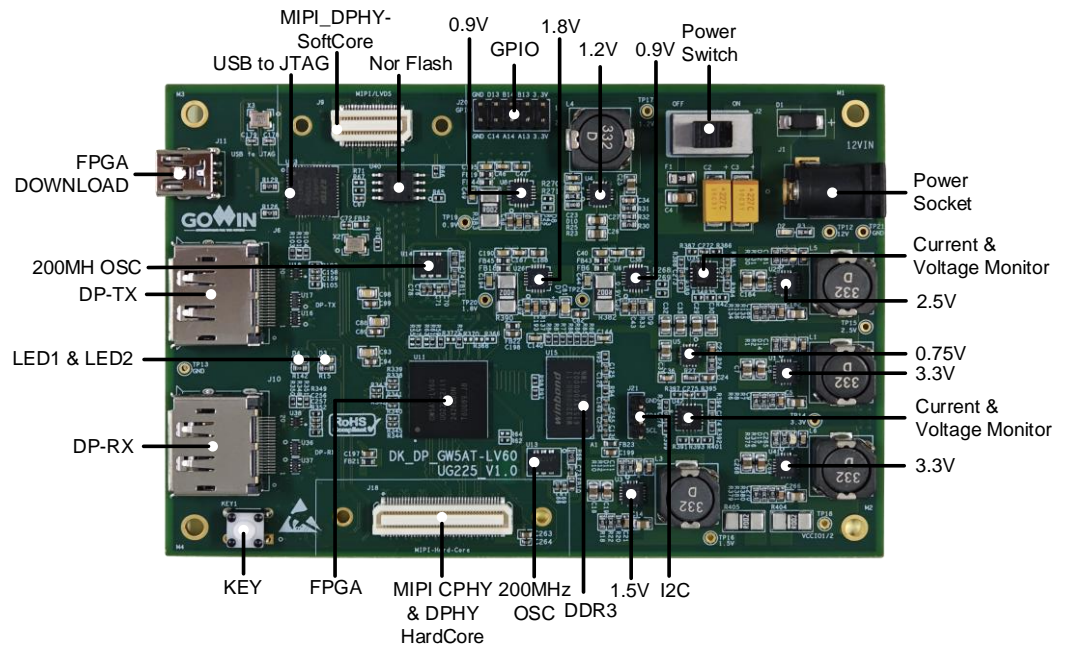
Figure 2-2 A Development Board Kit



- ① DK_DP_GW5AT-LV60UG225_V1.0 development board
- ② 12V power supply adapter
- ③ Mini USB-B Cable

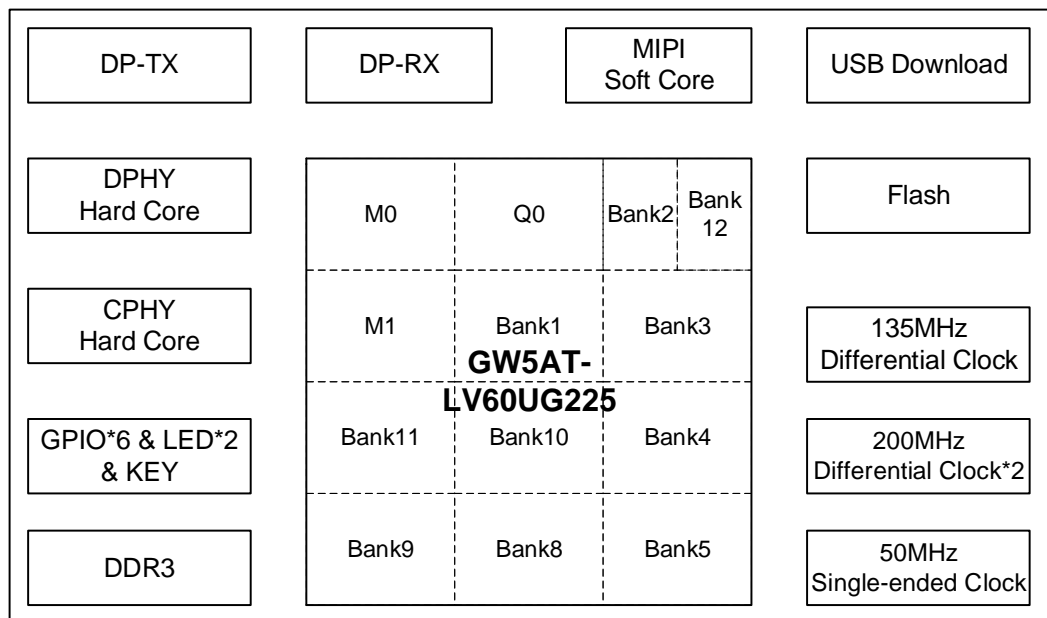
2.3 PCB Components

Figure 2-3 PCB Components



2.4 System Block Diagram

Figure 2-4 System Block Diagram



2.5 Features

The key features are as follows:

- **FPGA Device**
 - Gowin GW5AT-LV60UG225 FPGA
 - Max. user I/O: 113
- **Download and Boot**
 - Integrate USB download circuit on the board, download through Mini USB-B interface
 - External SPI Flash Boot
- **Power**
 - External DC12V/2A Power
 - The Power light is on after power on.
 - The board generates 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, 0.9V, 0.75V power.
- **Clock system**
 - 1-channel 50MHz clock
 - 1-channel 135MHz differential clock
 - 2-channel 200MHz differential clocks
- **Memory device**
 - 2Gbit DDR3 SDRAM
 - 64Mbit NOR Flash
- **DP Interface**
 - 1-channel DP-TX interface
 - 1-channel DP-RX interface
 - Display Port connector
- **MIPI Interface**
 - 1-channel CPHY hard core interface, including 3-trios data lanes
 - 1-channel DPHY hard core interface, including 4 data lanes + 1 clk lane
 - 1-channel DPHY soft core interface, including 8 data lanes + 1 clk lane
- **I2C Interface**
 - 1-channel I2C interface
- **Key & Indicator**
 - 1 Key
 - 2 LED indicators
- **GPIO**
 - 14 GPIOs with 3.3V power level

3 Development Board Circuit

3.1 FPGA

Overview

For the resources of GW5AT series of FPGA Products, refer to [DS981, GW5AT series of FPGA Products Data Sheet](#).

I/O BANK Description

For the I/O BANK, package, and pinout information, see [UG983, GW5AT series of FPGA Products Package and Pinout User Guide](#).

3.2 Power Supply for more details.

3.2.1 Introduction

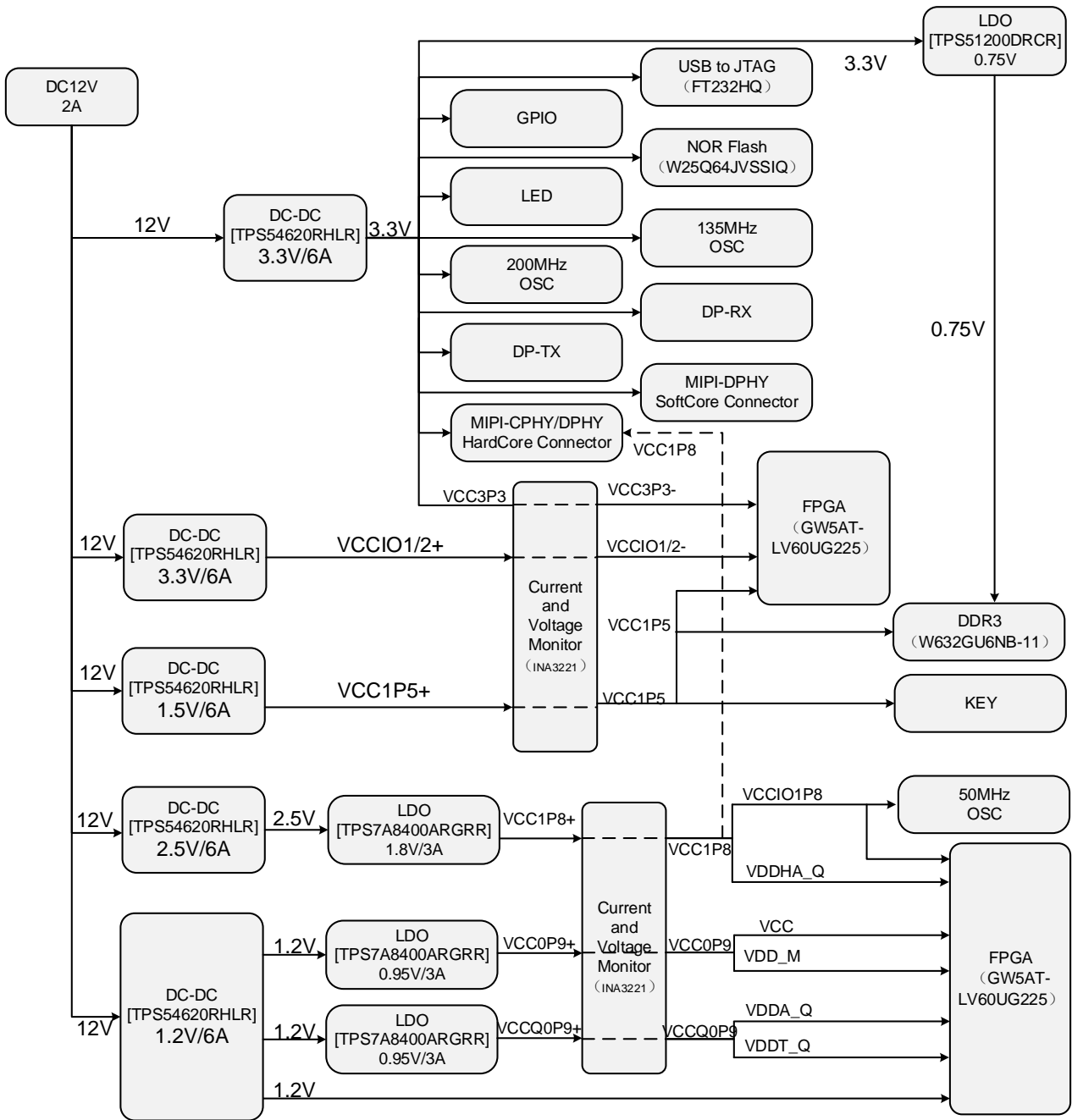
The development board needs to be powered by a 12V power adapter.

The input parameter of the adapter is AC 100-240V~50/60MHz 0.6A, and the output parameter is DC 12V 2A.

The input 12V power is regulated by the PMIC on the development board to generate 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, 0.9V, and 0.75V power supplies.

3.2.2 Power Distribution

Figure 3-1 Power Distribution Diagram



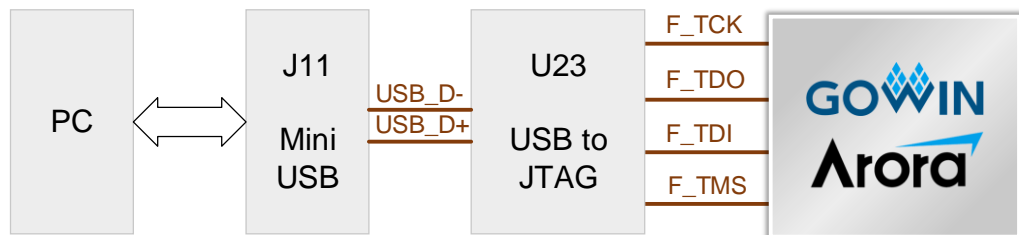
3.3 Download Module

3.3.1 Introduction

The development board has a Mini USB-B download port (J11) designed to program the programs to external SPI FLASH or download them to SRAM.

The download connection diagram is show in Figure 3-2.

Figure 3-2 Connection Diagram of Download



3.3.2 Pin Distribution

Table 3-1 JTAG Pin Distribution

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_TCK	C15	12	3.3V	JTAG signal
F_TDO	D15	12	3.3V	
F_TDI	B15	12	3.3V	
F_TMS	E15	12	3.3V	

3.4 Clock

3.4.1 Introduction

The development board provides multiple FPGA clock sources, including 1-channel 50 MHz single-ended clock, 1-channel 135 MHz differential clock, and 2-channel 200 MHz differential clocks. Among them, the 135MHz differential clock and one of the 200MHz differential clocks are connected the FPGA SerDes high-speed clock pins. The clock pin distribution is as shown in Figure 3-3.

Figure 3-3 Clock Connection Diagram



3.4.2 Pin Distribution

Table 3-2 Clock Pin Distribution

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_CLK_50M	H5	10	1.8V	50MHz single-ended clock
F_CLK_200M_P	K5	10	1.8V	200MHz differential clock
F_CLK_200M_N	J5	10	1.8V	200MHz differential clock
Q0_135MHz_P	B5	Q0	-	135M differential clock
Q0_135MHz_N	A5	Q0	-	135M differential clock
Q0_200MHz_P	D10	Q0	-	200MHz differential clock
Q0_200MHz_N	C10	Q0	-	200MHz differential clock

3.5 DDR3

3.5.1 Introduction

The development board includes one 2 Gbit DDR3 chip. The signal of DDR3 chip is connected to the BANK8 and BANK9 of FPGA. The specific configurations of DDR3 are as shown in Table 3-3.

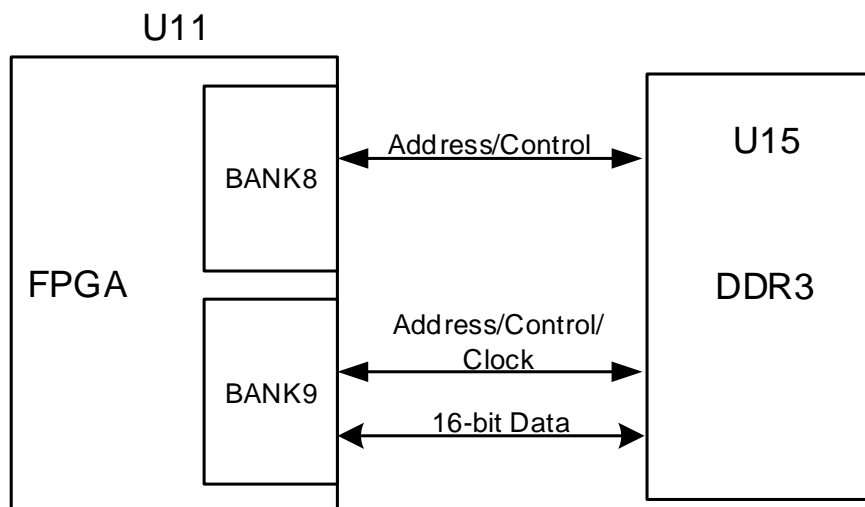
Table 3-3 DDR3 Configuration

Designator	Capacity
U15	128M x 16bit

DDR3 hardware design requires strict consideration of signal integrity. In the design of circuit and PCB, matching resistor/termination resistor, impedance control and equal length control of traces have been fully considered to ensure DDR3 works stably at high speed.

The hardware connection diagram of DDR3 is as show in Figure 3-4.

Figure 3-4 Hardware Connection Diagram of DDR3



3.5.2 Pin Distribution

Table 3-4 DDR3 Pin Distribution

Signal Name	FPGA (U1) Pin No.	BANK	I/O Level	Description
DDR3_A0	L7	9	1.5V	Address
DDR3_A1	M11	8	1.5V	Address
DDR3_A2	N11	8	1.5V	Address
DDR3_A3	N10	8	1.5V	Address
DDR3_A4	L10	8	1.5V	Address
DDR3_A5	M10	8	1.5V	Address
DDR3_A6	L8	9	1.5V	Address
DDR3_A7	N12	8	1.5V	Address
DDR3_A8	M9	9	1.5V	Address
DDR3_A9	R13	8	1.5V	Address
DDR3_A10	P13	8	1.5V	Address
DDR3_A11	K10	8	1.5V	Address
DDR3_A12	R14	8	1.5V	Address
DDR3_A13	P9	9	1.5V	Address
DDR3_BA0	N2	9	1.5V	Bank address
DDR3_BA1	P11	8	1.5V	Bank address
DDR3_BA2	L6	9	1.5V	Bank address
DDR3_CS#	P2	9	1.5V	Chip select
DDR3_CAS#	R2	9	1.5V	Column address strobe
DDR3_CKE	R12	8	1.5V	Clock Enable
DDR3_ODT	N1	9	1.5V	On-Die termination enable
DDR3_RAS#	N7	9	1.5V	Row address strobe
DDR3_RESET	N9	9	1.5V	Reset
DDR3_WE#	P1	9	1.5V	Write enable

Signal Name	FPGA (U1) Pin No.	BANK	I/O Level	Description
DDR3_CLK0_P	N8	9	1.5V	Differential clock
DDR3_CLK0_N	M8	9	1.5V	Differential clock
DDR3_DQ0	M6	9	1.5V	Data
DDR3_DQ1	R4	9	1.5V	Data
DDR3_DQ2	M5	9	1.5V	Data
DDR3_DQ3	R6	9	1.5V	Data
DDR3_DQ4	L5	9	1.5V	Data
DDR3_DQ5	R7	9	1.5V	Data
DDR3_DQ6	N6	9	1.5V	Data
DDR3_DQ7	P7	9	1.5V	Data
DDR3_DQ8	M4	9	1.5V	Data
DDR3_DQ9	M1	9	1.5V	Data
DDR3_DQ10	N5	9	1.5V	Data
DDR3_DQ11	L1	9	1.5V	Data
DDR3_DQ12	N4	9	1.5V	Data
DDR3_DQ13	L3	9	1.5V	Data
DDR3_DQ14	P5	9	1.5V	Data
DDR3_DQ15	L2	9	1.5V	Data
DDR3_LDM0	R5	9	1.5V	Data input mask
DDR3_UDM0	M3	9	1.5V	Data input mask
DDR3_LDQS0_P	R8	9	1.5V	Data Clock
DDR3_LDQS0_N	R9	9	1.5V	Data Clock
DDR3_UDQS0_P	R3	9	1.5V	Data Clock
DDR3_UDQS0_N	P3	9	1.5V	Data Clock

3.6 DP Interface

3.6.1 Introduction

The development board provides 1-lane DP-TX interface and 1-lane DP-RX interface. The connection diagram of the DP interfaces is as follows.

Figure 3-5 Connection Diagram of DP-TX Interface

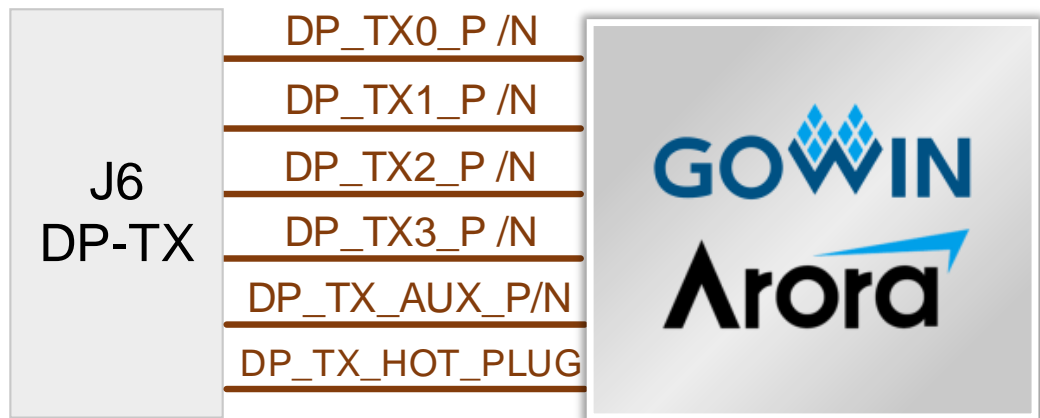


Figure 3-6 Connection Diagram of DP-RX Interface



3.6.2 Pin Distribution

Table 3-5 Pin Distribution of DP-TX Interface

J6 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	DP_TX0_P	D4	Q0	-	DP Data Transmit
2	GND	-	-	-	GND
3	DP_TX0_N	C4	Q0	-	DP Data Transmit
4	DP_TX1_P	D6	Q0	-	DP Data Transmit
5	GND	-	-	-	GND
6	DP_TX1_N	C6	Q0	-	DP Data Transmit
7	DP_TX2_P	D8	Q0	-	DP Data Transmit
8	GND	-	-	-	GND
9	DP_TX2_N	C8	Q0	-	DP Data Transmit
10	DP_TX3_P	D12	Q0	-	DP Data Transmit
11	GND	-	-	-	GND
12	DP_TX3_N	C12	Q0	-	DP Data Transmit
13	GND	-	-	-	GND
14	GND	-	-	-	GND
15	DP_TX_P	F5	11	1.8V	Auxiliary channel
16	GND	-	-	-	GND
17	DP_TX_N	G5	11	1.8V	Auxiliary channel
18	DP_HPD_T	F11	3	3.3V	Hot Plug Detect
19	NC	-	-	-	Floating
20	VCC3P3	-	-	3.3V	Power

Table 3-6 Pin Distribution of DP-RX Interface

J10 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	DP_RX3_N	A11	Q0	-	DP Data Receive
2	GND	-	-	-	GND
3	DP_RX3_P	B11	Q0	-	DP Data Receive

J10 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
4	DP_RX2_N	A9	Q0	-	DP Data Receive
5	GND	-	-	-	GND
6	DP_RX2_P	B9	Q0	-	DP Data Receive
7	DP_RX1_N	A7	Q0	-	DP Data Receive
8	GND	-	-	-	GND
9	DP_RX1_P	B7	Q0	-	DP Data Receive
10	DP_RX0_N	A3	Q0	-	DP Data Receive
11	GND	-	-	-	GND
12	DP_RX0_P	B3	Q0	-	DP Data Receive
13	GND	-	-	-	GND
14	GND	-	-	-	GND
15	DP_RX_P	K4	11	1.8V	Auxiliary channel
16	GND	-	-	-	GND
17	DP_RX_N	K3	11	1.8V	Auxiliary channel
18	DP_HPD_R	G11	3	3.3V	Hot Plug Detect
19	NC	-	-	-	Floating
20	VCC3P3	-	-	3.3V	Power

3.7 MIPI Interface

3.7.1 Introduction

The development board includes 1-channel MIPI CPHY hard core interface (3-trios data lanes), 1-channel MIPI DPHY soft core interface (8 data lanes + 1 clk lane), 1-channel MIPI DPHY hard core interface (4 data lanes + 1 clk lane). The MIPI CPHY hard core interface, MIPI DPHY hard core interface, and eight 3.3V GPIOs are led to 80P AXK580147YG connector with 0.5mm pitch. The MIPI DPHY soft core interface and RST signal are led to 40P AXK540147YG connector with 0.5mm pitch. The connection diagram is as follows.

Figure 3-7 Connection Diagram of MIPI CPHY & DPHY Hard Core Interfaces

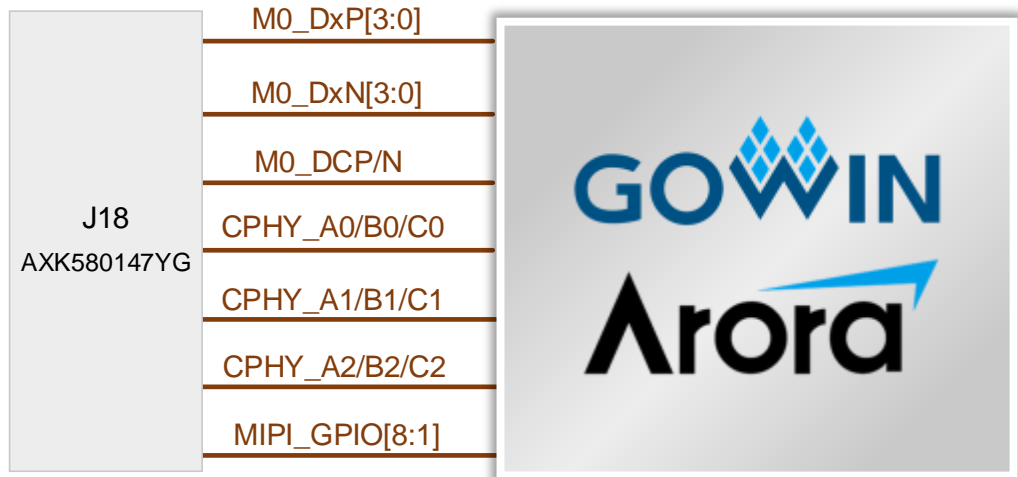


Figure 3-8 Connection Diagram of MIPI DPHY Soft Core Interface



3.7.2 Pin Distribution

Table 3-7 Pin Distribution of MIPI CPHY & DPHY Hard core Interface

J18 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	M0_D3N	C2	MIPI	-	MIPI DPHY data signal
2	NC	-	-	-	Floating
3	M0_D3P	C1	MIPI	-	MIPI DPHY data signal
4	NC	-	-	-	Floating
5	GND	-	-	-	GND
6	GND	-	-	-	GND
7	M0_D2N	E3	MIPI	-	MIPI DPHY data signal
8	GND	-	-	-	GND
9	M0_D2P	F4	MIPI	-	MIPI DPHY data signal
10	GND	-	-	-	GND
11	GND	-	-	-	GND
12	NC	-	-	-	Floating
13	M0_DCN	F3	MIPI	-	MIPI DPHY clock signal
14	NC	-	-	-	Floating
15	M0_DCP	G3	MIPI	-	MIPI DPHY clock signal
16	GND	-	-	-	GND
17	GND	-	-	-	GND
18	GND	-	-	-	GND
19	M0_D1N	H3	MIPI	-	MIPI DPHY data signal
20	GND	-	-	-	GND
21	M0_D1P	H4	MIPI	-	MIPI DPHY data signal
22	VCC1P8	-	-	1.8V	Power
23	GND	-	-	-	GND
24	VCC1P8	-	-	1.8V	Power
25	M0_D0N	J3	MIPI	-	MIPI DPHY data signal

J18 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
26	VCC1P8	-	-	1.8V	Power
27	M0_D0P	J4	MIPI	-	MIPI DPHY data signal
28	GND	-	-	-	GND
29	GND	-	-	-	GND
30	GND	-	-	-	GND
31	GND	-	-	-	GND
32	NC	-	-	-	Floating
33	GND	-	-	-	GND
34	NC	-	-	-	Floating
35	GND	-	-	-	GND
36	GND	-	-	-	GND
37	GND	-	-	-	GND
38	GND	-	-	-	GND
39	GND	-	-	-	GND
40	GND	-	-	-	GND
41	M1_D0A	D1	MIPI	-	MIPI CPHY data signal
42	NC	-	-	-	Floating
43	M1_D0B	E2	MIPI	-	MIPI CPHY data signal
44	NC	-	-	-	Floating
45	M1_D0C	E1	MIPI	-	MIPI CPHY data signal
46	GND	-	-	-	GND
47	GND	-	-	-	GND
48	GND	-	-	-	GND
49	GND	-	-	-	GND
50	GND	-	-	-	GND
51	M1_D1A	F1	MIPI	-	MIPI CPHY data signal
52	MIPI_GPIO1	E8	1	3.3V	GPIO reserved
53	M1_D1B	G1	MIPI	-	MIPI CPHY data signal
54	MIPI_GPIO2	E7	1	3.3V	GPIO reserved

J18 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
55	M1_D1C	G2	MIPI	-	MIPI CPHY data signal
56	MIPI_GPIO3	E6	1	3.3V	GPIO reserved
57	GND	-	-	-	GND
58	MIPI_GPIO4	E5	1	3.3V	GPIO reserved
59	GND	-	-	-	GND
60	GND	-	-	-	GND
61	M1_D2A	H1	MIPI	-	MIPI CPHY data signal
62	MIPI_GPIO5	E10	1	3.3V	GPIO reserved
63	M1_D2B	J1	MIPI	-	MIPI CPHY data signal
64	MIPI_GPIO6	F10	1	3.3V	GPIO reserved
65	M1_D2C	J2	MIPI	-	MIPI CPHY data signal
66	GND	-	-	-	GND
67	GND	-	-	-	GND
68	MIPI_GPIO7	E9	1	3.3V	GPIO reserved
69	GND	-	-	-	GND
70	MIPI_GPIO8	F8	1	3.3V	GPIO reserved
71	GND	-	-	-	GND
72	GND	-	-	-	GND
73	GND	-	-	-	GND
74	GND	-	-	-	GND
75	GND	-	-	-	GND
76	VCC3P3	-	-	3.3V	Power
77	GND	-	-	-	GND
78	VCC3P3	-	-	3.3V	Power
79	GND	-	-	-	GND
80	VCC3P3	-	-	3.3V	Power

Table 3-8 Pin Distribution of MIPI DPHY Soft Core Interface

J9 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	GND	-	-	-	GND
2	GND	-	-	-	GND
3	MIPI_D4N	K11	5	3.3V	MIPI transmit data
4	MIPI_D3P	N14	5	3.3V	MIPI transmit data
5	MIPI_D4P	J11	5	3.3V	MIPI transmit data
6	MIPI_D3N	N15	5	3.3V	MIPI transmit data
7	GND	-	-	-	GND
8	GND	-	-	-	GND
9	MIPI_D5N	M15	5	3.3V	MIPI transmit data
10	MIPI_D2P	K12	5	3.3V	MIPI transmit data
11	MIPI_D5P	L15	5	3.3V	MIPI transmit data
12	MIPI_D2N	K13	5	3.3V	MIPI transmit data
13	GND	-	-	-	GND
14	GND	-	-	-	GND
15	MIPI_D6N	L14	5	3.3V	MIPI transmit data
16	MIPI_D1P	L12	5	3.3V	MIPI transmit data
17	MIPI_D6P	L13	5	3.3V	MIPI transmit data
18	MIPI_D1N	M13	5	3.3V	MIPI transmit data
19	GND	-	-	-	GND
20	GND	-	-	-	GND
21	MIPI_D7N	J15	4	3.3V	MIPI transmit data
22	MIPI_D0P	J13	5	3.3V	MIPI transmit data
23	MIPI_D7P	H15	4	3.3V	MIPI transmit data
24	MIPI_D0N	J14	5	3.3V	MIPI transmit data
25	GND	-	-	-	GND
26	GND	-	-	-	GND
27	MIPI_D8N	H10	5	3.3V	MIPI transmit data
28	MIPI_CKP	G12	4	3.3V	MIPI clock signal

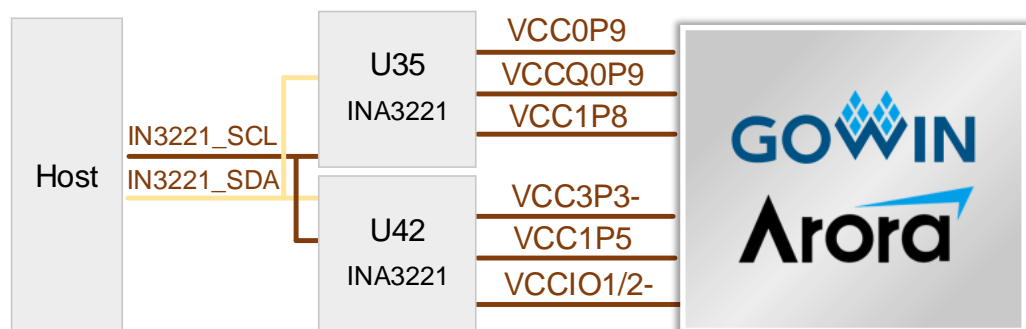
J9 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
29	MIPI_D8P	H11	5	3.3V	MIPI transmit data
30	MIPI_CKN	H12	4	3.3V	MIPI clock signal
31	GND	-	-	-	GND
32	GND	-	-	-	GND
33	MIPI_RST	G15	3	3.3V	Reset signal
34	GND	-	-	-	GND
35	GND	-	-	-	GND
36	VCC3P3	-	-	3.3V	Power
37	GND	-	-	-	GND
38	VCC3P3	-	-	3.3V	Power
39	GND	-	-	-	GND
40	VCC3P3	-	-	3.3V	Power

3.8 I2C Interface

3.8.1 Introduction

The development board includes 1-channel I2C interface as the host communication interface. The host can monitor the voltages of FPGA VCC, MIPI, VCCX, SerDes, and each BANK through this interface. The connection diagram of I2C interface is shown in Figure 3-9.

Figure 3-9 Connection Diagram of I2C Interface



3.8.2 Pin Distribution

Table 3-9 J21 Pin Distribution of I2C-1 Interface

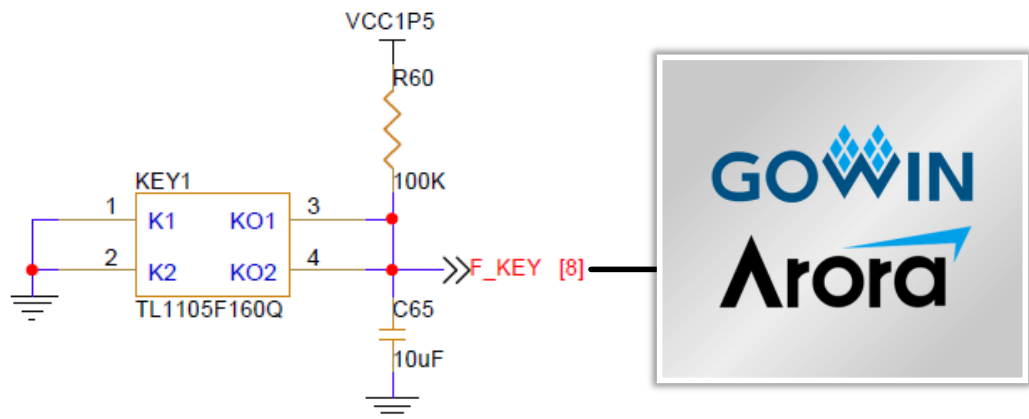
J21 Pin No.	Signal Name	I/O Level	Description
1	INA3221_SCL	3.3V	Serial bus clock line
2	INA3221_SDA	3.3V	Serial bus data line
3	GND	-	GND

3.9 Key & LED

3.9.1 Introduction

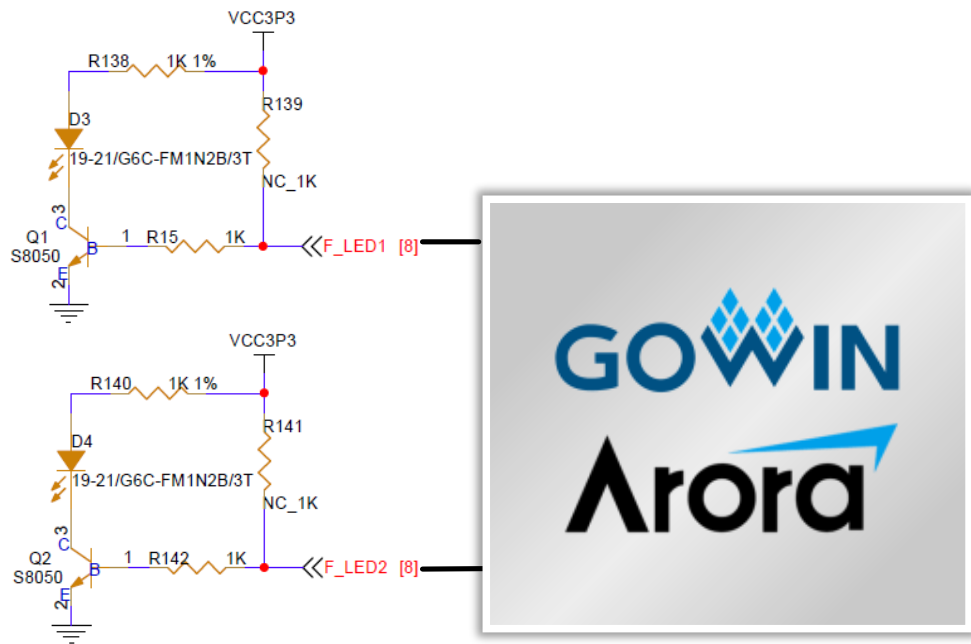
There is one user key on the development board. The user key is connected to the general IO of FPGA BANK8. The corresponding IO input voltage of the FPGA is low when the key is pressed while high when the key is not pressed. The connection diagram is shown in Figure 3-10.

Figure 3-10 Connection Diagram of Key



The development board includes two user LEDs. The user LEDs are connected to the IO of FPGA BANK8 and can be switched on and off via the program. The user LEDs will be on when the IO voltage is high. The user LEDs will be off when the IO voltage is low. The connection diagram is shown in Figure 3-10.

Figure 3-11 Connection Diagram of LED



3.9.2 Pin Distribution

Table 3-10 Pin Distribution of Key

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_KEY	L9	8	1.5V	Key

Table 3-11 Pin Distribution of LED

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_LED1	R11	8	1.5V	LED indicator
F_LED2	R10	8	1.5V	LED indicator

3.10 GPIO

3.10.1 Introduction

There is one 10P pin header J20 with 2.54 mm pitch on the development board, with a total of six 3.3V GPIO interfaces for user testing.

Figure 3-12 Connection Diagram of GPIO



3.10.2 Pin Distribution

Table 3-12 Pin Distribution of GPIO Interface

J20 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	VCC3P3	-	-	3.3V	Power
2	VCC3P3	-	-	3.3V	Power
3	F_GPIO0	B13	2	3.3V	GPIO reserved
4	F_GPIO1	A13	2	3.3V	GPIO reserved
5	F_GPIO2	B14	2	3.3V	GPIO reserved
6	F_GPIO3	A14	2	3.3V	GPIO reserved
7	F_GPIO4	D13	2	3.3V	GPIO reserved
8	F_GPIO5	C14	2	3.3V	GPIO reserved
9	GND	-	-	-	GND
10	GND	-	-	-	GND

