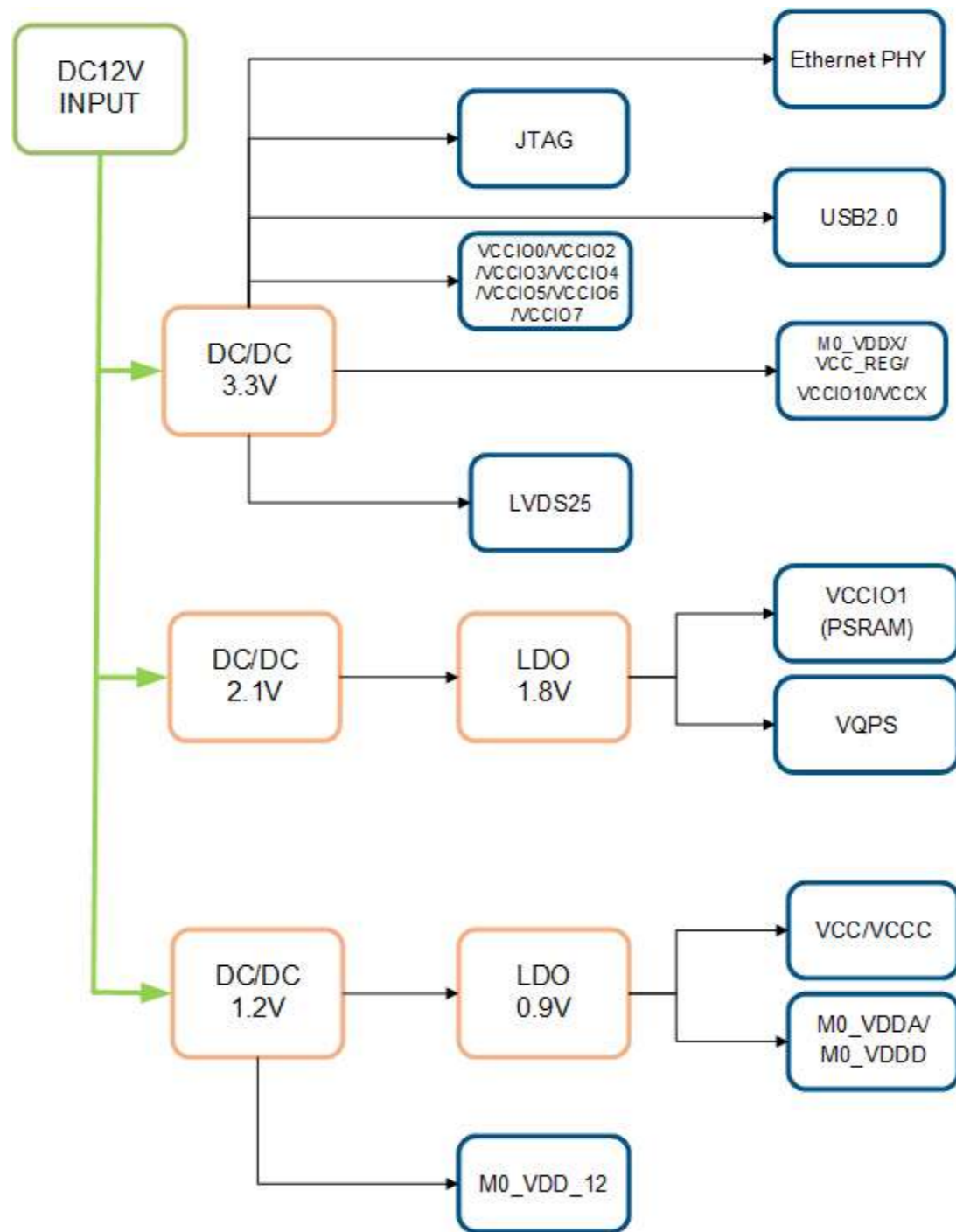
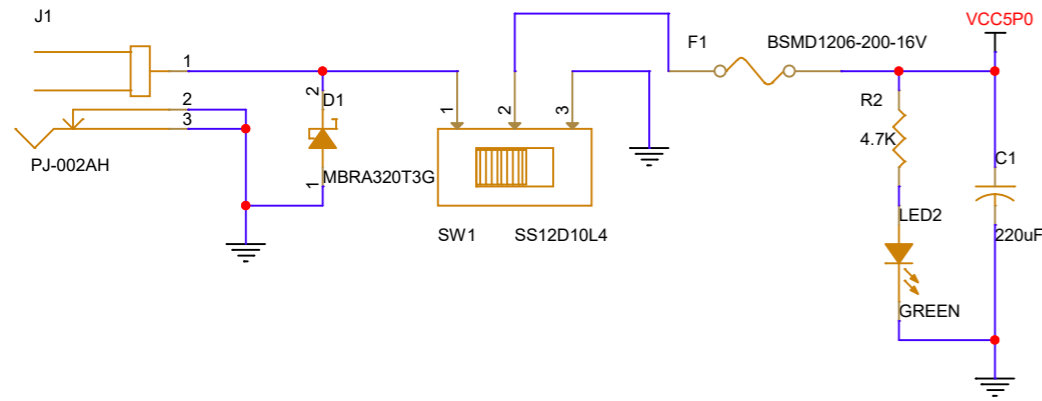


PAGE1	Block Diagram
PAGE2	POWER TREE
PAGE3	POWER-DC/DC
PAGE4	POWER-LDO
PAGE5	FPGA-LVDS-MIPI
PAGE6	FPGA-EthernetPHY
PAGE7	FPGA-USB-OSC
PAGE8	FPGA-74HC245
PAGE9	FPGA-POWER&GND

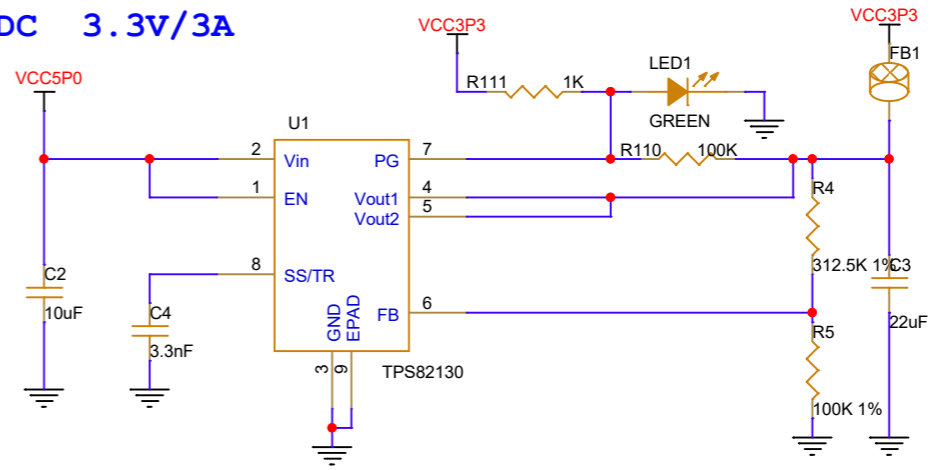
# POWER TREE



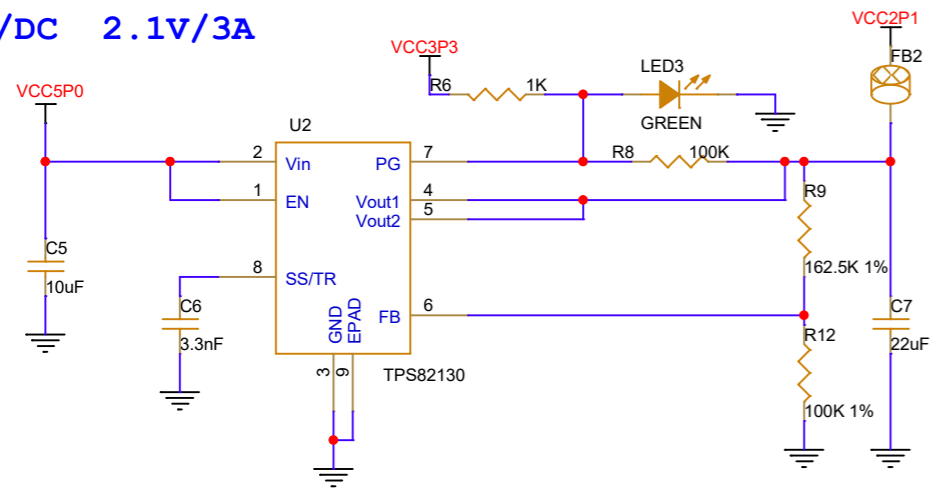
### 5V INPUT



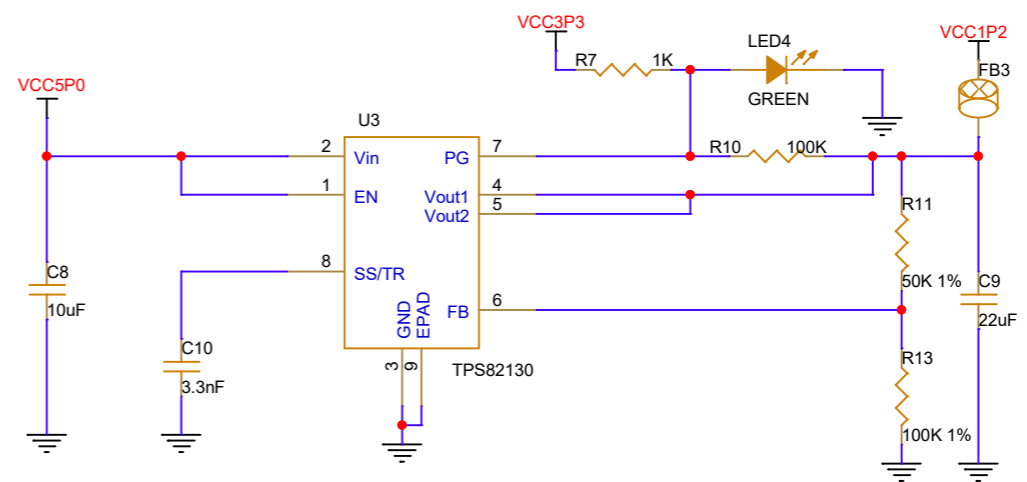
### DC/DC 3.3V/3A



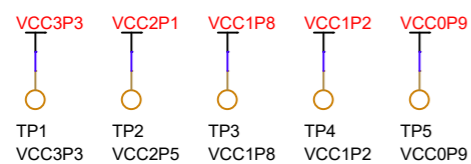
### DC/DC 2.1V/3A



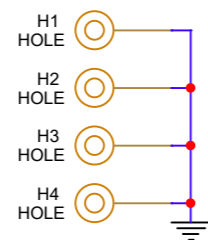
### DC/DC 1.2V/3A



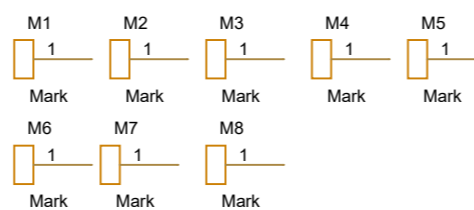
### Power Test Hole

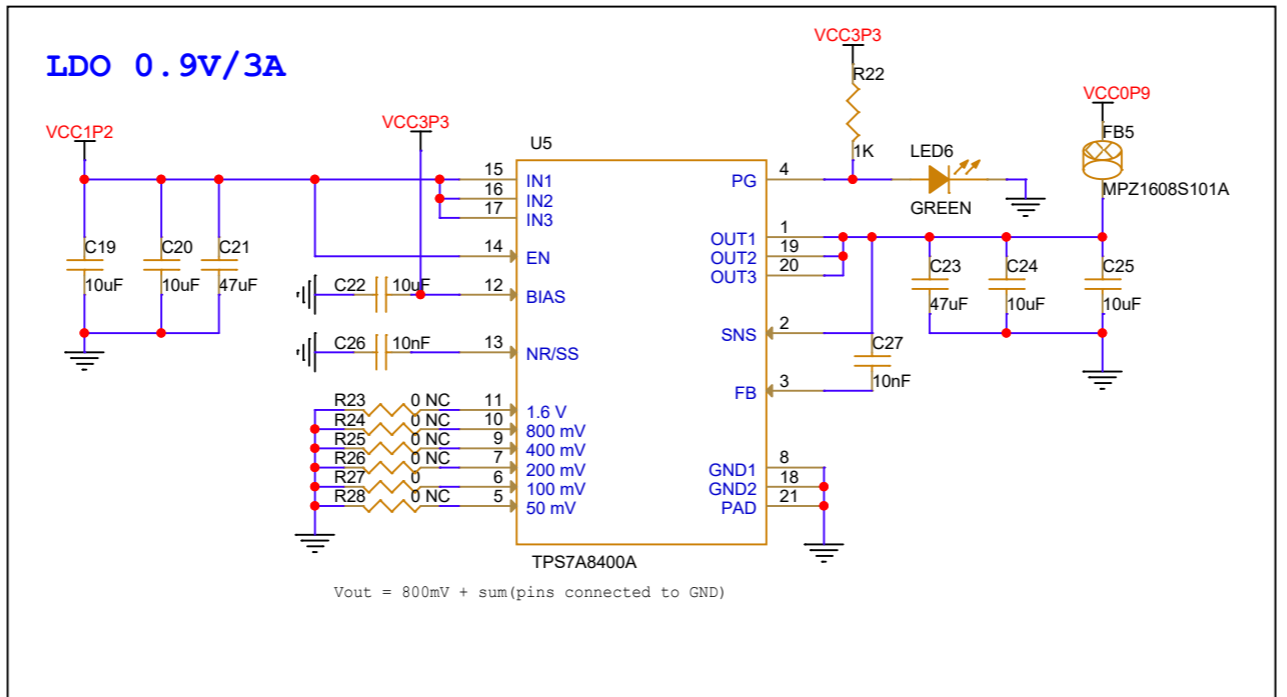
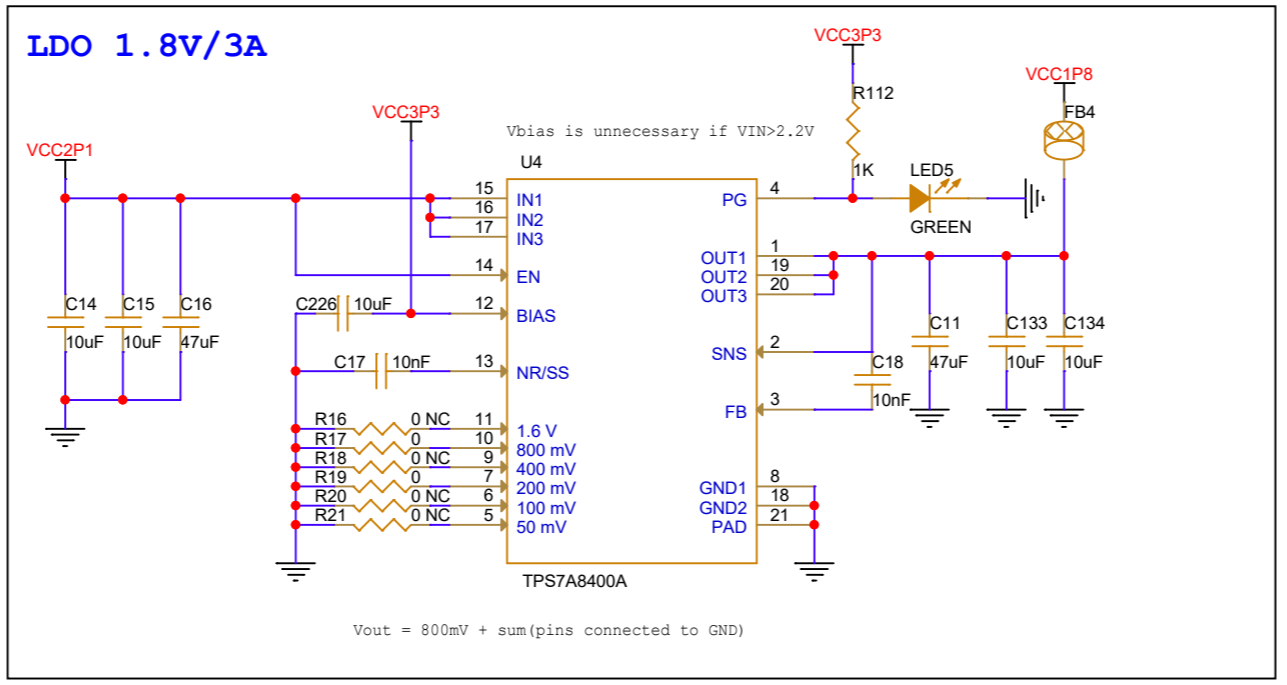


### Mounting Hole



### Mark





Title		
DK_START_GW5AR-LV25UG256PC211_V1.0		
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A3	POWER-LDO	1.0
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# FPGA

[8] GPIO[20:26] << GPIO[20:26]  
 [8] GPIO65 << GPIO65

U6F		Bank 6	
GPIO25	A15	IOL3A/GCLKT_14/LPLL0_T_IN2/LVDS/DQ7/X16	
GPIO26	B16	IOL3B/GCLKC_14/LPLL0_C_FB0/LVDS/DQ7/X16	
LR_2P5_CLKp	B14	IOL5A/GCLKT_13/LPLL0_T_IN1/LVDS/DQ7/X16	
LR_2P5_CLKn	A14	IOL5B/GCLKC_13/LPLL0_C_FB1/LVDS/DQ7/X16	
LR_2P5_2p	D11	IOL7A/LVDS/DQ7/X16	
LR_2P5_2n	C11	IOL7B/LVDS/DQ7/X16	
LT_2P5_2p	C9	IOL9A/LVDS/DQS7/DQ7/X16	
LT_2P5_2n	D9	IOL9B/LVDS/DQS7/DQ7/X16	
LT_2P5_3p	C8	IOL12A/LVDS/DQ7/X16	
LT_2P5_3n	D8	IOL12B/LVDS/DQ7/X16	
GPIO20	C6	IOL14A/LPLL1_T_IN0/LVDS/DQ7/X16	
GPIO21	D6	IOL14B/LVDS/DQ7/X16	
LR_2P5_1p	B13	IOL16A/LVDS/DQ6/DQS_67/X16	
LR_2P5_1n	A13	IOL16B/LVDS/DQ6/DQS_67/X16	
LR_2P5_3p	B11	IOL18A/LVDS/DQ6/X16	
LR_2P5_3n	B12	IOL18B/LVDS/DQ6/X16	
LR_2P5_4p	A11	IOL21A/LVDS/DQS6/DQ6/X16	
LR_2P5_4n	A12	IOL21B/LVDS/DQS6/DQ6/X16	
LT_2P5_1p	B10	IOL23A/LVDS/DQ6/X16	
LT_2P5_1n	A10	IOL23B/LVDS/DQ6/X16	
LT_2P5_CLKp	B9	IOL25A/LVDS/DQ6/X16	
LT_2P5_CLKn	A9	IOL25B/LVDS/DQ6/X16	
LT_2P5_4p	A8	IOL27A/LVDS/DQ6/X16	
LT_2P5_4n	B8	IOL27B/LVDS/DQ6/X16	
GPIO24	E8	IOL29A/LVDS/X16	
GPIO65	F8	IOL29B/LVDS/X16	
GPIO22	E7	IOL31A/LVDS/X16	
GPIO23	F7	IOL31B/LVDS/X16	

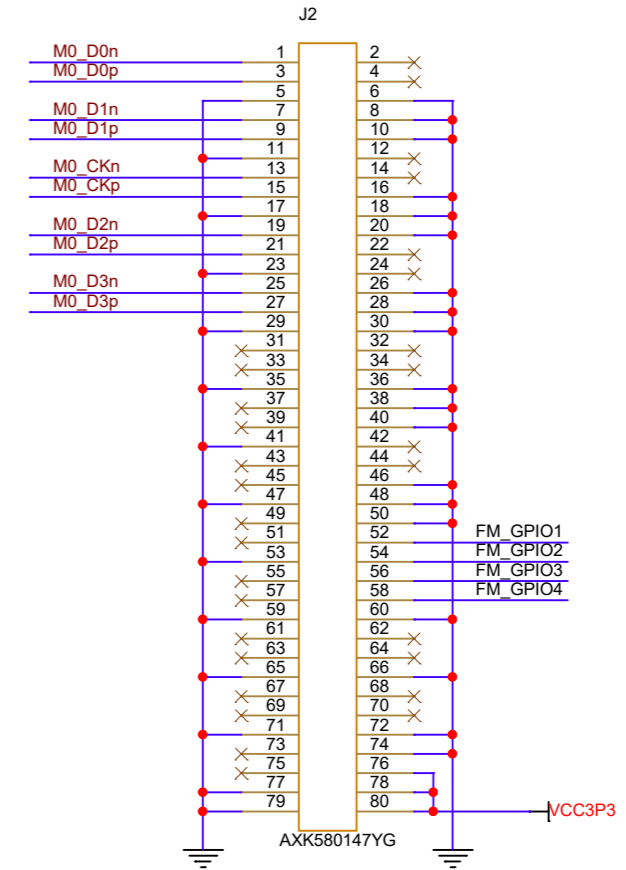
GW5AR-25-UG256P

U6H		Bank 10	
JTAG_TCK	R13	IOR1A/TCK	
JTAG_TDI	R14	IOR1B/TDI	
JTAG_TMS	T14	IOR3A/TMS	
JTAG_TDO	T15	IOR3B/TDO	
MIPI			
M0_CKn	B5	M0_CKN	
M0_CKp	A5	M0_CKP	
M0_D0n	B7	M0_D0N	
M0_D0p	A7	M0_D0P	
M0_D1n	B6	M0_D1N	
M0_D1p	A6	M0_D1P	
M0_D2n	B4	M0_D2N	
M0_D2p	A4	M0_D2P	
M0_D3n	B3	M0_D3N	
M0_D3p	A3	M0_D3P	

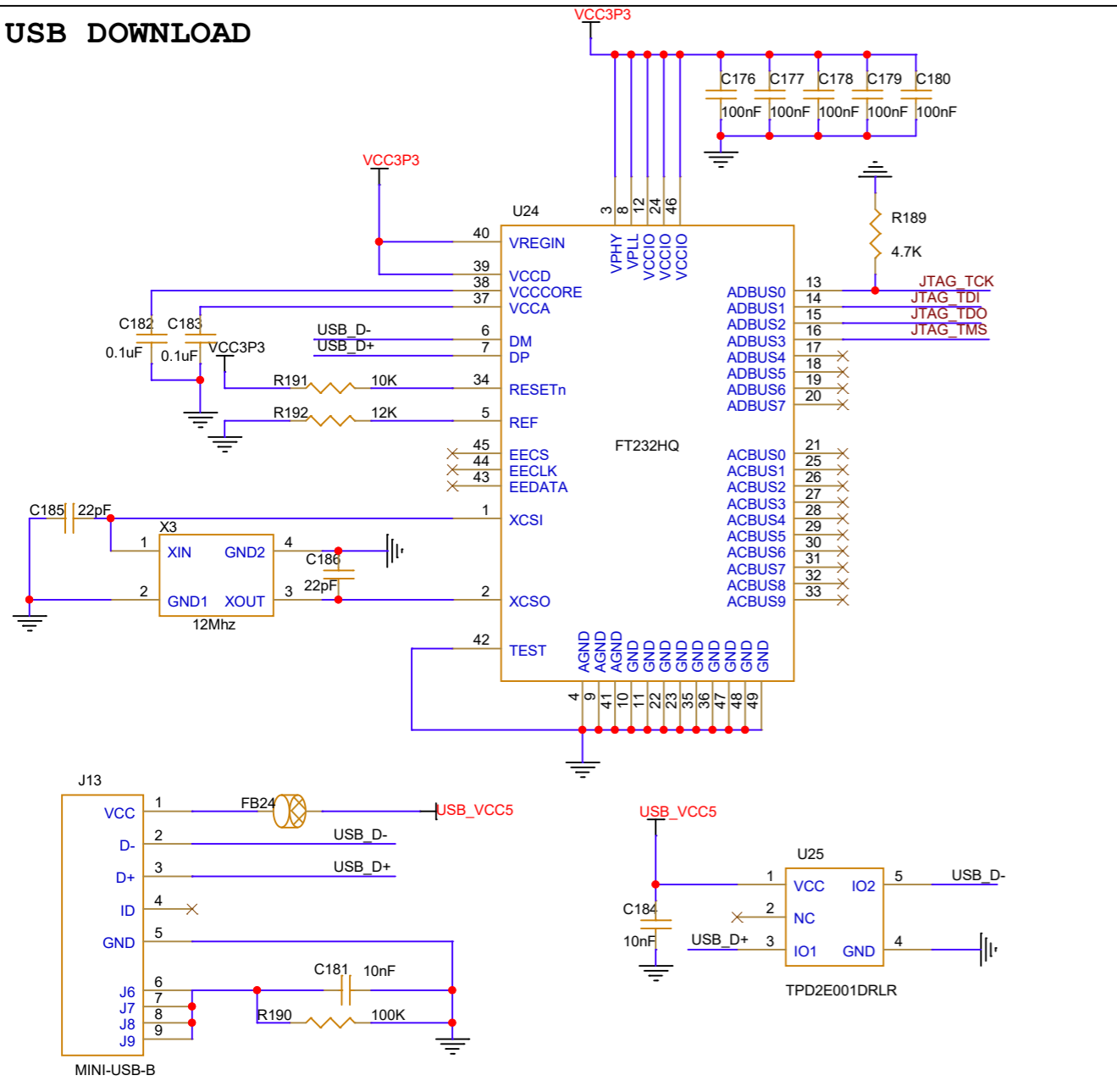
GW5AR-25-UG256P

[7] FM\_GPIO1 << FM\_GPIO1  
 [7] FM\_GPIO2 << FM\_GPIO2  
 [7] FM\_GPIO3 << FM\_GPIO3  
 [7] FM\_GPIO4 << FM\_GPIO4

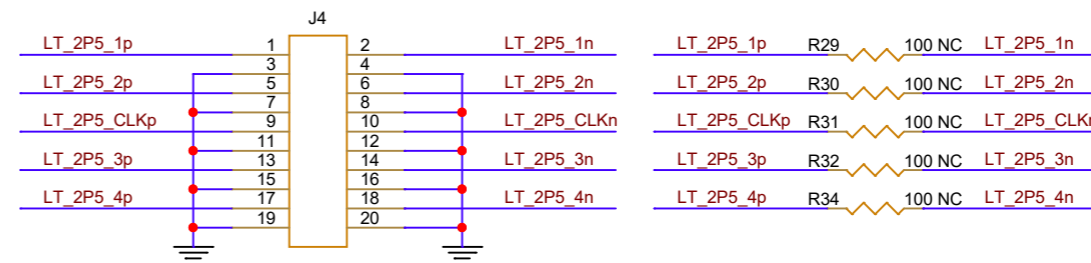
# MIPI



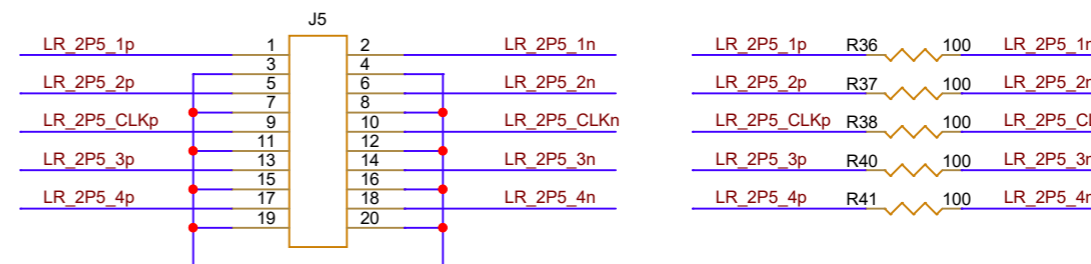
# USB DOWNLOAD



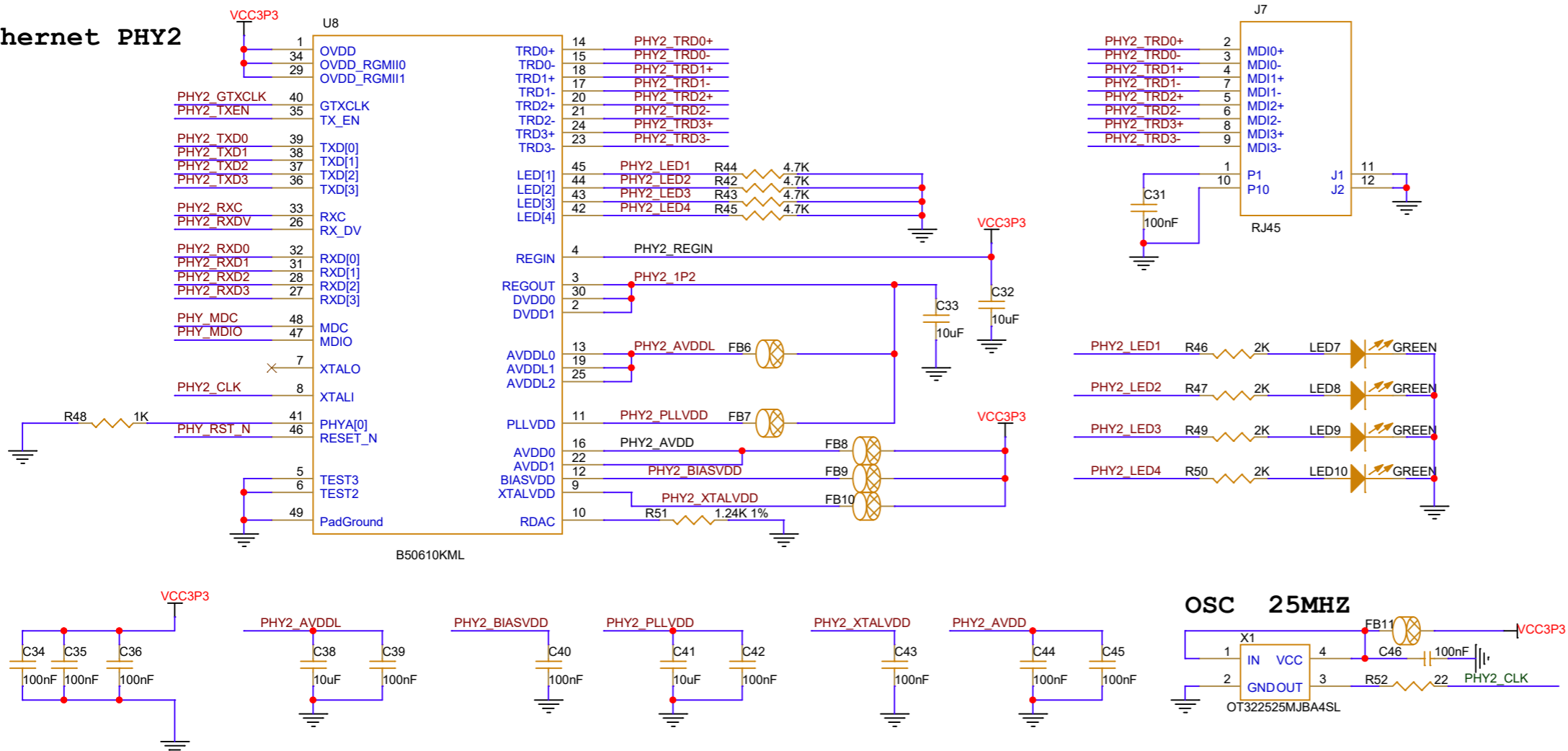
# LVDS TX



# LVDS RX

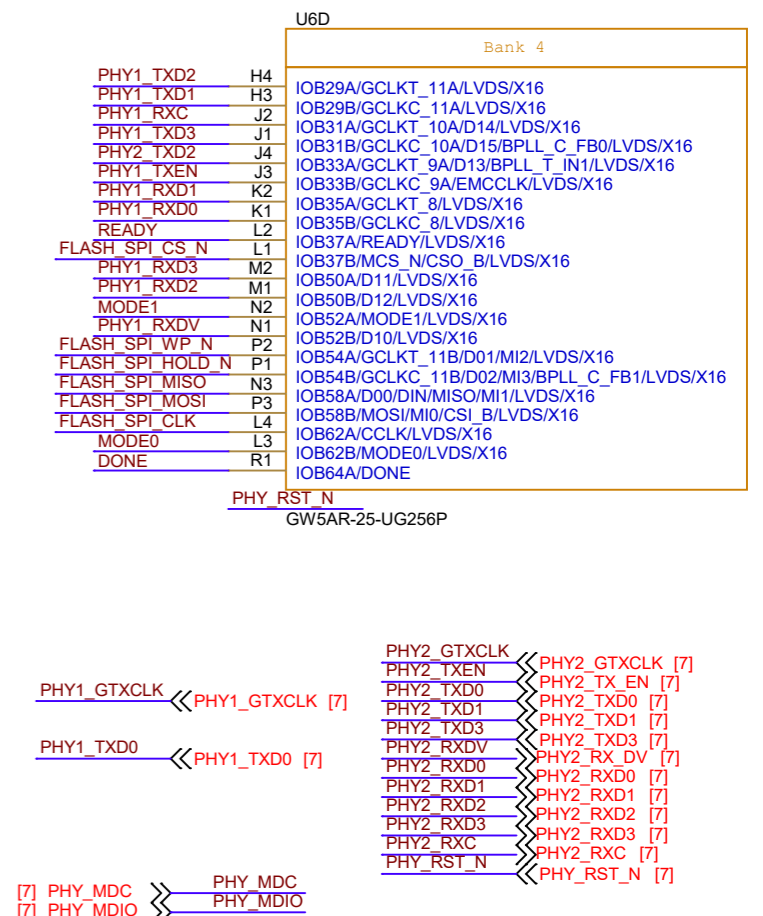


### Ethernet PHY2

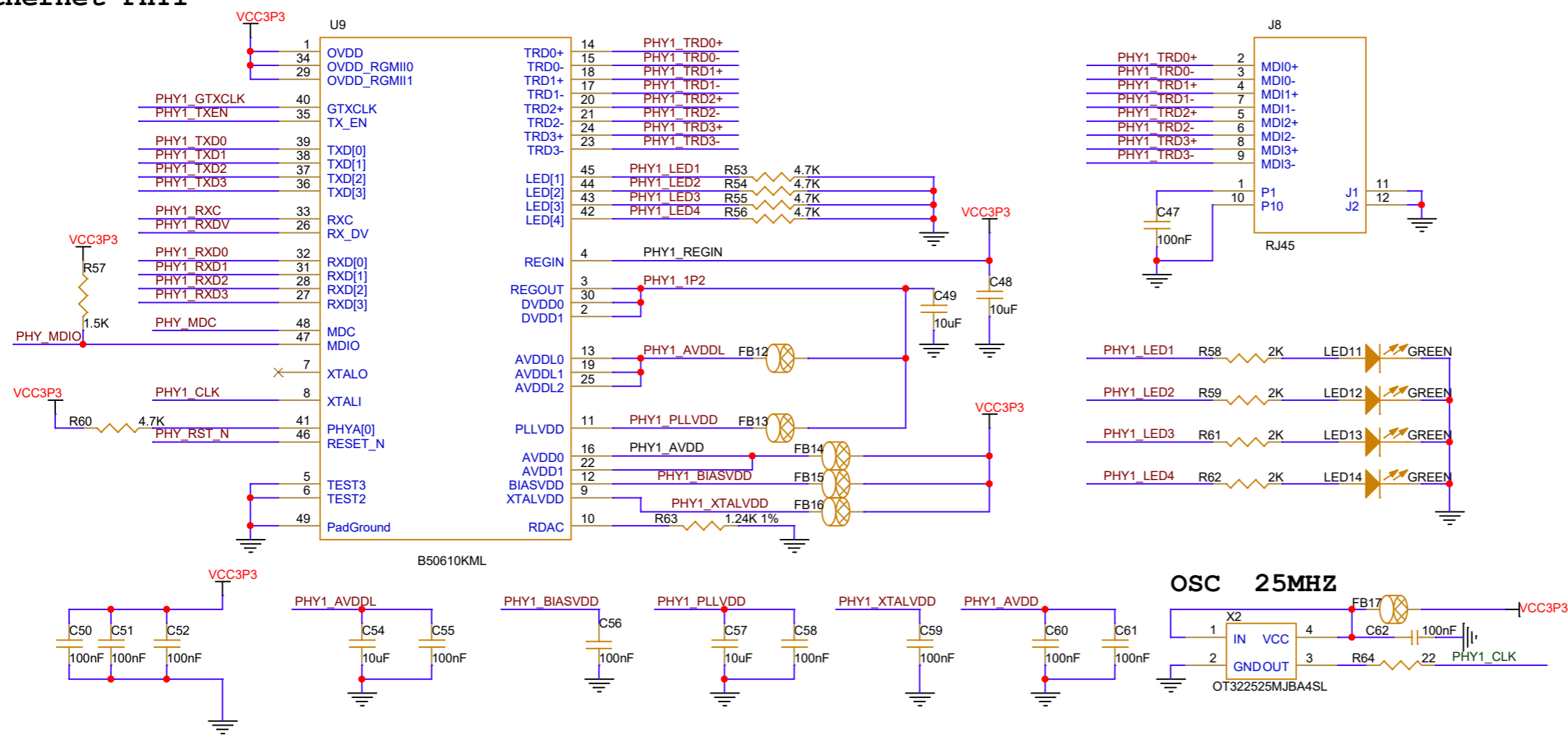


### FPGA

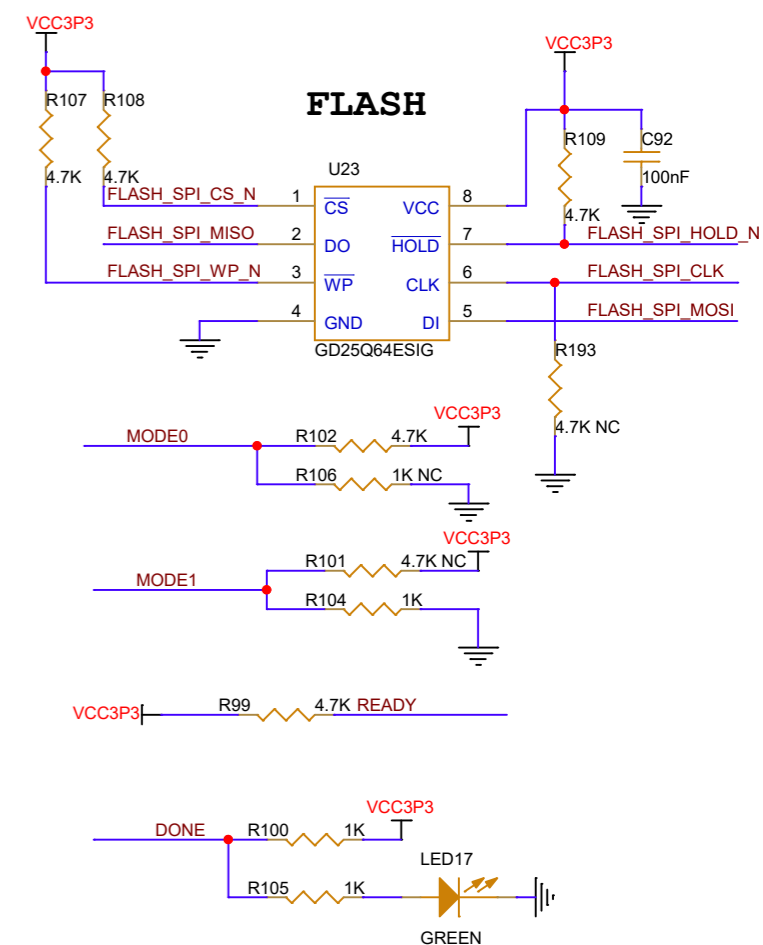
### Bank4



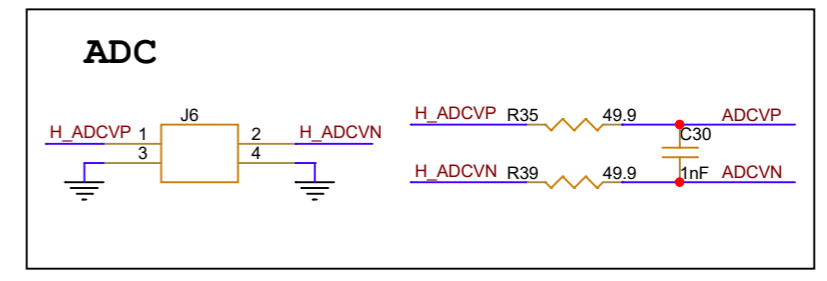
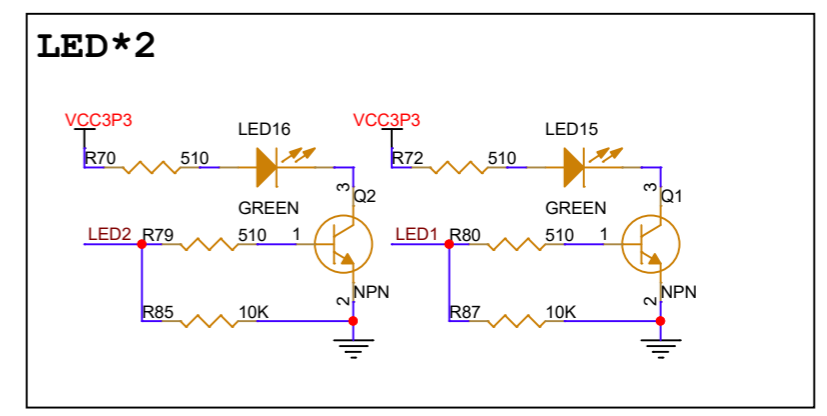
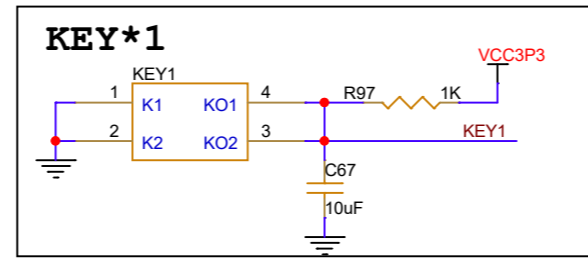
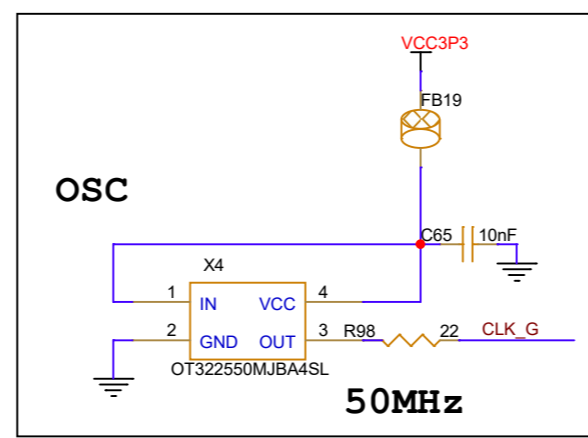
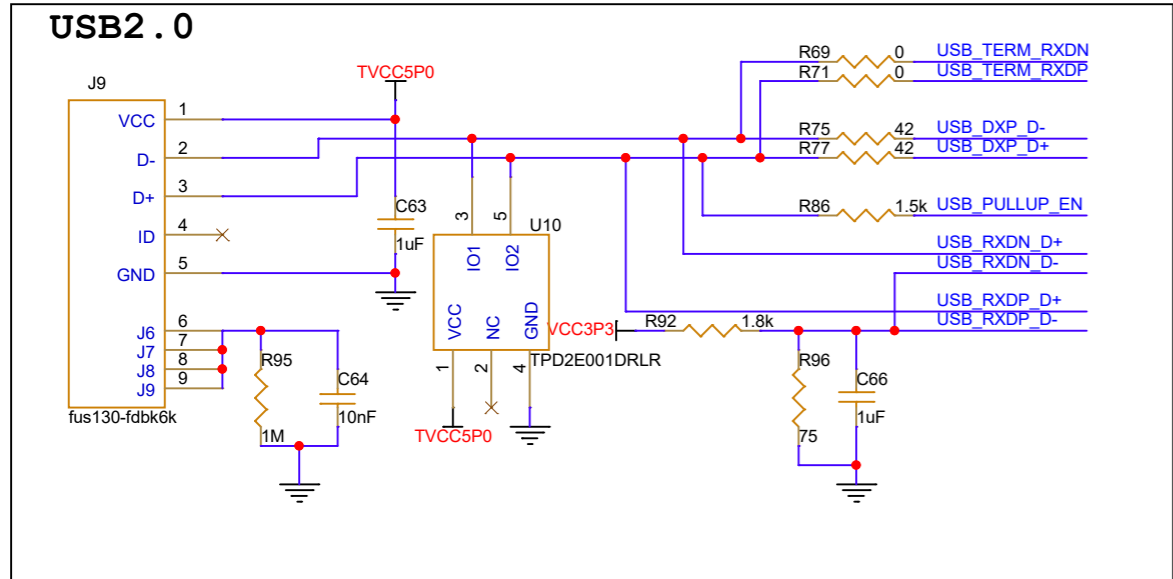
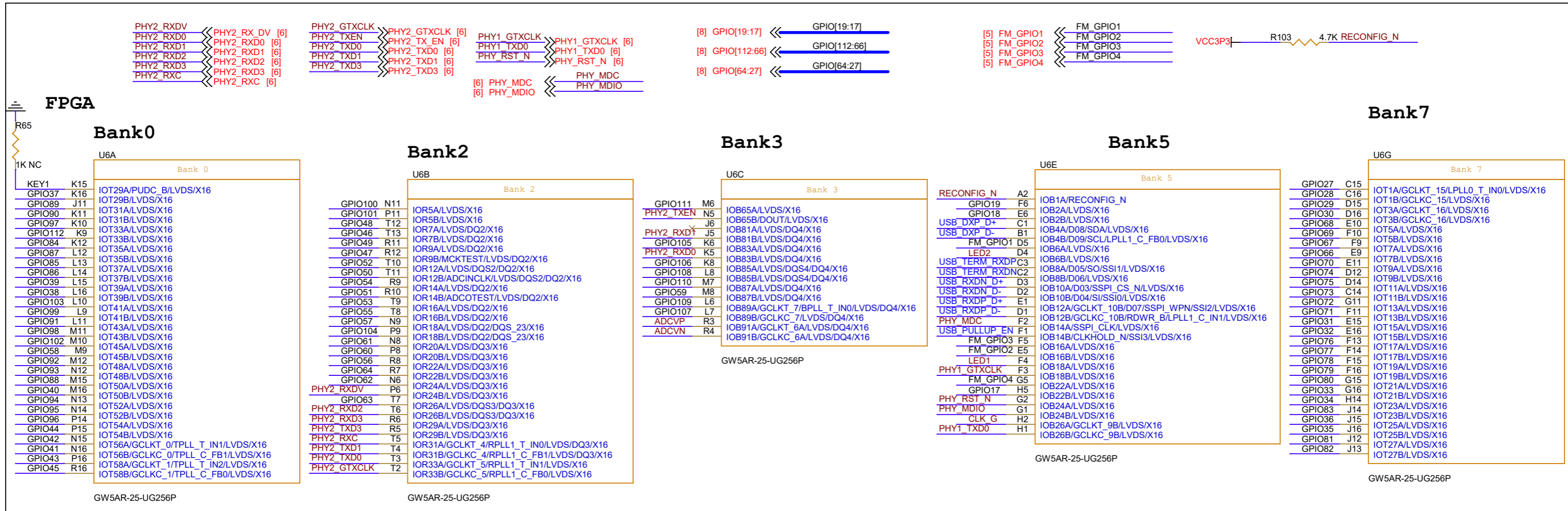
### Ethernet PHY1



### FLASH

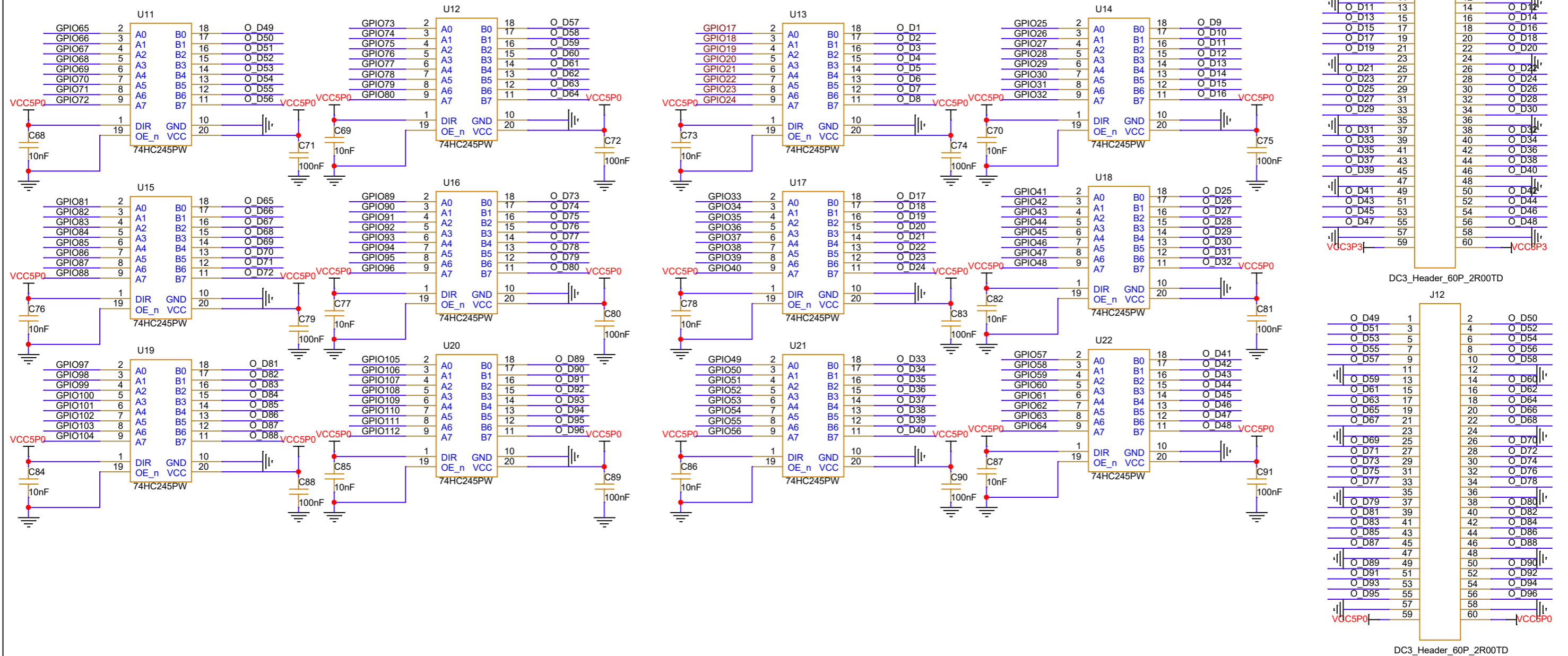


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A3	FPGA-EthernetPHY	1.0
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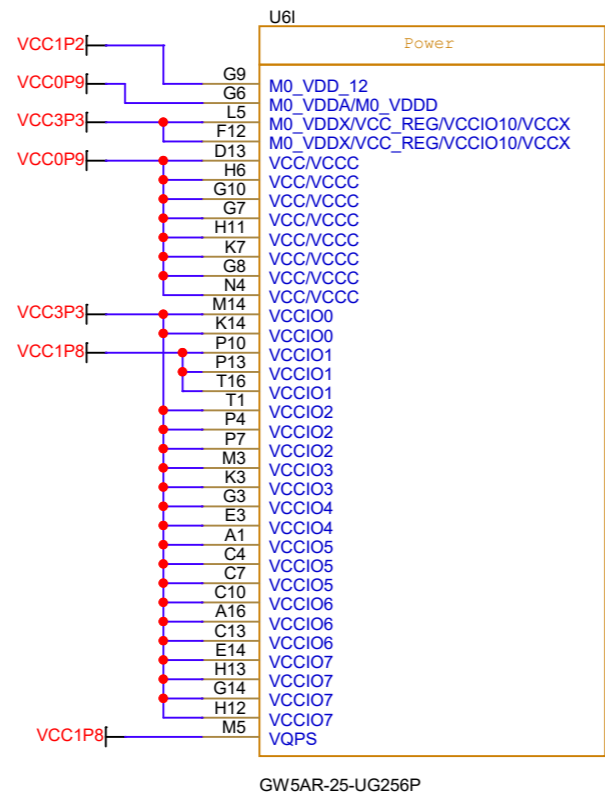
# 74HC245

[7] GPIO[112:66] >> GPIO[112:66]  
 [7] GPIO[19:17] >> GPIO[19:17]  
 [7] GPIO[64:27] >> GPIO[64:27]  
 [5] GPIO[20:26] >> GPIO[20:26]  
 [5] GPIO65 >> GPIO65

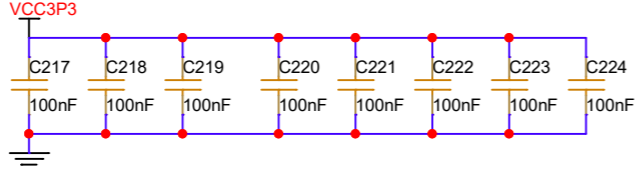
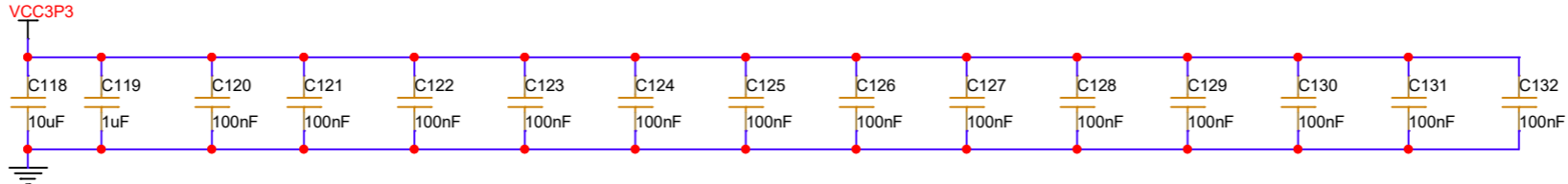
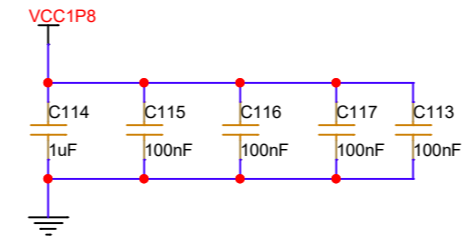
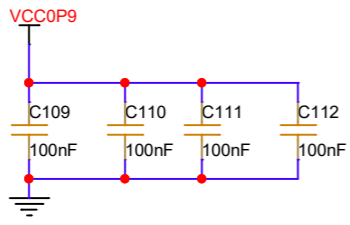
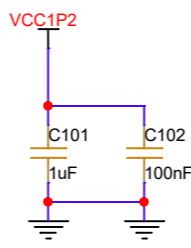
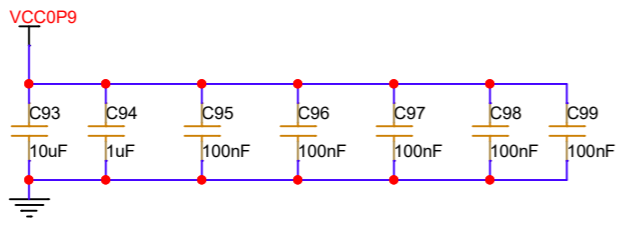
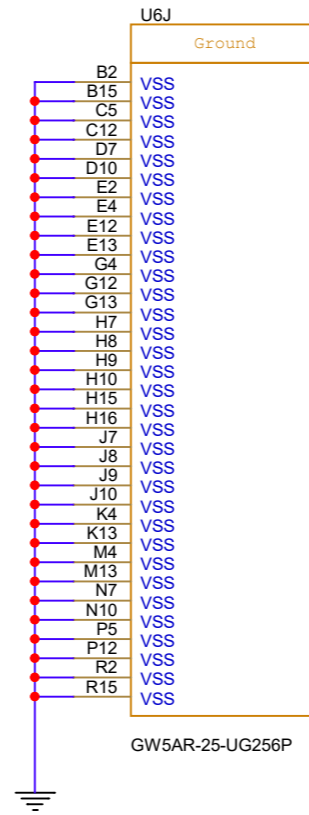




### FPGA POWER



### FPGA GND



Title		
DK_START_GW5AR-LV25UG256PC2I1_V1.0		
Size	Document Number	Rev
A3	FPGA POWER&GND	1.0
Date:	Monday, December 25, 2023	Sheet 9 of 9