DK_START_GW5AR-LV25UG256PC2I1_V1.0

User Guide

DBUG1273-1.0E, 9/26/2024

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Revision History

Date	Version	Description
09/26/2024	1.0E	Initial version published.

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1 About This Guide

1.1 Purpose

The DK_START_GW5AR-LV25UG256PC2I1_V1.0 development board (hereinafter referred to as “the development board”) user guide consists of following three parts:

- A brief introduction to the features of the development board.
- An introduction to the development board system architecture and hardware resources
- An introduction to the hardware circuits, functions and pin distribution

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- DS1103, Arora V 25K FPGA Products Data Sheet
- UG1110, GW5AR-25 Pinout
- UG1109, GW5AR series of FPGA Products Package and Pinout User Guide
- UG714, Arora V 25K FPGA Products Programming and Configuration User Guide
- SUG100, Gowin Software User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array

Terminology and Abbreviations	Meaning
GPIO	Gowin Programmable Input/Output
MIPI	Mobile Industry Processor Interface
ADC	Analog-to-digital Converter
JTAG	Joint Test Action Group
LDO	Low Dropout Regulator
LVDS	Low-Voltage Differential Signaling

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Development Board Introduction

2.1 Overview

Figure 2-1 DK_START_GW5AR-LV25UG256PC2I1_V1.0 Development Board

Gowin GW5AR series of FPGA products are the 5 series products of Arora family. As a kind of SIP chips, the GW5AR series of FPGA product integrates a PSRAM memory chip on the basis of the GW5A, with abundant internal resources, high-performance DSP with a new architecture that supports AI operations, high-speed LVDS interface and abundant BSRAM resources. At the same time, it integrates self-developed DDR3, and provides a variety of packages. It is suitable for applications such as low power, high performance and compatibility design. GOWINSEMI also provides a newly independently developed FPGA hardware development environment for the market, which supports

the GW5AR series of FPGA products. This environment provides a one-stop solution for FPGA synthesis, placement, routing, bitstream file generation, and downloading.

DK_START_GW5AR-LV25UG256PC2I1_V1.0 development board applies to Ethernet communication, LVDS communication, and MIPI communication; integrates MIPI, LVDS-TX, LVDS-RX, Ethernet, USB, and GPIO interfaces, etc, supporting FPGA's MIPI D-PHY function evaluation, hardware reliability verification, and software learning and debugging, etc.

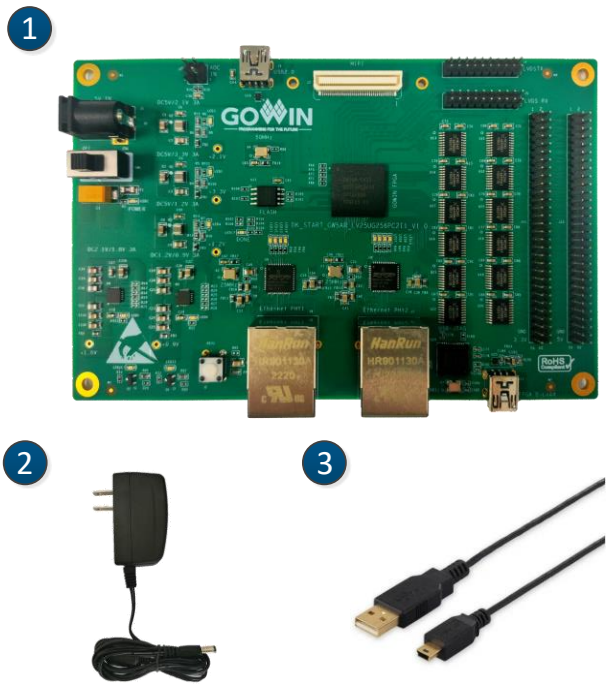
The development board adopts Gowin GW5AR-LV25UG256P FPGA device. For the internal resources of the chip, see *DS1108,Arora V 25K FPGA Products Data Sheet*.

2.2 A Development Board Kit

The development board kit includes the following items:

1. DK_START_GW5AR-LV25UG256PC2I1_V1.0 development board
2. 5V power (Input: AC 100-240V~50/60Hz 0.5A, output: DC5V 2A)
3. Mini USB-B Cable

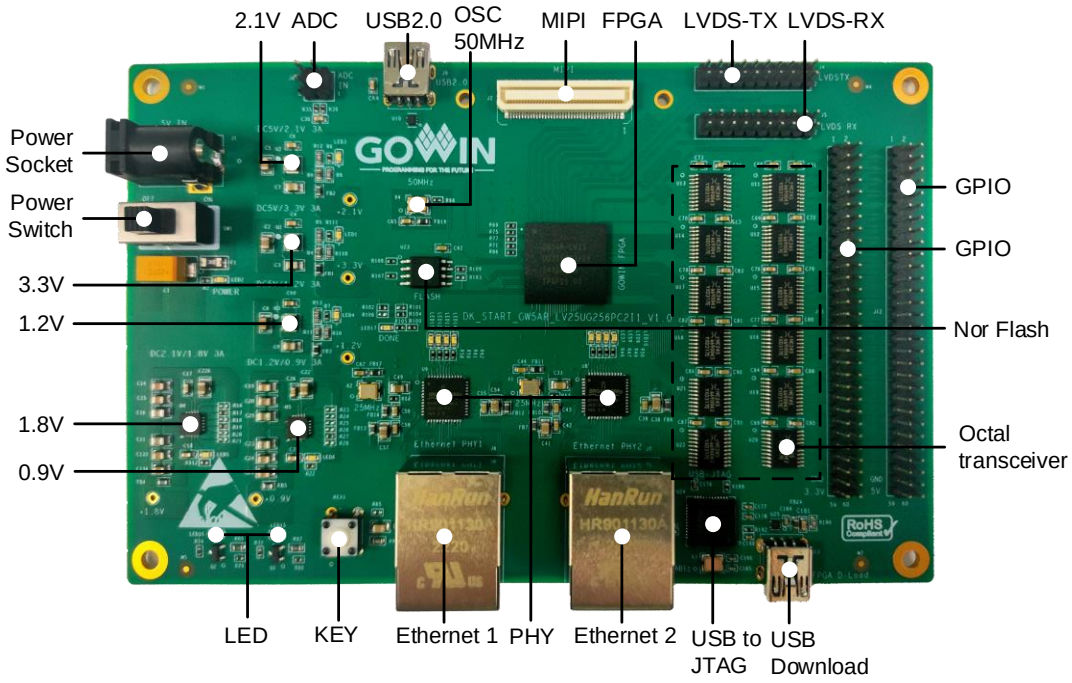
Figure 2-2 A Development Board Kit



① DK_START_GW5AR-LV25UG256PC2I1_V1.0 development board
② 5V power supply
③ Mini USB-B Cable

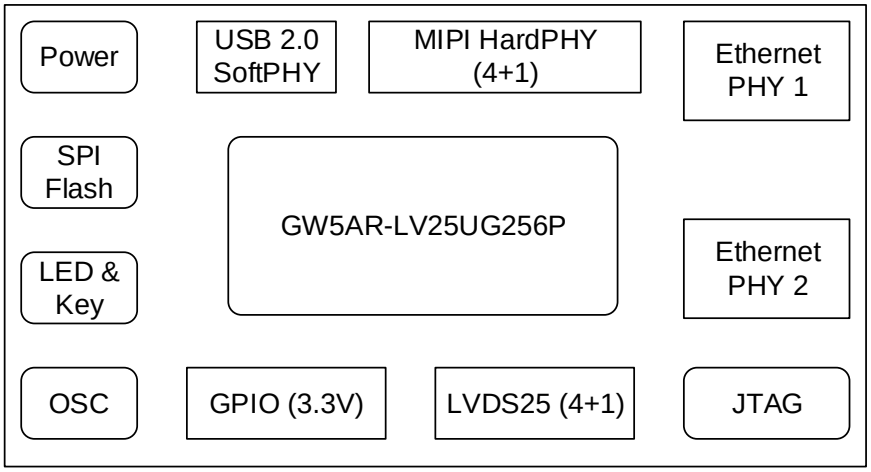
2.3 PCB Components

Figure 2-3 PCB Components



2.4 System Block Diagram

Figure 2-4 System Block Diagram



2.5 Features

The key features are as follows:

- FPGA Device
  - Gowin GW5AR-LV25UG256P FPGA
  - Max. user I/O: 178

- Download and Boot
  - Integrate USB download circuit on the board, download through Mini USB-B interface
  - External SPI Flash Boot
- Power
  - External DC5V 2A Power
  - The Power light is on after power on.
  - The board generates 3.3V, 2.1V, 1.8V, 1.2V, 0.9V power.
- System Clock
  - 50MHz clock
- Memory device
  - 64Mbit NOR Flash
- Ethernet Interface
  - 2-channel Ethernet interfaces
  - RGMII interface, supporting 10BASE-T/100BASE-TX/1000BASE-T
  - RJ45 connector integrated with network transformer internally
- MIPI Interface
  - MIPI_RX/TX hard core, single channel, includes 4 data + 1 clk
  - 4 GPIOs
  - 3.3V power supply
  - Use connector with 80 contacts and 0.5mm pitch
- LVDS Interface
  - 1-channel LVDS-TX interface, single channel, including 4 data + 1 clk
  - 1-channel LVDS-RX interface, single channel, including 4 data + 1 clk
- USB 2.0 Interface
  - Mini USB-B interface with electrostatic protection
- ADC Interface
  - 1-channel ADC interface
  - The interface uses 2x2p pins.
  - The ADC differential input is designed with an anti-aliasing filter circuit.
- LED & Key
  - 2 LED indicators
  - 1 key
- GPIO
  - 96 5V level output signals

3 Development Board Circuit

3.1 FPGA

3.1.1 Overview

For the resources of GW5AR series of FPGA Products, refer to *DS1103, Arora V 25K FPGA Products Data Sheet*.

3.1.2 I/O BANK Introduction

For the I/O BANK, package, and pinout information, see *UG1109, GW5AR series of FPGA Products Package and Pinout User Guide* for more details.

3.2 Power Supply

3.2.1 Introduction

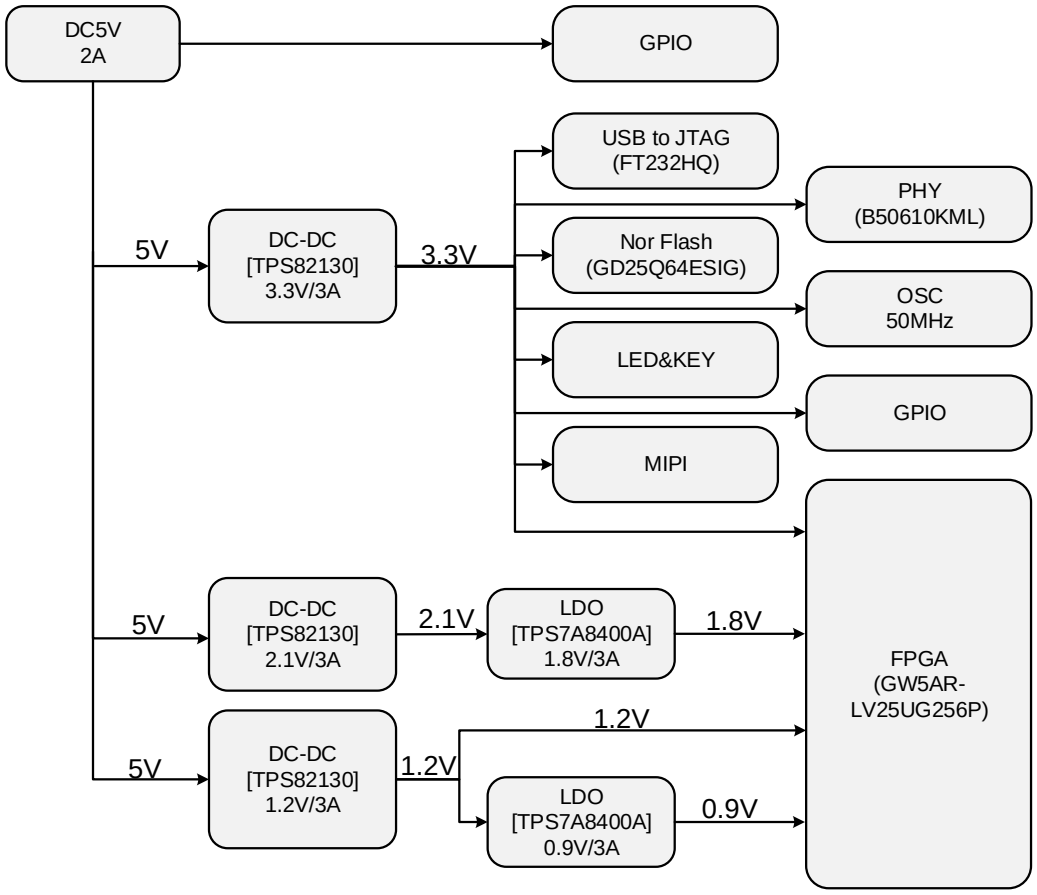
The development board needs to be powered by a 5V power adapter.

The input parameter of the adapter is AC 100-240V~50/60MHz 0.5A, and the output parameter is DC 12V 2A.

The input 5V power is regulated by the PMIC on the development board to generate 3.3V, 2.1V, 1.8V, 1.2V, and 0.9V power supplies, thus meeting the power supply requirements of the development board.

3.2.2 Power Distribution

Figure 3-1 Power Distribution Diagram



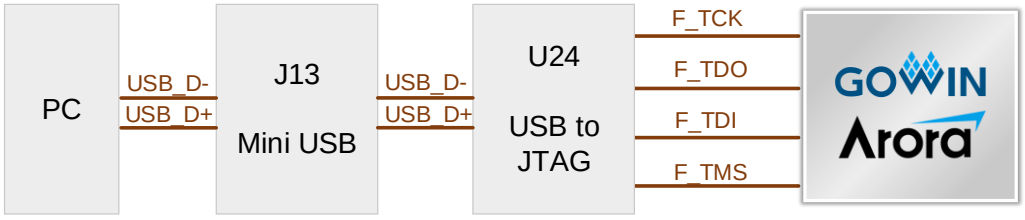
3.3 Download Module

3.3.1 Introduction

The development board has a Mini USB-B download port (J13) designed to program the programs to external SPI FLASH or download them to SRAM.

The download connection diagram is show in Figure 3-2.

Figure 3-2 Connection Diagram of Download



3.3.2 Pin Distribution

Table 3-1 JTAG Pin Distribution

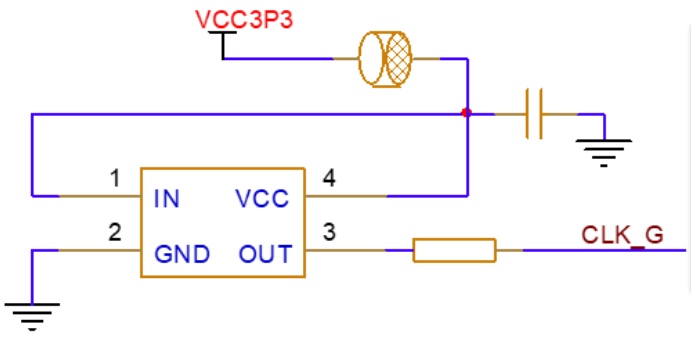
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
JTAG_TCK	R13	10	3.3V	JTAG signal
JTAG_TDO	T15	10	3.3V	
JTAG_TDI	R14	10	3.3V	
JTAG_TMS	T14	10	3.3V	

3.4 Clock

3.4.1 Introduction

FPGA clock source, 50MHz single-ended clock signal introduction The clock connection schematic is as shown in Figure 3-3.

Figure 3-3 Clock Connection Diagram



3.4.2 Pin Distribution

Table 3-2 Clock Pin Distribution

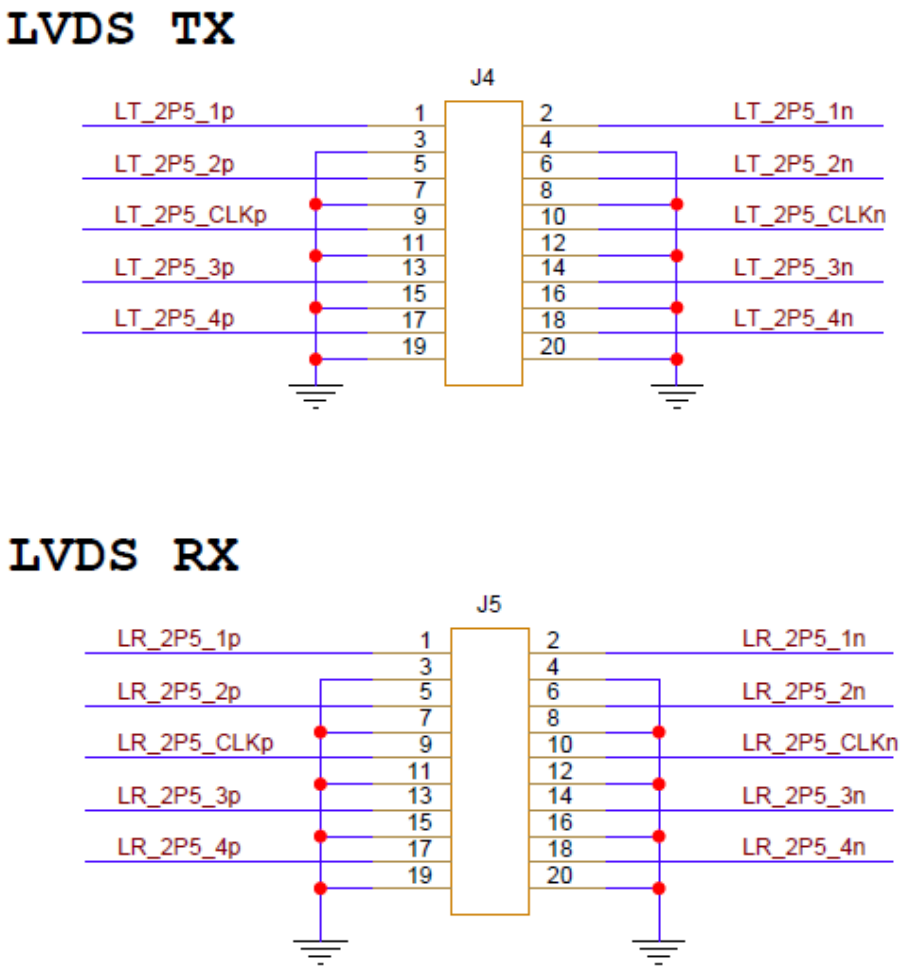
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
CLK_G	H2	5	3.3V	50MHz single-ended clock

3.5 LVDS Interface

3.5.1 Introduction

The development board includes both LVDS transmitter and receiver interfaces, with each connector being a 2x10P pin headers with 2.0 mm pitch. LVDS_TX contains: 4 data + 1 clk; LVDS_RX contains: 4 data + 1 clk. The interface circuit diagram is as follows.

Figure 3-4 Schematic of LVDS Interface



3.5.2 Pin Distribution

Table 3-3 LVD_TX Interface Pin Distribution

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
LT_2P5_1p	B10	6	3.3V	LVDS data
LT_2P5_1n	A10	6	3.3V	LVDS data
LT_2P5_2p	C9	6	3.3V	LVDS data
LT_2P5_2n	D9	6	3.3V	LVDS data
LT_2P5_CLKp	B9	6	3.3V	LVDS Clock
LT_2P5_CLKn	A9	6	3.3V	LVDS Clock
LT_2P5_3p	C8	6	3.3V	LVDS data
LT_2P5_3n	D8	6	3.3V	LVDS data
LT_2P5_4p	A8	6	3.3V	LVDS data
LT_2P5_4n	B8	6	3.3V	LVDS data

Table 3-4 LVDS_RX Interface Pin Distribution

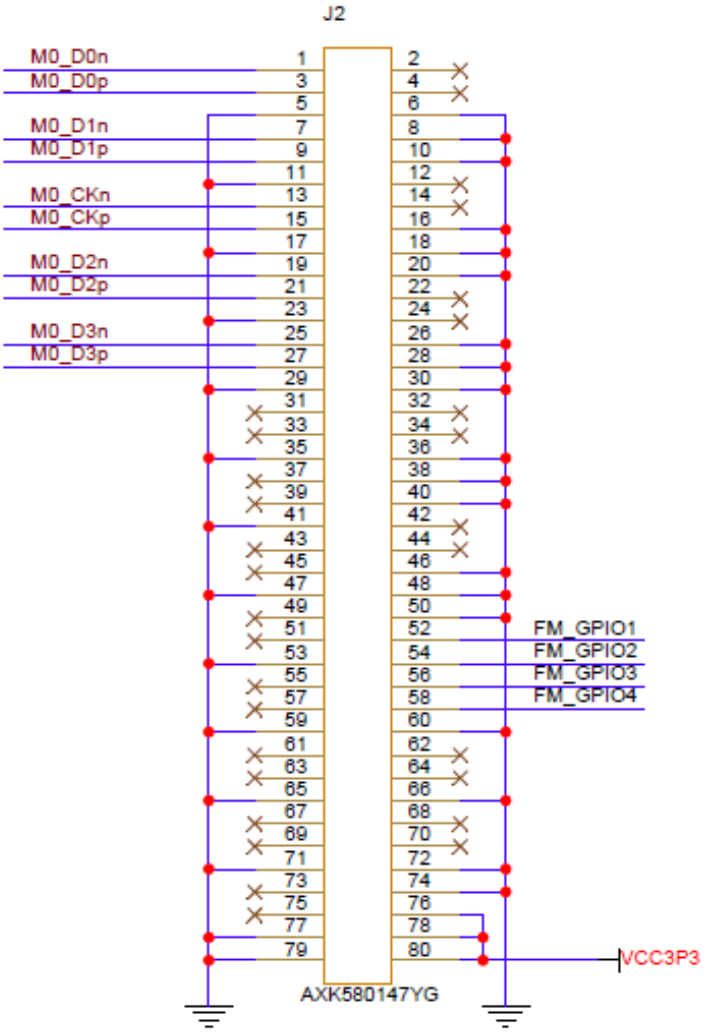
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
LR_2P5_1p	B13	6	3.3V	LVDS data
LR_2P5_1n	A13	6	3.3V	LVDS data
LR_2P5_2p	D11	6	3.3V	LVDS data
LR_2P5_2n	C11	6	3.3V	LVDS data
LR_2P5_CLKp	B14	6	3.3V	LVDS Clock
LR_2P5_CLKn	A14	6	3.3V	LVDS Clock
LR_2P5_3p	B11	6	3.3V	LVDS data
LR_2P5_3n	B12	6	3.3V	LVDS data
LR_2P5_4p	A11	6	3.3V	LVDS data
LR_2P5_4n	A12	6	3.3V	LVDS data

3.6 MIPI Interface

3.6.1 Introduction

The MIPI interface on the development board uses 80pin AXK580147YG connector with 0.5 mm pitch. Lead out MIPI DPHY RX/TX hardcore signal (4 data + 1 clk) and 4 GPIOs from FPGA. The interface circuit diagram is shown in Figure 3-5.

Figure 3-5 Schematic of MIPI Interface



3.6.2 Pin Distribution

Table 3-5 Pin Distribution of MIPI Interface

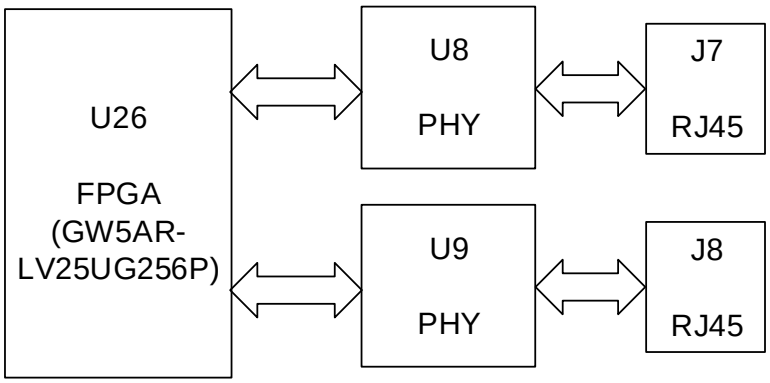
Signal Name	FPGA (U1) Pin No.	BANK	I/O Level	Description
M0_D0n	B7	MIPI	-	MIPI data signal
M0_D0p	A7	MIPI	-	MIPI data signal
M0_D1n	B6	MIPI	-	MIPI data signal
M0_D1p	A6	MIPI	-	MIPI data signal
M0_CKn	B5	MIPI	-	MIPI clock signal
M0_CKp	A5	MIPI	-	MIPI clock signal
M0_D2n	B4	MIPI	-	MIPI data signal
M0_D2p	A4	MIPI	-	MIPI data signal
M0_D3n	B3	MIPI	-	MIPI data signal
M0_D3p	A3	MIPI	-	MIPI data signal
FM_GPIO1	D5	5	3.3V	GPIO
FM_GPIO2	E5	5	3.3V	GPIO
FM_GPIO3	F5	5	3.3V	GPIO
FM_GPIO4	G5	5	3.3V	GPIO

3.7 Ethernet Interface

3.7.1 Introduction

The development board provides 2-channel Ethernet interfaces, supporting RGMII (10BASE-T/100BASE-TX/1000BASE-T) interfaces. Use the RJ45 connector integrated with network transformer internally. The connection diagram is shown in Figure 3-6.

Figure 3-6 Ethernet Interface Connection Diagram



3.7.2 Pin Distribution

Table 3-6 Pin Distribution of Ethernet Interface 1

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
PHY1_TXD0	H1	5	3.3V	RGMII transmit data
PHY1_TXD1	H3	4	3.3V	RGMII transmit data
PHY1_TXD2	H4	4	3.3V	RGMII transmit data
PHY1_TXD3	J1	4	3.3V	RGMII transmit data
PHY1_GTXCLK	F3	5	3.3V	RGMII transmit clock
PHY1_TXEN	J3	4	3.3V	RGMII transmit data enable
PHY1_RXD0	K1	4	3.3V	RGMII/MII receive data
PHY1_RXD1	K2	4	3.3V	RGMII/MII receive data
PHY1_RXD2	M1	4	3.3V	RGMII/MII receive data
PHY1_RXD3	M2	4	3.3V	RGMII/MII receive data
PHY1_RXC	J2	4	3.3V	RGMII receive clock
PHY1_RXDV	N1	4	3.3V	RGMII receive data enable
PHY_MDIO	G1	5	3.3V	Manage channel data
PHY_MDC	F2	5	3.3V	Manage channel clock
PHY_RST_N	G2	5	3.3V	Reset signal

Table 3-7 Pin Distribution of Ethernet Interface 2

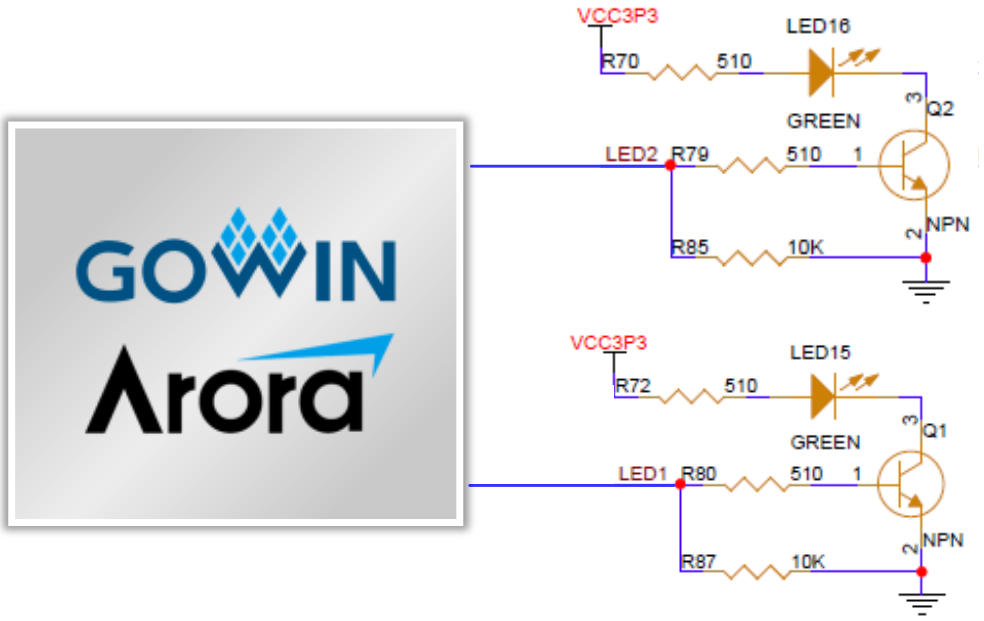
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
PHY2_TXD0	T3	2	3.3V	RGMII transmit data
PHY2_TXD1	T4	2	3.3V	RGMII transmit data
PHY2_TXD2	J4	4	3.3V	RGMII transmit data
PHY2_TXD3	R5	2	3.3V	RGMII transmit data
PHY2_GTXCLK	T2	2	3.3V	RGMII transmit clock
PHY2_TXEN	N5	3	3.3V	RGMII transmit data enable
PHY2_RXD0	K5	3	3.3V	RGMII/MII receive data
PHY2_RXD1	J5	3	3.3V	RGMII/MII receive data
PHY2_RXD2	T6	2	3.3V	RGMII/MII receive data
PHY2_RXD3	R6	2	3.3V	RGMII/MII receive data
PHY2_RXC	T5	2	3.3V	RGMII receive clock
PHY2_RXDV	P6	2	3.3V	RGMII receive data enable
PHY_MDIO	G1	5	3.3V	Manage channel data
PHY_MDC	F2	5	3.3V	Manage channel clock
PHY_RST_N	G2	5	3.3V	Reset signal

3.8 LED & Key

3.8.1 Introduction

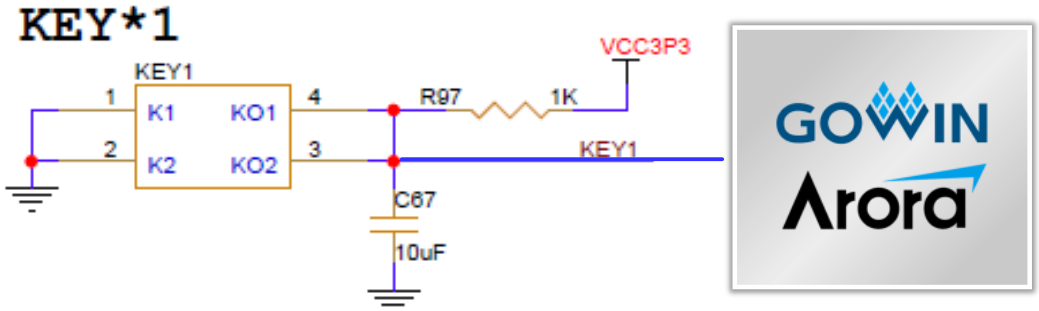
The development board includes two user LEDs. The user LEDs are connected to the IO of FPGA BANK5 and can be switched on and off via the program. The user LEDs will be on when the IO voltage is high. The user LEDs will be off when the IO voltage is low. The connection diagram is shown in Figure 3-7 .

Figure 3-7 LED Schematic



There is one user key on the development board. The user key is connected to the general IO of FPGA BANK0. The corresponding IO input voltage of the FPGA is low when the key is pressed while high when the key is not pressed. The key circuit is equipped with hardware debounce. The connection diagram is shown in Figure 3-8**.**

Figure 3-8 Connection Diagram of Key



3.8.2 Pin Distribution

Table 3-8 LED Pin Distribution

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
LED1	F4	5	3.3V	LED
LED2	D4	5	3.3V	LED

Table 3-9 Pin Distribution of Key

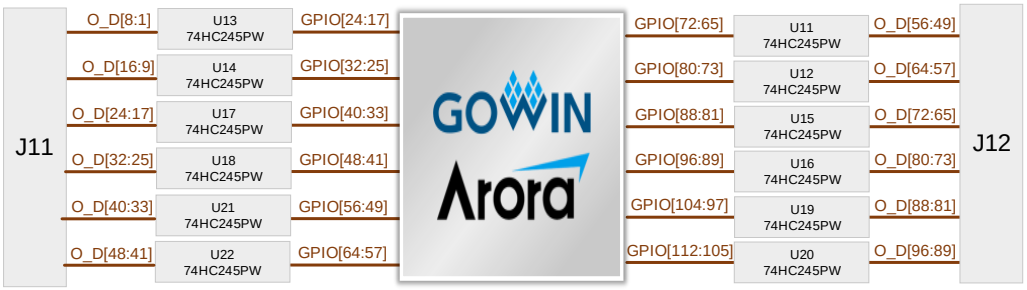
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
KEY1	K15	0	3.3V	Key

3.9 GPIO

3.9.1 Introduction

The FPGA on the development board connects to the J11 and J12 interfaces through a bus transceiver to externally lead to 5V level output GPIOs. The schematic of GPIO interfaces is shown in below.

Figure 3-9 Schematic of GPIO Interface



3.9.2 Pin Distribution

Table 3-10 J11 Pin Distribution for GPIO Interface

J11 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	O_D1	H5	5	3.3V	Output
2	O_D2	E6	5	3.3V	Output
3	O_D3	F6	5	3.3V	Output
4	O_D4	C6	6	3.3V	Output
5	O_D5	D6	6	3.3V	Output
6	O_D6	E7	6	3.3V	Output
7	O_D7	F7	6	3.3V	Output
8	O_D8	E8	6	3.3V	Output
9	O_D9	A15	6	3.3V	Output
10	O_D10	B16	6	3.3V	Output
11	GND	-	-	-	GND
12	GND	-	-	-	GND

J11 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
13	O_D11	C15	7	3.3V	Output
14	O_D12	C16	7	3.3V	Output
15	O_D13	D15	7	3.3V	Output
16	O_D14	D16	7	3.3V	Output
17	O_D15	E15	7	3.3V	Output
18	O_D16	E16	7	3.3V	Output
19	O_D17	G16	7	3.3V	Output
20	O_D18	H14	7	3.3V	Output
21	O_D19	J16	7	3.3V	Output
22	O_D20	J15	7	3.3V	Output
23	GND	-	-	-	GND
24	GND	-	-	-	GND
25	O_D21	K16	0	3.3V	Output
26	O_D22	L16	0	3.3V	Output
27	O_D23	L15	0	3.3V	Output
28	O_D24	M16	0	3.3V	Output
29	O_D25	N16	0	3.3V	Output
30	O_D26	N15	0	3.3V	Output
31	O_D27	P16	0	3.3V	Output
32	O_D28	P15	0	3.3V	Output
33	O_D29	R16	0	3.3V	Output
34	O_D30	T13	2	3.3V	Output
35	GND	-	-	-	GND
36	GND	-	-	-	GND
37	O_D31	R12	2	3.3V	Output
38	O_D32	T12	2	3.3V	Output
39	O_D33	R11	2	3.3V	Output
40	O_D34	T11	2	3.3V	Output
41	O_D35	R10	2	3.3V	Output
42	O_D36	T10	2	3.3V	Output

J11 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
43	O_D37	T9	2	3.3V	Output
44	O_D38	R9	2	3.3V	Output
45	O_D39	T8	2	3.3V	Output
46	O_D40	R8	2	3.3V	Output
47	GND	-	-	-	GND
48	GND	-	-	-	GND
49	O_D41	N9	2	3.3V	Output
50	O_D42	M9	0	3.3V	Output
51	O_D43	M8	3	3.3V	Output
52	O_D44	P8	2	3.3V	Output
53	O_D45	N8	2	3.3V	Output
54	O_D46	N6	2	3.3V	Output
55	O_D47	T7	2	3.3V	Output
56	O_D48	R7	2	3.3V	Output
57	GND	-	-	-	GND
58	GND	-	-	-	GND
59	VCC3P3	-	-	3.3V	POWER
60	VCC3P3	-	-	3.3V	POWER

Table 3-11 J12 Pin Distribution for GPIO Interface

J12 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	O_D49	F8	6	3.3V	Output
2	O_D50	E9	7	3.3V	Output
3	O_D51	F9	7	3.3V	Output
4	O_D52	E10	7	3.3V	Output
5	O_D53	F10	7	3.3V	Output
6	O_D54	E11	7	3.3V	Output
7	O_D55	F11	7	3.3V	Output
8	O_D56	G11	7	3.3V	Output
9	O_D57	C14	7	3.3V	Output
10	O_D58	D12	7	3.3V	Output
11	GND	-	-	-	GND
12	GND	-	-	-	GND
13	O_D59	D14	7	3.3V	Output
14	O_D60	F13	7	3.3V	Output
15	O_D61	F14	7	3.3V	Output
16	O_D62	F15	7	3.3V	Output
17	O_D63	F16	7	3.3V	Output
18	O_D64	G15	7	3.3V	Output
19	O_D65	J12	7	3.3V	Output
20	O_D66	J13	7	3.3V	Output
21	O_D67	J14	7	3.3V	Output
22	O_D68	K12	0	3.3V	Output
23	GND	-	-	-	GND
24	GND	-	-	-	GND
25	O_D69	L13	0	3.3V	Output
26	O_D70	L14	0	3.3V	Output
27	O_D71	L12	0	3.3V	Output
28	O_D72	M15	0	3.3V	Output
29	O_D73	J11	0	3.3V	Output

J12 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
30	O_D74	K11	0	3.3V	Output
31	O_D75	L11	0	3.3V	Output
32	O_D76	M12	0	3.3V	Output
33	O_D77	N12	0	3.3V	Output
34	O_D78	N13	0	3.3V	Output
35	GND	-	-	-	GND
36	GND	-	-	-	GND
37	O_D79	N14	0	3.3V	Output
38	O_D80	P14	0	3.3V	Output
39	O_D81	K10	0	3.3V	Output
40	O_D82	M11	0	3.3V	Output
41	O_D83	L9	0	3.3V	Output
42	O_D84	N11	2	3.3V	Output
43	O_D85	P11	2	3.3V	Output
44	O_D86	M10	0	3.3V	Output
45	O_D87	L10	0	3.3V	Output
46	O_D88	P9	2	3.3V	Output
47	GND	-	-	-	GND
48	GND	-	-	-	GND
49	O_D89	K6	3	3.3V	Output
50	O_D90	K8	3	3.3V	Output
51	O_D91	L7	3	3.3V	Output
52	O_D92	L8	3	3.3V	Output
53	O_D93	L6	3	3.3V	Output
54	O_D94	M7	3	3.3V	Output
55	O_D95	M6	3	3.3V	Output
56	O_D96	K9	0	3.3V	Output
57	GND	-	-	-	GND
58	GND	-	-	-	GND
59	VCC5P0	-	-	5V	POWER

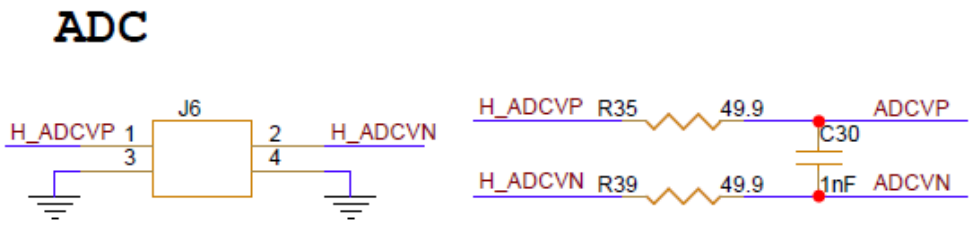
J12 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
60	VCC5P0	-	-	5V	POWER

3.10 ADC Interface

3.10.1 Introduction

The development board includes input interfaces for ADC signals. The connector uses a 2x2P pin header with 2.54mm pitch. Figure 3-10 is the ADC interface schematic diagram and the anti-aliasing filter circuit.

Figure 3-10 Schematic of ADC Interface



3.10.2 Pin Distribution

Table 3-12 ADC Interface Pinout

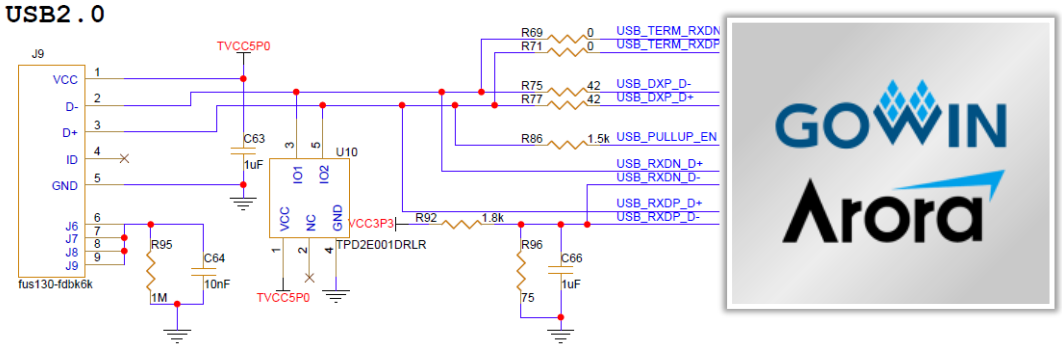
Signal Name	FPGA Pin No.	BANK	IO Level	Description
H_ADCVP	R3	3	3.3V	Analog signal input
H_ADCVN	R4	3	3.3V	Analog signal input

3.11 USB 2.0 Interface

3.11.1 Introduction

The development board implements the USB 2.0 interface through the Mini USB-B connector and includes the ESD protection circuit for communication between the FPGA and external devices.

Figure 3-11 Schematic of USB 2.0 Interface



3.11.2 Pin Distribution

Table 3-13 Pin Distribution of USB 2.0 Interface

Signal Name	FPGA (U1) Pin No.	BANK	IO Level	Description
USB_TERM_RXDN	C2	5	3.3V	Terminal resistance control at high speed, USB data pin at full speed and low speed
USB_TERM_RXDP	C3	5	3.3V	Terminal resistance control at high speed, USB data pin at full speed and low speed
USB_DXP_D-	B1	5	3.3V	USB data pin at high speed
USB_DXP_D+	C1	5	3.3V	USB data pin at high speed
USB_PULLUP_EN	F1	5	3.3V	Pull-up
USB_RXDN_D+	D3	5	3.3V	USB- signal
USB_RXDN_D-	D2	5	3.3V	USB+ Reference signal
USB_RXDP_D+	E1	5	3.3V	USB+ signal
USB_RXDP_D-	D1	5	3.3V	USB- Reference signal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