DK_START_GW5AST-LV138FPG676A_V1.0 Daughter Board

User guide

DBUG1272-1.0.1E, 11/01/2024

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Revision History

Date	Version	Description
07/22/2024	1.0E	Initial version published.
11/01/2024	1.0.1E	The SDI daughter board renamed.

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1 About This Guide

1.1 Purpose

The DK_START_GW5AST-LV138FPG676A_V1.0 Daughter Board User Guide describes the five daughter boards for the DK_START_GW5AST-LV138FPG676A_V1.0:

1. EVAL_GW5AT-LV138KFPG676ES_Dcard_IES_V1.0 (hereinafter referred to as IES daughter board)
2. EVAL_GW5AT-LV138FPG676_Dcard_SDI_SGMII_V2.1 (hereinafter referred to as SDI daughter board)
3. EVAL_GW5AT-LV138KFPG676ES_Dcard_MIPI-RX_ISP_V1.0 (hereinafter referred to as ISP daughter board)
4. EVAL_GW5AT-LV138KFPG676ES_Dcard_DVI_SLVS_V1.0 (hereinafter referred to as DVI daughter board)
5. EVAL_GW5AT-LV138KFPG676ES_Dcard_EDP_HDMI_V1.0 (hereinafter referred to as EDP daughter board)

Each set of daughter board describes the following three sections:

1. A brief introduction to the features of the daughter board.
2. An introduction to the system architecture and hardware resources of the daughter board.
3. An introduction to the functions, circuits, and pin distributions of each hardware circuit of the daughter board.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- DS981, Arora V 138K & 75K FPGA Products Data Sheet
- UG986, GW5AST-138 Pinout
- UG1102, GW5AST series of FPGA Products Package and Pinout User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
IES	Gowin Industrial Ethernet System
HDMI	High Definition Multimedia Interface
SDI	Serial Digital Interface
SGMII	Serial Gigabit Media Independent Interface
MIPI	Mobile Industry Processor Interface
ISP	Image Signal Processing
DVI	Digital Visual Interface
SLVS	Scalable Low Voltage Signaling
EDP	Embedded Display Port
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable Input/Output
LVDS	Low-Voltage Differential Signaling

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

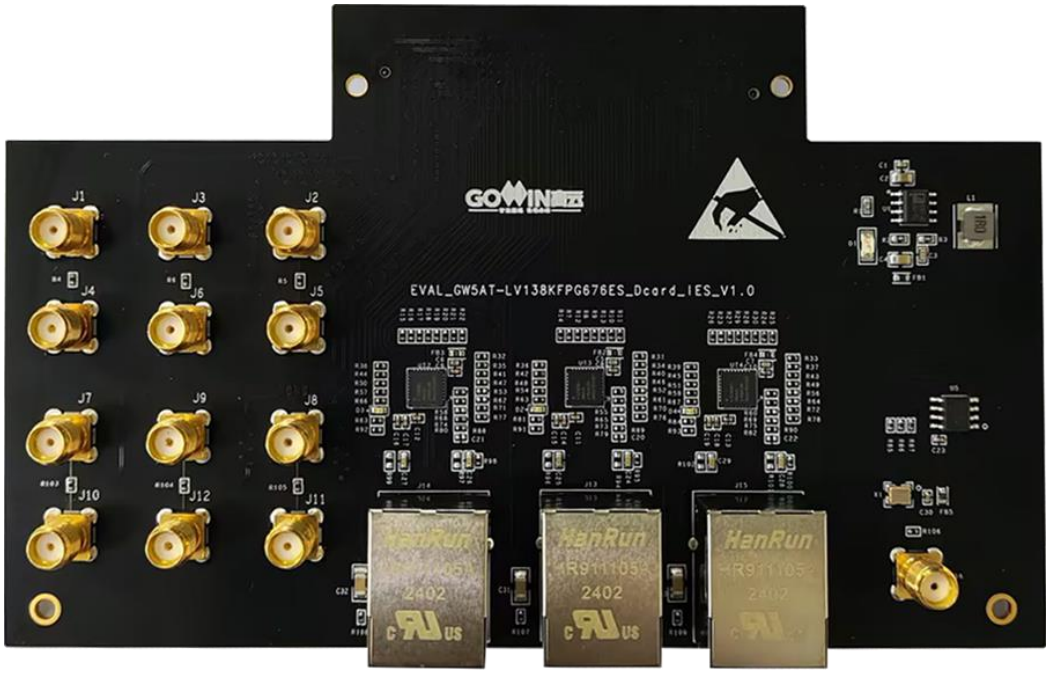
E-mail: support@gowinsemi.com

2 IES Daughter Board

2.1 Introduction

2.1.1 Overview

Figure 2-1 EVAL_GW5AT-LV138KFPG676ES_Dcard_IES_V1.0 Daughter Board



The IES daughter board needs to be used with the DK_START_GW5AST-LV138FPG676A_V1.0 motherboard, primarily for Ethernet communication, LVDS communication, and IES evaluation.

2.1.2 A Daughter Board Kit

The daughter board kit includes the following item:

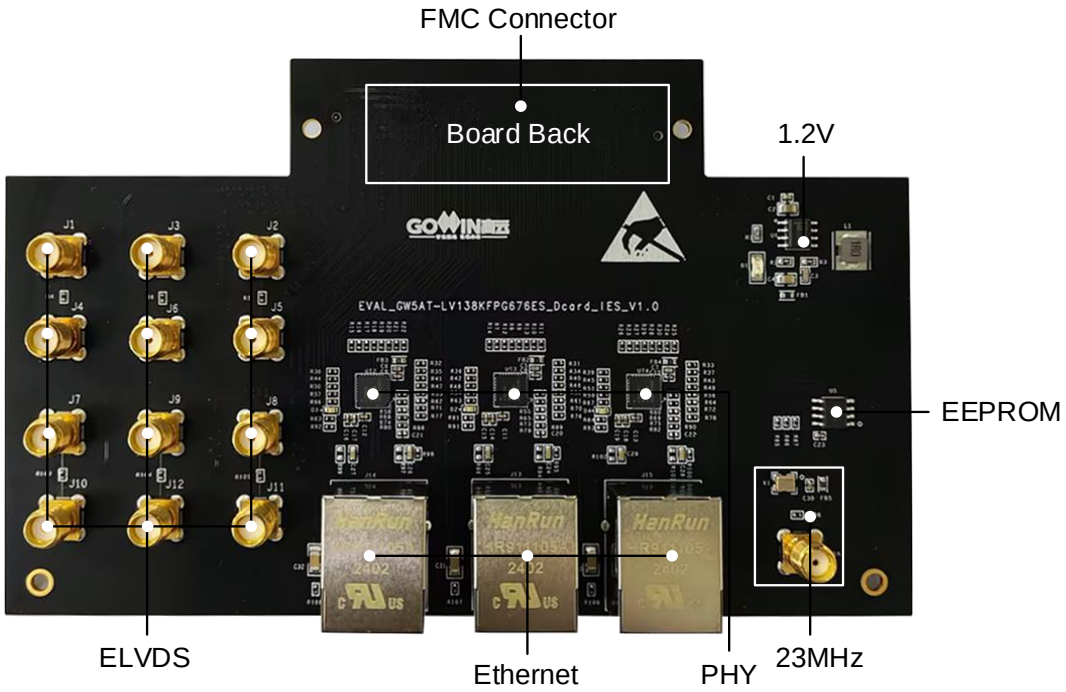
- EVAL_GW5AT-LV138KFPG676ES_Dcard_IES_V1.0 daughter board

Figure 2-2 A Daughter Board Kit

① EVAL_GW5AT-LV138KFPG676ES_Dcard_IES_V1.0 daughter board

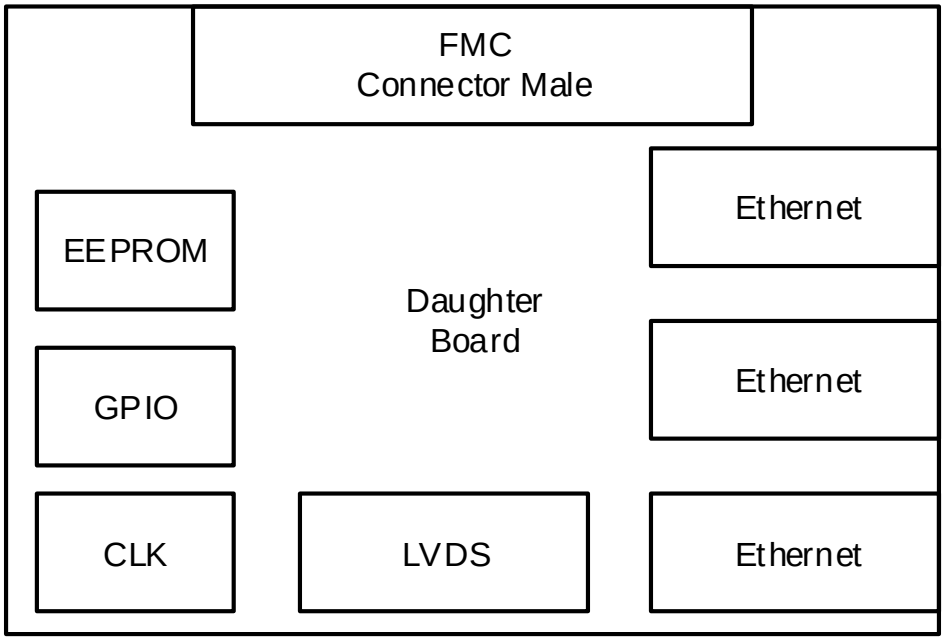
2.1.3 PCB Components

Figure 2-3 PCB Components



2.1.4 System Block Diagram

Figure 2-4 System Block Diagram



2.1.5 Features

The key features are as follows:

1. Power
   - The motherboard provides DC 3.3V power
   - The green Power light is on after power on
2. Clock system
   - One 25MHz single port clock
3. Memory
   - 32Kbit EEPROM
4. Ethernet
   - Three Ethernet interfaces
   - Support MII interfaces (10Base-T/100Base-TX)
   - RJ45 connector integrated with network transformer internally
5. ELVDS interface
   - ELVDS interface, including six pairs of differential signals
6. Board-to-board connector
   - Use 400Pin FMC connector with 1.27mm pitch
   - Communicate with the DK_START_GW5AST-LV138FPG676A_V1.0 motherboard

2.2 Daughter Board Circuit

2.2.1 Power Supply

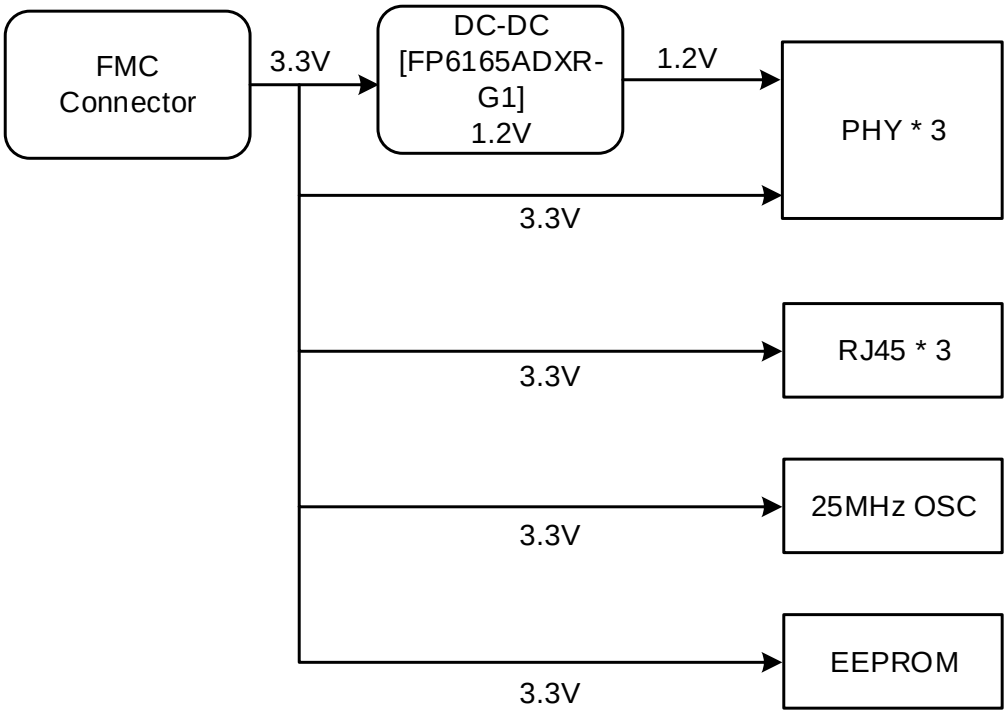
2.2.1.1 Introduction

The motherboard supplies 3.3V power to the daughter board through the FMC connector.

The input 3.3V power generates a 1.2V power supply through the power chip on the IES daughter board to meet the power requirements of the IES daughter board.

2.2.1.2 Power System Distribution

Figure 2-5 Power Supply System Distribution

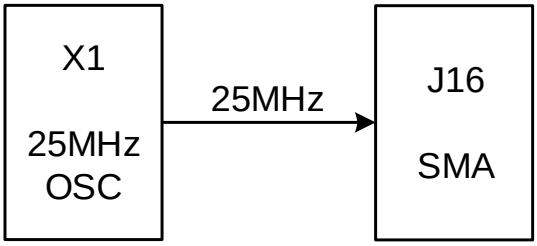


2.2.2 Clock

2.2.2.1 Introduction

The daughter board provides one 25MHz single-ended clock output via SMA interfaces.

Figure 2-6 Clock Connection Diagram



2.2.2.2 Pin Distribution

Table 2-1 Clock Pin Distribution

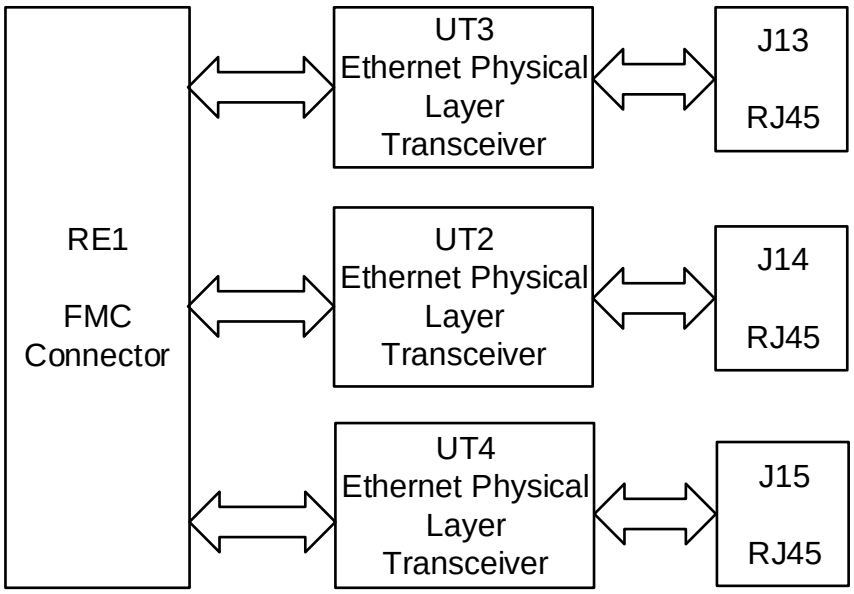
Device Number	Signal Name	Description
J16	25MHz	25MHz single-ended clock

2.2.3 Ethernet

2.2.3.1 Introduction

The IES daughter board provides three Ethernet interfaces, supporting 10BASE-T/100BASE-TX modes. Use the RJ45 connector integrated with network transformer internally. The connection diagram is as follows.

Figure 2-7 Ethernet Interface Connection Diagram



2.2.3.2 Pin Distribution

Table 2-2 Ethernet Interface J13 Pin Distribution

J13 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	TD+	--	--	--	Transmit data
2	TD-	--	--	--	Transmit data
3	RD+	--	--	--	Receive data
4	GND	--	--	--	GND
5	GND	--	--	--	GND
6	RD-	--	--	--	Receive data
7	NC	--	--	--	Floating
8	GND	--	--	--	GND
9	VCC3P3	--	--	3.3V	Power
10	F_PHY2_LINKACT0	W24	2	3.3V	Connection/active status indicator
11	NC	--	--	--	Floating
12	NC	--	--	--	Floating

Table 2-3 Ethernet Interface J14 Pin Distribution

J14 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	TD+	--	--	--	Transmit data
2	TD-	--	--	--	Transmit data
3	RD+	--	--	--	Receive data
4	GND	--	--	--	GND
5	GND	--	--	--	GND
6	RD-	--	--	--	Receive data
7	NC	--	--	--	Floating
8	GND	--	--	--	GND
9	VCC3P3	--	--	3.3V	Power
10	F_PHY1_LINKACT0	U26	2	3.3V	Connection/active status indicator
11	NC	--	--	--	Floating

J14 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
12	NC	--	--	--	Floating

Table 2-4 Ethernet Interface J15 Pin Distribution

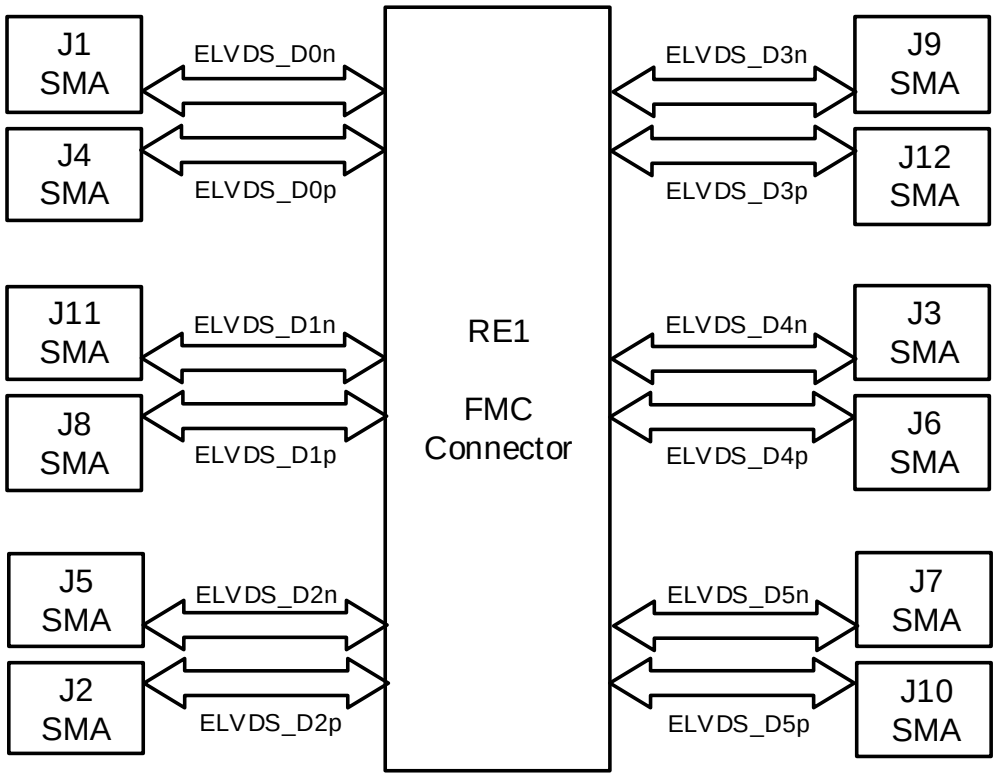
J15 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	TD+	--	--	--	Transmit data
2	TD-	--	--	--	Transmit data
3	RD+	--	--	--	Receive data
4	GND	--	--	--	GND
5	GND	--	--	--	GND
6	RD-	--	--	--	Receive data
7	NC	--	--	--	Floating
8	GND	--	--	--	GND
9	VCC3P3	--	--	3.3V	Power
10	F_PHY3_LINKACT0	G22	4	3.3V	Connection/active status indicator
11	NC	--	--	--	Floating
12	NC	--	--	--	Floating

2.2.4 ELVDS interface

2.2.4.1 Introduction

The ELVDS interfaces provided by the IES daughter board are SMA females containing six pairs of differential signals. The connection diagram is as follows.

Figure 2-8 Connection Diagram of ELVDS Interface



2.2.4.2 Pin Distribution

Table 2-5 ELVDS Interface Pin Distribution

Device Number	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
J1	ELVDS_D0n	F19	5	3.3V	ELVDS differential signal 0-
J4	ELVDS_D0p	F18	5	3.3V	ELVDS differential signal 0+
J11	ELVDS_D1n	D21	5	3.3V	ELVDS differential signal 1-
J8	ELVDS_D1p	E21	5	3.3V	ELVDS differential signal 1+
J5	ELVDS_D2n	F20	5	3.3V	ELVDS differential signal 2-
J2	ELVDS_D2p	G19	5	3.3V	ELVDS differential signal 2+
J9	ELVDS_D3n	A22	5	3.3V	ELVDS differential signal 3-
J12	ELVDS_D3p	B22	5	3.3V	ELVDS differential signal 3+
J3	ELVDS_D4n	E18	5	3.3V	ELVDS differential signal 4-
J6	ELVDS_D4p	E17	5	3.3V	ELVDS differential signal 4+
J7	ELVDS_D5n	C18	5	3.3V	ELVDS differential signal 5-
J10	ELVDS_D5p	D18	5	3.3V	ELVDS differential signal 5+

2.2.5 Board-to-board connector

2.2.5.1 Introduction

The IES daughter board has a 400Pin FMC board-to-board connector with 1.27mm pitch for communication with the DK_START_GW5AST-LV138FPG676A_V1.0 motherboard.

2.2.5.2 Pin Distribution

Table 2-6 Pin Distribution for RE1 Board-to-Board Connector

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
A1	GND	--	--	--	GND
A2	NC	--	--	--	Floating
A3	NC	--	--	--	Floating
A4	GND	--	--	--	GND
A5	GND	--	--	--	GND
A6	NC	--	--	--	Floating
A7	NC	--	--	--	Floating
A8	GND	--	--	--	GND
A9	GND	--	--	--	GND
A10	NC	--	--	--	Floating
A11	NC	--	--	--	Floating
A12	GND	--	--	--	GND
A13	GND	--	--	--	GND
A14	NC	--	--	--	Floating
A15	NC	--	--	--	Floating
A16	GND	--	--	--	GND
A17	GND	--	--	--	GND
A18	NC	--	--	--	Floating
A19	NC	--	--	--	Floating
A20	GND	--	--	--	GND
A21	GND	--	--	--	GND
A22	NC	--	--	--	Floating
A23	NC	--	--	--	Floating

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
A24	GND	--	--	--	GND
A25	GND	--	--	--	GND
A26	NC	--	--	--	Floating
A27	NC	--	--	--	Floating
A28	GND	--	--	--	GND
A29	GND	--	--	--	GND
A30	NC	--	--	--	Floating
A31	NC	--	--	--	Floating
A32	GND	--	--	--	GND
A33	GND	--	--	--	GND
A34	NC	--	--	--	Floating
A35	NC	--	--	--	Floating
A36	GND	--	--	--	GND
A37	GND	--	--	--	GND
A38	NC	--	--	--	Floating
A39	NC	--	--	--	Floating
A40	GND	--	--	--	GND
B1	NC	--	--	--	Floating
B2	GND	--	--	--	GND
B3	GND	--	--	--	GND
B4	NC	--	--	--	Floating
B5	NC	--	--	--	Floating
B6	GND	--	--	--	GND
B7	GND	--	--	--	GND
B8	NC	--	--	--	Floating
B9	NC	--	--	--	Floating
B10	GND	--	--	--	GND
B11	GND	--	--	--	GND
B12	NC	--	--	--	Floating
B13	NC	--	--	--	Floating

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
B14	GND	--	--	--	GND
B15	GND	--	--	--	GND
B16	NC	--	--	--	Floating
B17	NC	--	--	--	Floating
B18	GND	--	--	--	GND
B19	GND	--	--	--	GND
B20	NC	--	--	--	Floating
B21	NC	--	--	--	Floating
B22	GND	--	--	--	GND
B23	GND	--	--	--	GND
B24	NC	--	--	--	Floating
B25	NC	--	--	--	Floating
B26	GND	--	--	--	GND
B27	GND	--	--	--	GND
B28	NC	--	--	--	Floating
B29	NC	--	--	--	Floating
B30	GND	--	--	--	GND
B31	GND	--	--	--	GND
B32	NC	--	--	--	Floating
B33	NC	--	--	--	Floating
B34	GND	--	--	--	GND
B35	GND	--	--	--	GND
B36	NC	--	--	--	Floating
B37	NC	--	--	--	Floating
B38	GND	--	--	--	GND
B39	GND	--	--	--	GND
B40	NC	--	--	--	Floating
C1	GND	--	--	--	GND
C2	NC	--	--	--	Floating
C3	NC	--	--	--	Floating

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
C4	GND	--	--	--	GND
C5	GND	--	--	--	GND
C6	NC	--	--	--	Floating
C7	NC	--	--	--	Floating
C8	GND	--	--	--	GND
C9	GND	--	--	--	GND
C10	ELVDS_D0p	F18	5	3.3V	ELVDS differential signal 0+
C11	ELVDS_D0n	F19	5	3.3V	ELVDS differential signal 0-
C12	GND	--	--	--	GND
C13	GND	--	--	--	GND
C14	NC	--	--	--	Floating
C15	NC	--	--	--	Floating
C16	GND	--	--	--	GND
C17	GND	--	--	--	GND
C18	NC	--	--	--	Floating
C19	NC	--	--	--	Floating
C20	GND	--	--	--	GND
C21	GND	--	--	--	GND
C22	F_PHY_MDC	G20	4	3.3V	MII clock input
C23	F_PHY_MDIO	G21	4	3.3V	MII data input/output
C24	GND	--	--	--	GND
C25	GND	--	--	--	GND
C26	NC	--	--	--	Floating
C27	NC	--	--	--	Floating
C28	GND	--	--	--	GND
C29	GND	--	--	--	GND
C30	NC	--	--	--	Floating
C31	NC	--	--	--	Floating

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
C32	GND	--	--	--	GND
C33	GND	--	--	--	GND
C34	GND	--	--	--	GND
C35	NC	--	--	--	Floating
C36	GND	--	--	--	GND
C37	NC	--	--	--	Floating
C38	GND	--	--	--	GND
C39	VCC3P3	--	--	--	Power
C40	GND	--	--	--	GND
D1	NC	--	--	--	Floating
D2	GND	--	--	--	GND
D3	GND	--	--	--	GND
D4	NC	--	--	--	Floating
D5	NC	--	--	--	Floating
D6	GND	--	--	--	GND
D7	GND	--	--	--	GND
D8	ELVDS_D4p	E17	5	3.3V	ELVDS differential signal 4+
D9	ELVDS_D4n	E18	5	3.3V	ELVDS differential signal 4-
D10	GND	--	--	--	GND
D11	ELVDS_D2p	G19	5	3.3V	ELVDS differential signal 2+
D12	ELVDS_D2n	F20	5	3.3V	ELVDS differential signal 2-
D13	GND	--	--	--	GND
D14	NC	--	--	--	Floating
D15	NC	--	--	--	Floating
D16	GND	--	--	--	GND
D17	NC	--	--	--	Floating
D18	NC	--	--	--	Floating

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
D19	GND	--	--	--	GND
D20	NC	--	--	--	Floating
D21	NC	--	--	--	Floating
D22	GND	--	--	--	GND
D23	NC	--	--	--	Floating
D24	NC	--	--	--	Floating
D25	GND	--	--	--	GND
D26	NC	--	--	--	Floating
D27	F_PHY3_RXER	L18	4	3.3V	MII receiving error
D28	GND	--	--	--	GND
D29	NC	--	--	--	Floating
D30	NC	--	--	--	Floating
D31	NC	--	--	--	Floating
D32	NC	--	--	--	Floating
D33	NC	--	--	--	Floating
D34	NC	--	--	--	Floating
D35	NC	--	--	--	Floating
D36	VCC3P3	--	--	--	Power
D37	GND	--	--	--	GND
D38	VCC3P3	--	--	--	Power
D39	GND	--	--	--	GND
D40	VCC3P3	--	--	--	Power
E1	GND	--	--	--	GND
E2	NC	--	--	--	Floating
E3	NC	--	--	--	Floating
E4	GND	--	--	--	GND
E5	GND	--	--	--	GND
E6	F_PHY1_RST_n	V23	2	3.3V	Chip reset
E7	F_PHY1_CRS	W23	2	3.3V	MII carrier sense
E8	GND	--	--	--	GND

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
E9	F_PHY1_TXD2	V19	2	3.3V	MII transmit data
E10	F_PHY1_TXD1	W19	2	3.3V	MII transmit data
E11	GND	--	--	--	GND
E12	F_PHY1_TXD0	AA22	2	3.3V	MII transmit data
E13	F_PHY1_TXEN	AA23	2	3.3V	MII transmit enable
E14	GND	--	--	--	GND
E15	F_PHY1_RXC	Y25	2	3.3V	MII receive clock
E16	F_PHY1_RXDV	AA25	2	3.3V	MII receive data, valid
E17	GND	--	--	--	GND
E18	F_PHY1_RXD1	V26	2	3.3V	MII receive data
E19	F_PHY1_RXD2	W26	2	3.3V	MII receive data
E20	GND	--	--	--	GND
E21	NC	--	--	--	Floating
E22	NC	--	--	--	Floating
E23	GND	--	--	--	GND
E24	NC	--	--	--	Floating
E25	NC	--	--	--	Floating
E26	GND	--	--	--	GND
E27	NC	--	--	--	Floating
E28	NC	--	--	--	Floating
E29	GND	--	--	--	GND
E30	NC	--	--	--	Floating
E31	NC	--	--	--	Floating
E32	GND	--	--	--	GND
E33	NC	--	--	--	Floating
E34	NC	--	--	--	Floating
E35	GND	--	--	--	GND
E36	NC	--	--	--	Floating
E37	NC	--	--	--	Floating

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
E38	GND	--	--	--	GND
E39	NC	--	--	--	Floating
E40	GND	--	--	--	GND
F1	NC	--	--	--	Floating
F2	GND	--	--	--	GND
F3	GND	--	--	--	GND
F4	F_PHY1_CLK	U21	2	3.3V	External clock input
F5	F_PHY1_Link	V21	2	3.3V	Connection status indicator
F6	GND	--	--	--	GND
F7	F_PHY1_COL	V16	2	3.3V	MII collision detection
F8	F_PHY1_TXD3	V17	2	3.3V	MII transmit data
F9	GND	--	--	--	GND
F10	NC	--	--	--	Floating
F11	F_PHY1_RXD3	Y20	2	3.3V	MII receive data
F12	GND	--	--	--	GND
F13	F_PHY1_TXC	AB24	2	3.3V	MII transmit clock
F14	F_PHY1_RXER	AC24	2	3.3V	MII receiving error
F15	GND	--	--	--	GND
F16	F_PHY2_RXER	AB26	2	3.3V	MII receiving error
F17	F_PHY1_RXD0	AC26	2	3.3V	MII receive data
F18	GND	--	--	--	GND
F19	NC	--	--	--	Floating
F20	F_PHY1_LINKACT0	U26	2	3.3V	Connection/active status indicator
F21	GND	--	--	--	GND
F22	NC	--	--	--	Floating
F23	NC	--	--	--	Floating
F24	GND	--	--	--	GND

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F25	NC	--	--	--	Floating
F26	NC	--	--	--	Floating
F27	GND	--	--	--	GND
F28	NC	--	--	--	Floating
F29	NC	--	--	--	Floating
F30	GND	--	--	--	GND
F31	NC	--	--	--	Floating
F32	NC	--	--	--	Floating
F33	GND	--	--	--	GND
F34	NC	--	--	--	Floating
F35	NC	--	--	--	Floating
F36	GND	--	--	--	GND
F37	NC	--	--	--	Floating
F38	NC	--	--	--	Floating
F39	GND	--	--	--	GND
F40	NC	--	--	--	Floating
G1	GND	--	--	--	GND
G2	NC	--	--	--	Floating
G3	NC	--	--	--	Floating
G4	GND	--	--	--	GND
G5	GND	--	--	--	GND
G6	ELVDS_D5p	D18	5	3.3V	ELVDS differential signal 5+
G7	ELVDS_D5n	C18	5	3.3V	ELVDS differential signal 5-
G8	GND	--	--	--	GND
G9	ELVDS_D1p	E12	5	3.3V	ELVDS differential signal 1+
G10	ELVDS_D1n	D12	5	3.3V	ELVDS differential signal 1-
G11	GND	--	--	--	GND

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
G12	NC	--	--	--	Floating
G13	NC	--	--	--	Floating
G14	GND	--	--	--	GND
G15	NC	--	--	--	Floating
G16	NC	--	--	--	Floating
G17	GND	--	--	--	GND
G18	NC	--	--	--	Floating
G19	NC	--	--	--	Floating
G20	GND	--	--	--	GND
G21	F_PHY3_RST_n	M16	4	3.3V	On-chip reset
G22	F_PHY3_TXD3	M17	4	3.3V	MII transmit data
G23	GND	--	--	--	GND
G24	F_PHY3_TXD2	J24	4	3.3V	MII transmit data
G25	F_PHY3_TXD0	H24	4	3.3V	MII transmit data
G26	GND	--	--	--	GND
G27	F_PHY3_TXC	G24	4	3.3V	MII transmit clock
G28	F_PHY3_RXC	F24	4	3.3V	MII receive clock
G29	GND	--	--	--	GND
G30	F_PHY3_RXD0	U25	4	3.3V	MII receive data
G31	F_PHY3_RXD2	D25	4	3.3V	MII receive data
G32	GND	--	--	--	GND
G33	F_PHY3_LINKACT0	G22	4	3.3V	Connection/active status indicator
G34	F_PHY3_RXD3	F22	4	3.3V	MII receive data
G35	GND	--	--	--	GND
G36	F_A2	J19	4	3.3V	Chip address A2
G37	F_SDA	H19	4	3.3V	Serial address/data I/O
G38	GND	--	--	--	GND
G39	NC	--	--	--	Floating
G40	GND	--	--	--	GND

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
H1	NC	--	--	--	Floating
H2	NC	--	--	--	Floating
H3	GND	--	--	--	GND
H4	NC	--	--	--	Floating
H5	NC	--	--	--	Floating
H6	GND	--	--	--	GND
H7	ELVDS_D3p	B22	5	3.3V	ELVDS differential signal 3+
H8	ELVDS_D3n	A22	5	3.3V	ELVDS differential signal 3-
H9	GND	--	--	--	GND
H10	NC	--	--	--	Floating
H11	NC	--	--	--	Floating
H12	GND	--	--	--	GND
H13	NC	--	--	--	Floating
H14	NC	--	--	--	Floating
H15	GND	--	--	--	GND
H16	NC	--	--	--	Floating
H17	NC	--	--	--	Floating
H18	GND	--	--	--	GND
H19	NC	--	--	--	Floating
H20	NC	--	--	--	Floating
H21	GND	--	--	--	GND
H22	F_PHY3_CRS	M14	4	3.3V	MII carrier sense
H23	F_PHY3_COL	L14	4	3.3V	MII collision detection
H24	GND	--	--	--	GND
H25	F_PHY3_TXD1	H26	4	3.3V	MII transmit data
H26	F_PHY3_TXEN	G26	4	3.3V	MII transmit enable
H27	GND	--	--	--	GND

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
H28	NC	--	--	--	Floating
H29	F_PHY3_RXDV	D26	4	3.3V	MII receive data, valid
H30	GND	--	--	--	GND
H31	F_PHY3_RXD1	F23	4	3.3V	MII receive data
H32	F_PHY3_Link	E23	4	3.3V	Connection status indicator
H33	GND	--	--	--	GND
H34	F_A0	K20	4	3.3V	Chip address A0
H35	F_A1	J20	4	3.3V	Chip address A1
H36	GND	--	--	--	GND
H37	F_SCL	J18	4	3.3V	Serial Clock
H38	WP	H18	4	3.3V	Write protection
H39	GND	--	--	--	GND
H40	NC	--	--	--	Floating
J1	GND	--	--	--	GND
J2	NC	--	--	--	Floating
J3	NC	--	--	--	Floating
J4	GND	--	--	--	GND
J5	GND	--	--	--	GND
J6	F_PHY2_RST_n	U14	2	3.3V	On-chip reset
J7	F_PHY2_CRS	V14	2	3.3V	MII carrier sense
J8	GND	--	--	--	GND
J9	F_PHY2_RXD3	V18	2	3.3V	MII receive data
J10	F_PHY2_TXD3	W18	2	3.3V	MII transmit data
J11	GND	--	--	--	GND
J12	F_PHY2_TXD2	U22	2	3.3V	MII transmit data
J13	F_PHY2_TXD1	V22	2	3.3V	MII transmit data
J14	GND	--	--	--	GND
J15	F_PHY2_TXEN	AA24	2	3.3V	MII transmit enable

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
J16	F_PHY2_TXC	AB25	2	3.3V	MII transmit clock
J17	GND	--	--	--	GND
J18	F_PHY2_RXC	W25	2	3.3V	MII receive clock
J19	F_PHY2_RXDV	Y26	2	3.3V	MII receive data, valid
J20	GND	--	--	--	GND
J21	F_PHY2_RXD2	V24	2	3.3V	MII receive data
J22	F_PHY2_LINKACT0	W24	2	3.3V	Connection/active status indicator
J23	GND	--	--	--	GND
J24	NC	--	--	--	Floating
J25	NC	--	--	--	Floating
J26	GND	--	--	--	GND
J27	NC	--	--	--	Floating
J28	NC	--	--	--	Floating
J29	GND	--	--	--	GND
J30	NC	--	--	--	Floating
J31	NC	--	--	--	Floating
J32	GND	--	--	--	GND
J33	NC	--	--	--	Floating
J34	NC	--	--	--	Floating
J35	GND	--	--	--	GND
J36	NC	--	--	--	Floating
J37	NC	--	--	--	Floating
J38	GND	--	--	--	GND
J39	NC	--	--	--	Floating
J40	GND	--	--	--	GND
K1	NC	--	--	--	Floating
K2	GND	--	--	--	GND
K3	GND	--	--	--	GND
K4	NC	--	--	--	Floating

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
K5	NC	--	--	--	Floating
K6	GND	--	--	--	GND
K7	NC	--	--	--	Floating
K8	F_PHY2_Link	T15	2	3.3V	Connection status indicator
K9	GND	--	--	--	GND
K10	F_PHY2_COL	U15	2	3.3V	MII collision detection
K11	NC	--	--	--	Floating
K12	GND	--	--	--	GND
K13	NC	--	--	--	Floating
K14	F_PHY2_TXD0	U20	2	3.3V	MII transmit data
K15	GND	--	--	--	GND
K16	F_PHY2_CLK	Y22	2	3.3V	External clock input
K17	F_PHY3_CLK	Y23	2	3.3V	External clock input
K18	GND	--	--	--	GND
K19	F_PHY2_RXD0	T17	2	3.3V	MII receive data
K20	F_PHY2_RXD1	T18	2	3.3V	MII receive data
K21	GND	--	--	--	GND
K22	NC	--	--	--	Floating
K23	NC	--	--	--	Floating
K24	GND	--	--	--	GND
K25	NC	--	--	--	Floating
K26	NC	--	--	--	Floating
K27	GND	--	--	--	GND
K28	NC	--	--	--	Floating
K29	NC	--	--	--	Floating
K30	GND	--	--	--	GND
K31	NC	--	--	--	Floating

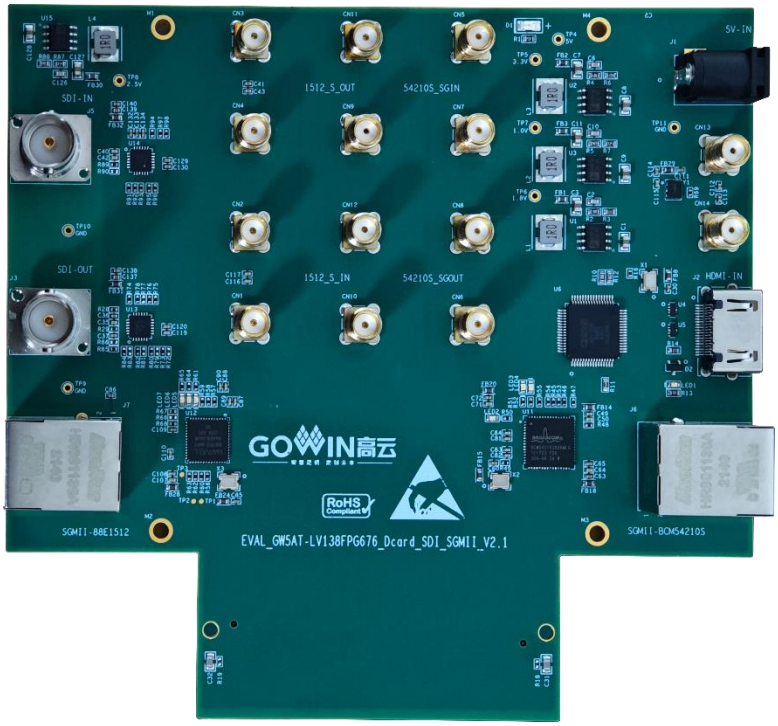
RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
K32	NC	--	--	--	Floating
K33	GND	--	--	--	GND
K34	NC	--	--	--	Floating
K35	NC	--	--	--	Floating
K36	GND	--	--	--	GND
K37	NC	--	--	--	Floating
K38	NC	--	--	--	Floating
K39	GND	--	--	--	GND
K40	NC	--	--	--	Floating

3 SDI Daughter Board

3.1 Introduction

3.1.1 Overview

Figure 3-1 EVAL_GW5AT-LV138FPG676_Dcard_SDI_SGMII_V2.1 Daughter Board



The SDI daughter board needs to be used with the DK_START_GW5AST-LV138FPG676A_V1.0 motherboard, primarily for HDMI communication, SDI communication, and SGMII communication.

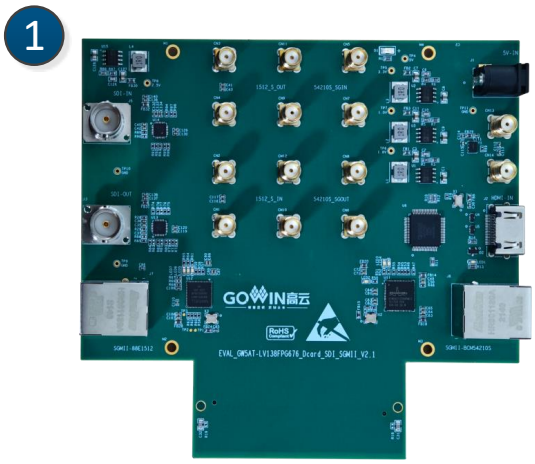
The SDI daughter board supports 3Gbps SDI data transfer.

3.1.2 A Daughter Board Kit

The daughter board kit includes the following item:

- EVAL_GW5AT-LV138FPG676_Dcard_SDI_SGMII_V2.1 daughter board

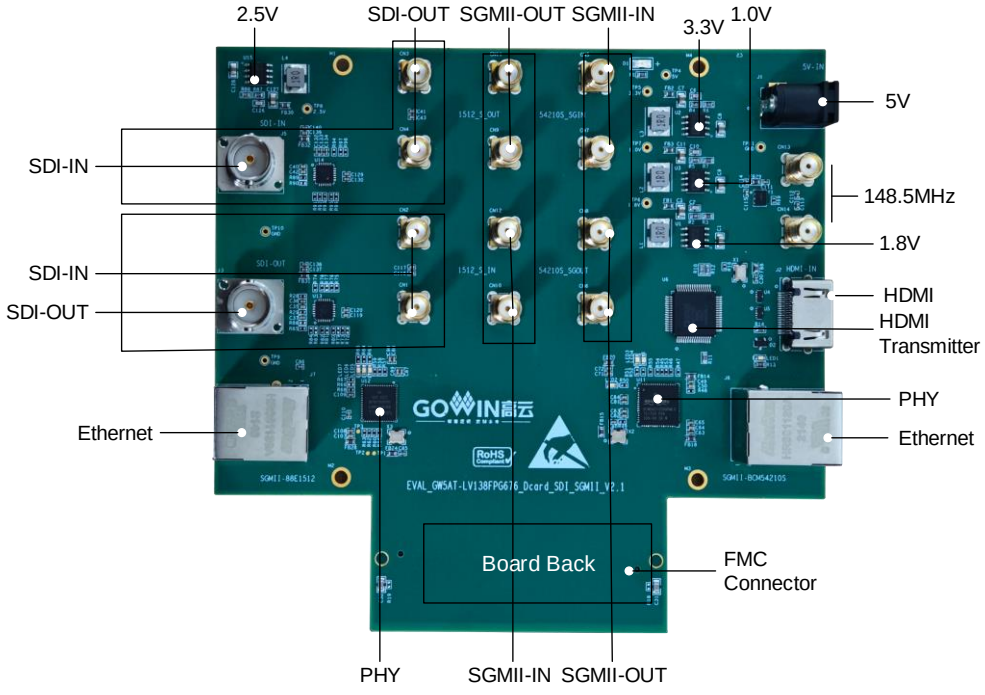
Figure 3-2 A Daughter Board Kit



① EVAL_GW5AT-LV138FPG676_Dcard_SDI_SGMII_V2.1 daughter board

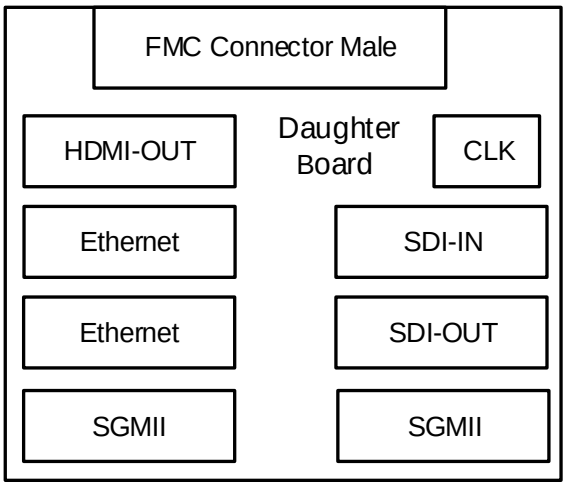
3.1.3 PCB Components

Figure 3-3 PCB Components



3.1.4 System Block Diagram

Figure 3-4 System Block Diagram



3.1.5 Features

The key features are as follows:

1. Power
   - External DC 5V Power
   - The green Power light is on after power on
2. Clock system
   - One 148.5MHz differential clock
3. Ethernet interface
   - Two Ethernet interfaces
   - RJ45 connector integrated with network transformer internally
4. SGMII interface
   - Two SGMII-IN interfaces
   - Two SGMII-OUT interfaces
5. HDMI interface
   - One HDMI-TX interface for HDMI-TX communication via the ADV7513 encoding chip
6. SDI interface
   - One SDI-IN interface
   - One SDI-OUT interface
   - 3G-SDI interface with data rate up to 2.97Gbps
7. Board-to-board connector
   - Use 400Pin FMC connector with 1.27mm pitch
   - Communicate with the DK_START_GW5AST-LV138FPG676A_V1.0 motherboard

3.2 Daughter Board Circuit

3.2.1 Power Supply

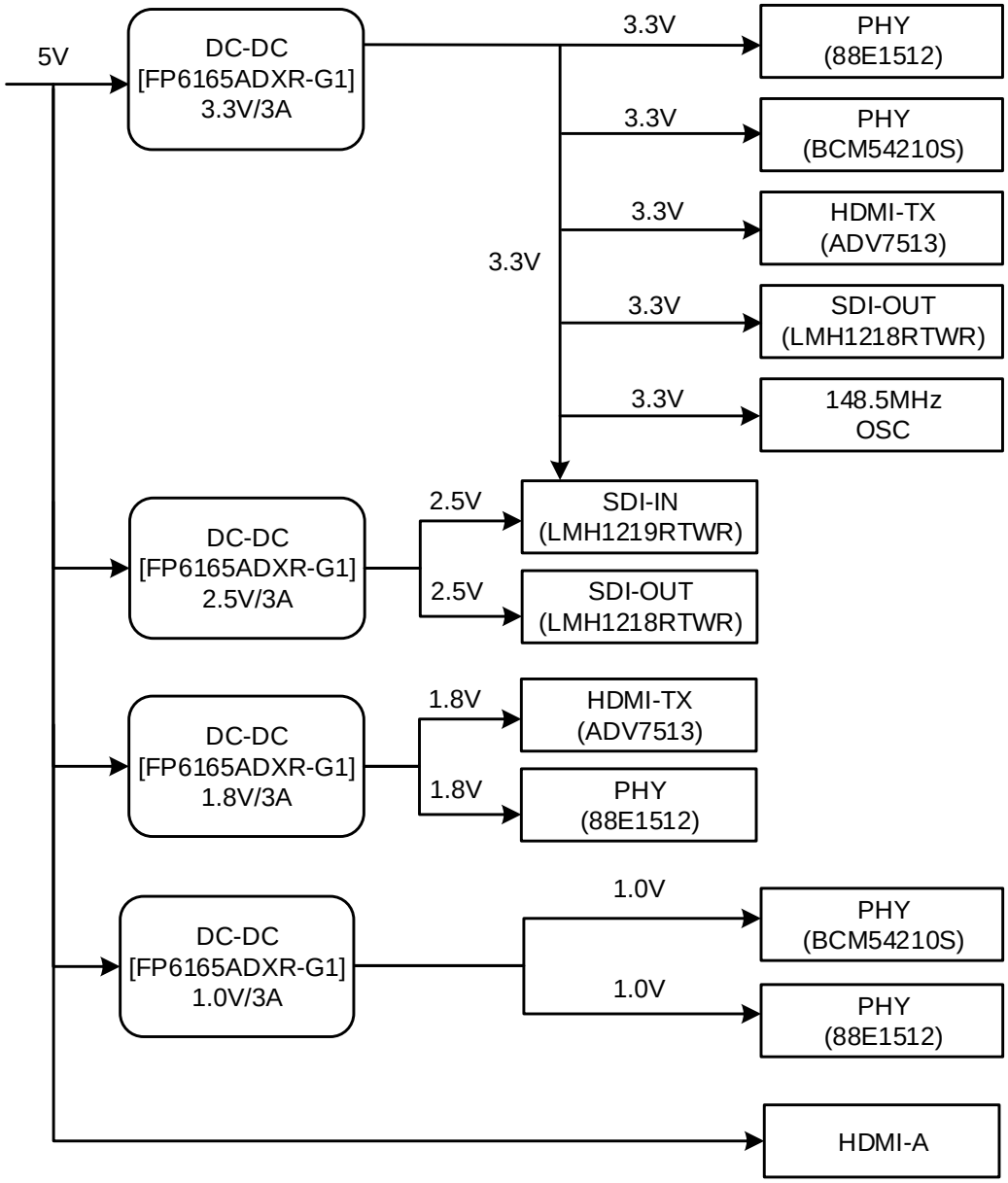
3.2.1.1 Introduction

The SDI daughter board is powered by an external 5V power adapter.

The input 5V power generates a 3.3V, 2.5V, 1.8V, 1.0V power supply through the power chip on the SDI daughter board to meet the power requirements of the SDI daughter board.

3.2.1.2 Power System Distribution

Figure 3-5 Power Supply System Distribution Diagram

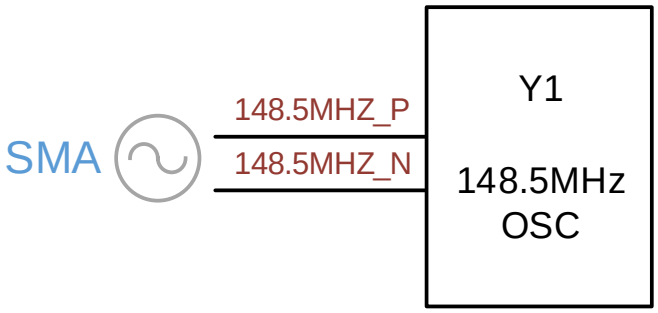


3.2.2 Clock

3.2.2.1 Introduction

The SDI daughter board provides one 148.5MHz differential clock. The clock signal is let out through two SMA females.

Figure 3-6 Clock Connection Diagram



3.2.2.2 Pin Distribution

Table 3-1 Clock Pin Distribution

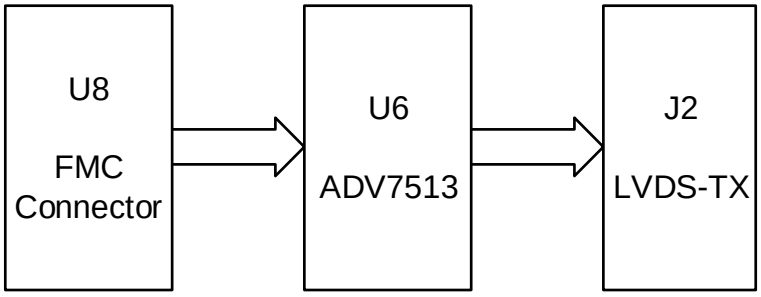
Device Number	Signal Name	Description
CN13	148.5MHZ_P	P-side of 148.5M differential clock
CN14	148.5MHZ_N	N-side of 148.5M differential clock

3.2.3 HDMI Interface

3.2.3.1 Introduction

The SDI daughter board provides one HDMI output Interface. HDMI-TX communication is implemented via the ADV7513 encoding chip. The connection diagram is as follows.

Figure 3-7 Connection Diagram of HDMI-TX Interface



3.2.3.2 Pin Distribution

Table 3-2 J2 Pin Distribution for HDMI-TX Interface

J2 Pin No.	Signal Name	I/O Level	Description
1	HDMI_TXA2P	3.3V	HDMI differential data
2	GND	--	GND
3	HDMI_TXA2N	3.3V	HDMI differential data
4	HDMI_TXA1P	3.3V	HDMI differential data
5	GND	--	GND
6	HDMI_TXA1N	3.3V	HDMI differential data
7	HDMI_TXA0P	3.3V	HDMI differential data
8	GND	--	GND
9	HDMI_TXA0N	3.3V	HDMI differential data
10	HDMI_TXACP	3.3V	HDMI differential clock
11	GND	--	GND
12	HDMI_TXACN	3.3V	HDMI differential clock
13	HDMI_CEC	3.3V	CEC control signal
14	NC	--	Floating
15	HDMI_DDC_SCL	5V	I2C serial clock
16	HDMI_DDC_SDA	5V	I2C serial data
17	GND	--	GND
18	HDMI_5V	5V	Power
19	HDMI_HPD	5V	Hot Plug Detect
20	GND	--	GND
21	GND	--	GND
22	GND	--	GND
23	GND	--	GND

3.2.4 SDI Interface

3.2.4.1 Introduction

The SDI daughter board provides one SDI input interface and one SDI output interface. The SDI-IN interface receives serial data from one BNC female and sends the processed serial data via two SMA females; the SDI-OUT interface receives serial data from two SMA females and

sends the processed serial data via one BNC female. The connection diagram of SDI interface is as follows.

Figure 3-8 Connection Diagram of SDI-IN Interface

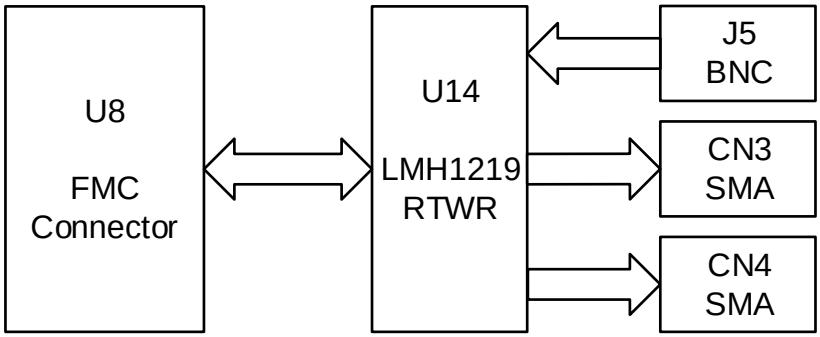
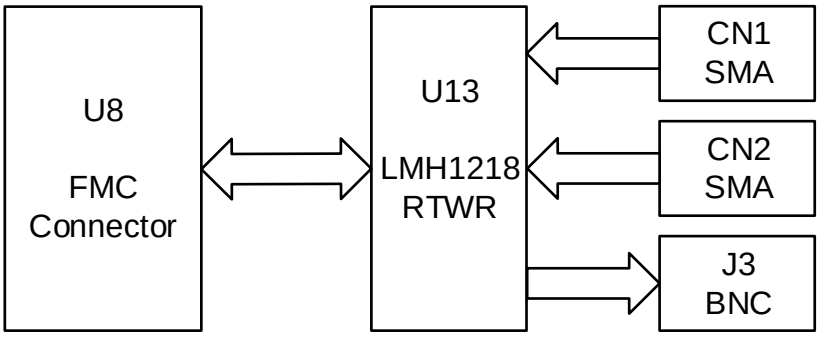


Figure 3-9 Connection Diagram of SDI-OUT Interface



3.2.4.2 Pin Distribution

Table 3-3 SDI-IN Interface Pin Distribution

Device Number	Signal Name	I/O Level	Description
CN3	SDO+	2.5V	SDO+
CN4	SDO-	2.5V	SDO-
J5	SDI+	2.5V	SDI+

Table 3-4 SDI-OUT Interface Pin Distribution

Device Number	Signal Name	I/O Level	Description
CN1	1218_SDI+	2.5V	SDI+
CN2	1218_SDI-	2.5V	SDI-
J3	1218_SDO+	2.5V	SDO+

3.2.5 Ethernet

3.2.5.1 Introduction

The SDI daughter board provides two Ethernet interfaces, supporting 10BASE-T/100BASE-TX/1000BASE-T modes. Use the RJ45 connector integrated with network transformer internally. The connection diagram is as follows.

Figure 3-10 Connection Diagram of Ethernet 1 Interface

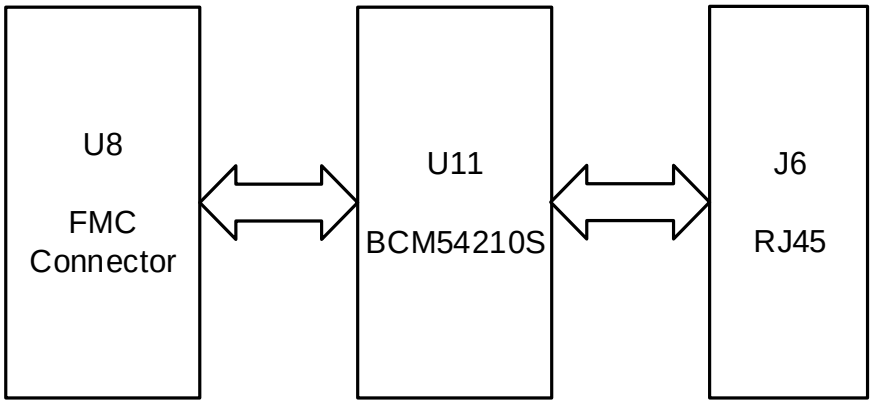
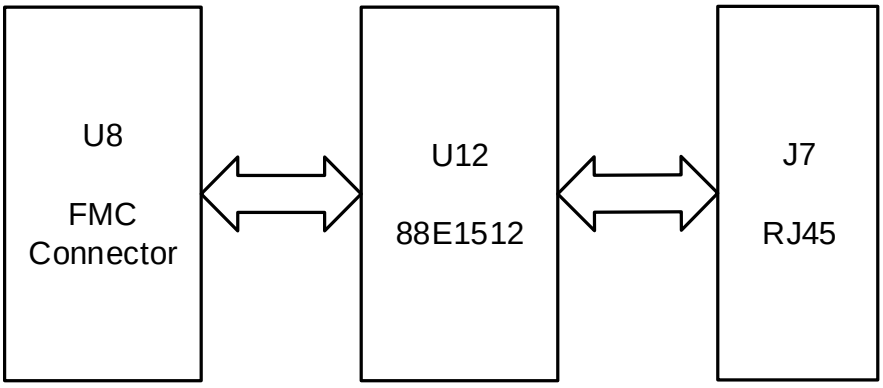


Figure 3-11 Connection Diagram of Ethernet 2 Interface



3.2.5.2 Pin Distribution

Table 3-5 J6 Pin Distribution of Ethernet 1 Interface

J6 Pin No.	Signal Name	Description
1	GND	GND
2	PHY1_TRD0+	Differential data channel 0+
3	PHY1_TRD0-	Differential data channel 0-
4	PHY1_TRD1+	Differential data channel 1+
5	PHY1_TRD2+	Differential data channel 2+
6	PHY1_TRD2-	Differential data channel 2-
7	PHY1_TRD1-	Differential data channel 1-
8	PHY1_TRD3+	Differential data channel 3+
9	PHY1_TRD3-	Differential data channel 3-
10	GND	GND

Table 3-6 J7 Pin Distribution of Ethernet 2 Interface

J7 Pin No.	Signal Name	Description
1	GND	GND
2	1512_MDIP0	Media interface 0
3	1512_MDIN0	Media interface 0
4	1512_MDIP1	Media interface 1
5	1512_MDIP2	Media interface 2
6	1512_MDIN2	Media interface 2
7	1512_MDIN1	Media interface 1
8	1512_MDIP3	Media interface 3
9	1512_MDIN3	Media interface 3
10	GND	GND

3.2.6 SGMII Interface

3.2.6.1 Introduction

The SDI daughter board provides two SGMII input interfaces and two SGMII output interfaces. SGMII signals are transmitted by connecting the SerDes interface (SMA female) on the motherboard through the SMA female on the daughter board. The connection diagram is as follows.

Figure 3-12 Connection Diagram of SGMII 1

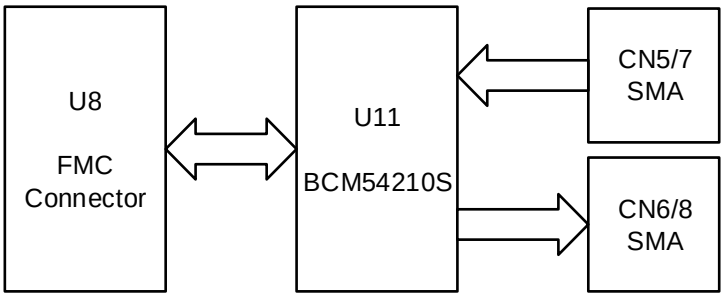
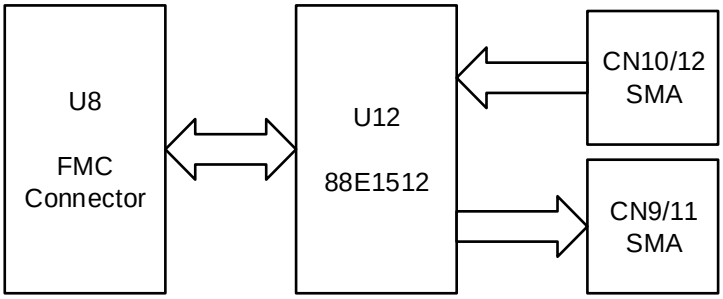


Figure 3-13 Connection Diagram of SGMII 2



3.2.6.2 Pin Distribution

Table 3-7 SGMII 1 Interface Pin Distribution

Pin No.	Signal Name	Description
CN5	54210S_SGIN+	SGMII data input
CN7	54210S_SGIN-	SGMII data input
CN6	54210S_SGOUT+	SGMII data output
CN8	54210S_SGOUT-	SGMII data output

Table 3-8 SGMII 2 Interface Pin Distribution

Pin No.	Signal Name	Description
CN10	1512_S_INP	SGMII receive data
CN12	1512_S_INN	SGMII receive data
CN9	1512_S_OUTP	SGMII transmit data
CN11	1512_S_OUT	SGMII transmit data

3.2.7 Board-to-board connector

3.2.7.1 Introduction

The SDI daughter board has a 400Pin FMC connector with 1.27mm pitch for communication with the DK_START_GW5AST-LV138FPG676A_V1.0 motherboard.

3.2.7.2 Pin Distribution

Table 3-9 Pin Distribution for U8 Board-to-Board Connector

U8 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
A1	GND	--	--	--	GND
A2	NC	--	--	--	Floating
A3	NC	--	--	--	Floating
A4	GND	--	--	--	GND
A5	GND	--	--	--	GND
A6	NC	--	--	--	Floating
A7	NC	--	--	--	Floating
A8	GND	--	--	--	GND
A9	GND	--	--	--	GND
A10	NC	--	--	--	Floating
A11	NC	--	--	--	Floating
A12	GND	--	--	--	GND
A13	GND	--	--	--	GND
A14	NC	--	--	--	Floating
A15	NC	--	--	--	Floating
A16	GND	--	--	--	GND
A17	GND	--	--	--	GND
A18	NC	--	--	--	Floating
A19	NC	--	--	--	Floating
A20	GND	--	--	--	GND
A21	GND	--	--	--	GND
A22	NC	--	--	--	Floating
A23	NC	--	--	--	Floating
A24	GND	--	--	--	GND
A25	GND	--	--	--	GND
A26	NC	--	--	--	Floating
A27	NC	--	--	--	Floating
A28	GND	--	--	--	GND

U8 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
A29	GND	--	--	--	GND
A30	NC	--	--	--	Floating
A31	NC	--	--	--	Floating
A32	GND	--	--	--	GND
A33	GND	--	--	--	GND
A34	NC	--	--	--	Floating
A35	NC	--	--	--	Floating
A36	GND	--	--	--	GND
A37	GND	--	--	--	GND
A38	NC	--	--	--	Floating
A39	NC	--	--	--	Floating
A40	GND	--	--	--	GND
B1	NC	--	--	--	Floating
B2	GND	--	--	--	GND
B3	GND	--	--	--	GND
B4	NC	--	--	--	Floating
B5	NC	--	--	--	Floating
B6	GND	--	--	--	GND
B7	GND	--	--	--	GND
B8	NC	--	--	--	Floating
B9	NC	--	--	--	Floating
B10	GND	--	--	--	GND
B11	GND	--	--	--	GND
B12	NC	--	--	--	Floating
B13	NC	--	--	--	Floating
B14	GND	--	--	--	GND
B15	GND	--	--	--	GND
B16	NC	--	--	--	Floating
B17	NC	--	--	--	Floating
B18	GND	--	--	--	GND

U8 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
B19	GND	--	--	--	GND
B20	NC	--	--	--	Floating
B21	NC	--	--	--	Floating
B22	GND	--	--	--	GND
B23	GND	--	--	--	GND
B24	NC	--	--	--	Floating
B25	NC	--	--	--	Floating
B26	GND	--	--	--	GND
B27	GND	--	--	--	GND
B28	NC	--	--	--	Floating
B29	NC	--	--	--	Floating
B30	GND	--	--	--	GND
B31	GND	--	--	--	GND
B32	NC	--	--	--	Floating
B33	NC	--	--	--	Floating
B34	GND	--	--	--	GND
B35	GND	--	--	--	GND
B36	NC	--	--	--	Floating
B37	NC	--	--	--	Floating
B38	GND	--	--	--	GND
B39	GND	--	--	--	GND
B40	NC	--	--	--	Floating
C1	GND	--	--	--	GND
C2	NC	--	--	--	Floating
C3	NC	--	--	--	Floating
C4	GND	--	--	--	GND
C5	GND	--	--	--	GND
C6	NC	--	--	--	Floating
C7	NC	--	--	--	Floating
C8	GND	--	--	--	GND

U8 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
C9	GND	--	--	--	GND
C10	NC	--	--	--	Floating
C11	7513_D8	F19	5	3.3V	RGB data signal
C12	GND	--	--	--	GND
C13	GND	--	--	--	GND
C14	NC	--	--	--	Floating
C15	NC	--	--	--	Floating
C16	GND	--	--	--	GND
C17	GND	--	--	--	GND
C18	NC	--	--	--	Floating
C19	NC	--	--	--	Floating
C20	GND	--	--	--	GND
C21	GND	--	--	--	GND
C22	1512_MDC	G20	4	2.5V	Management data clock
C23	1512_MDIO	G21	4	2.5V	Management data
C24	GND	--	--	--	GND
C25	GND	--	--	--	GND
C26	1512_RESETn	G25	4	2.5V	Hardware reset
C27	NC	--	--	--	Floating
C28	GND	--	--	--	GND
C29	GND	--	--	--	GND
C30	NC	--	--	--	Floating
C31	NC	--	--	--	Floating
C32	GND	--	--	--	GND
C33	GND	--	--	--	GND
C34	GND	--	--	--	GND
C35	NC	--	--	--	Floating
C36	GND	--	--	--	GND
C37	NC	--	--	--	Floating

U8 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
C38	GND	--	--	--	GND
C39	NC	--	--	--	Floating
C40	GND	--	--	--	GND
D1	NC	--	--	--	Floating
D2	GND	--	--	--	GND
D3	GND	--	--	--	GND
D4	NC	--	--	--	Floating
D5	NC	--	--	--	Floating
D6	GND	--	--	--	GND
D7	GND	--	--	--	GND
D8	7513_INT	E17	5	3.3V	Interrupt signal
D9	7513_DE	E18	5	3.3V	Data enable signal
D10	GND	--	--	--	GND
D11	7513_D6	G19	5	3.3V	RGB data signal
D12	NC	--	--	--	Floating
D13	GND	--	--	--	GND
D14	NC	--	--	--	Floating
D15	NC	--	--	--	Floating
D16	GND	--	--	--	GND
D17	NC	--	--	--	Floating
D18	NC	--	--	--	Floating
D19	GND	--	--	--	GND
D20	1512_RX_CLK	K21	4	2.5V	Receive clock
D21	1512_CLK125	J21	4	2.5V	125MHz clock output
D22	GND	--	--	--	GND
D23	1219_SCL	K22	4	2.5V	Serial clock line
D24	1219_SEL	K23	4	2.5V	Mode Selection
D25	GND	--	--	--	GND
D26	1219_AD0	L17	4	2.5V	Address signal AD0
D27	1219_VOD_DE	L18	4	2.5V	High-speed signal

U8 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
					pre-emphasis
D28	GND	--	--	--	GND
D29	NC	--	--	--	Floating
D30	NC	--	--	--	Floating
D31	NC	--	--	--	Floating
D32	NC	--	--	--	Floating
D33	NC	--	--	--	Floating
D34	NC	--	--	--	Floating
D35	GND	--	--	--	GND
D36	NC	--	--	--	Floating
D37	GND	--	--	--	GND
D38	NC	--	--	--	Floating
D39	GND	--	--	--	GND
D40	NC	--	--	--	Floating
E1	GND	--	--	--	GND
E2	NC	--	--	--	Floating
E3	NC	--	--	--	Floating
E4	GND	--	--	--	GND
E5	GND	--	--	--	GND
E6	7513_SCL	V23	2	3.3V	I2C serial interface clock
E7	7513_SDA	W23	2	3.3V	I2C serial interface data
E8	GND	--	--	--	GND
E9	7513_D0	V19	2	3.3V	RGB data signal
E10	7513_D5	W19	2	3.3V	RGB data signal
E11	GND	--	--	--	GND
E12	NC	--	--	--	Floating
E13	NC	--	--	--	Floating
E14	GND	--	--	--	GND
E15	NC	--	--	--	Floating

U8 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
E16	NC	--	--	--	Floating
E17	GND	--	--	--	GND
E18	NC	--	--	--	Floating
E19	NC	--	--	--	Floating
E20	GND	--	--	--	GND
E21	NC	--	--	--	Floating
E22	NC	--	--	--	Floating
E23	GND	--	--	--	GND
E24	NC	--	--	--	Floating
E25	NC	--	--	--	Floating
E26	GND	--	--	--	GND
E27	NC	--	--	--	Floating
E28	NC	--	--	--	Floating
E29	GND	--	--	--	GND
E30	NC	--	--	--	Floating
E31	NC	--	--	--	Floating
E32	GND	--	--	--	GND
E33	NC	--	--	--	Floating
E34	NC	--	--	--	Floating
E35	GND	--	--	--	GND
E36	NC	--	--	--	Floating
E37	NC	--	--	--	Floating
E38	GND	--	--	--	GND
E39	NC	--	--	--	Floating
E40	GND	--	--	--	GND
F1	NC	--	--	--	Floating
F2	GND	--	--	--	GND
F3	GND	--	--	--	GND
F4	54210S_RXC	U21	2	3.3V	RGMII receive clock
F5	54210S_GTXCLK	V21	2	3.3V	RGMII transmit clock

U8 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F6	GND	--	--	--	GND
F7	54210S_RXD3	V16	2	3.3V	RGMII/MII receive data
F8	54210S_DV	V17	2	3.3V	RGMII receive data, valid
F9	GND	--	--	--	GND
F10	54210S_RXD2	W20	2	3.3V	RGMII/MII receive data
F11	54210S_RXD1	Y20	2	3.3V	RGMII/MII receive data
F12	GND	--	--	--	GND
F13	54210S_RXD0	AB24	2	3.3V	RGMII/MII receive data
F14	54210S_TX_EN	AC24	2	3.3V	RGMII transmit enable
F15	GND	--	--	--	GND
F16	54210S_TXD3	AB26	2	3.3V	RGMII transmit data
F17	54210S_TXD2	AC26	2	3.3V	RGMII transmit data
F18	GND	--	--	--	GND
F19	54210S_TXD1	U25	2	3.3V	RGMII transmit data
F20	54210S_TXD0	U26	2	3.3V	RGMII transmit data
F21	GND	--	--	--	GND
F22	NC	--	--	--	Floating
F23	NC	--	--	--	Floating
F24	GND	--	--	--	GND
F25	NC	--	--	--	Floating
F26	NC	--	--	--	Floating
F27	GND	--	--	--	GND
F28	NC	--	--	--	Floating
F29	NC	--	--	--	Floating
F30	GND	--	--	--	GND
F31	NC	--	--	--	Floating

U8 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F32	NC	--	--	--	Floating
F33	GND	--	--	--	GND
F34	NC	--	--	--	Floating
F35	NC	--	--	--	Floating
F36	GND	--	--	--	GND
F37	NC	--	--	--	Floating
F38	NC	--	--	--	Floating
F39	GND	--	--	--	GND
F40	NC	--	--	--	Floating
G1	GND	--	--	--	GND
G2	NC	--	--	--	Floating
G3	NC	--	--	--	Floating
G4	GND	--	--	--	GND
G5	GND	--	--	--	GND
G6	7513_MCLK	D18	5	3.3V	IIS interface MCLK
G7	7513_IIS0	C18	5	3.3V	IIS interface data signal
G8	GND	--	--	--	GND
G9	7513_D1	E21	5	3.3V	RGB data signal
G10	7513_D3	D21	5	3.3V	RGB data signal
G11	GND	--	--	--	GND
G12	7513_D12	A17	5	3.3V	RGB data signal
G13	7513_D14	A18	5	3.3V	RGB data signal
G14	GND	--	--	--	GND
G15	7513_CLK	E16	5	3.3V	Video output clock
G16	7513_D19	D16	5	3.3V	RGB data signal
G17	GND	--	--	--	GND
G18	7513_D22	G15	5	3.3V	RGB data signal
G19	7513_D23	F15	5	3.3V	RGB data signal
G20	GND	--	--	--	GND

U8 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
G21	1512_TX_CTRL	M16	4	2.5V	RGMII transmit control
G22	1512_TXD3	M17	4	2.5V	RGMII transmit data
G23	GND	--	--	--	GND
G24	1512_TXD2	J24	4	2.5V	RGMII transmit data
G25	1512_TX_CLK	H24	4	2.5V	RGMII transmit clock
G26	GND	--	--	--	GND
G27	1512_TXD1	G24	4	2.5V	RGMII transmit data
G28	1512_TXD0	F24	4	2.5V	RGMII transmit data
G29	GND	--	--	--	GND
G30	1512_RXD3	E25	4	2.5V	RGMII receive data
G31	1218_AD1	D25	4	2.5V	Address signal AD1
G32	GND	--	--	--	GND
G33	1512_RXD2	G22	4	2.5V	RGMII receive data
G34	1512_RXD1	F22	4	2.5V	RGMII receive data
G35	GND	--	--	--	GND
G36	1512_RXD0	J19	4	2.5V	RGMII receive data
G37	1512_RX_CTRL	H19	4	2.5V	RGMII receive control
G38	GND	--	--	--	GND
G39	NC	--	--	--	Floating
G40	GND	--	--	--	GND
H1	NC	--	--	--	Floating
H2	NC	--	--	--	Floating
H3	GND	--	--	--	GND
H4	NC	--	--	--	Floating
H5	NC	--	--	--	Floating
H6	GND	--	--	--	GND
H7	7513_VSYNC	B22	5	3.3V	Vertical synchronization signal
H8	7513_HSYNC	A22	5	3.3V	Horizontal

U8 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
					synchronization signal
H9	GND	--	--	--	GND
H10	7513_D7	B20	5	3.3V	RGB data signal
H11	7513_D9	A20	5	3.3V	RGB data signal
H12	GND	--	--	--	GND
H13	7513_D11	H14	5	3.3V	RGB data signal
H14	7513_D13	H15	5	3.3V	RGB data signal
H15	GND	--	--	--	GND
H16	7513_D17	G17	5	3.3V	RGB data signal
H17	7513_D20	F17	5	3.3V	RGB data signal
H18	GND	--	--	--	GND
H19	NC	--	--	--	Floating
H20	NC	--	--	--	Floating
H21	GND	--	--	--	GND
H22	1219_CTRL	M14	4	2.5V	Output control
H23	1219_AD1	L14	4	2.5V	Address signal AD1
H24	GND	--	--	--	GND
H25	1219_SDA	--	--	--	Serial data signal
H26	1219_LOCK_N	G26	4	2.5V	Lock indicator
H27	GND	--	--	--	GND
H28	1219_IO_SEL	E26	4	2.5V	Input/Output control
H29	1218_LOCK	D26	4	2.5V	Lock indicator
H30	GND	--	--	--	GND
H31	1218_LOS_INT_N	F23	4	2.5V	Signal loss alert
H32	1218_EN	E23	4	2.5V	Enable signal
H33	GND	--	--	--	GND
H34	1218_SDA	K20	4	2.5V	Serial data signal
H35	1218_SCL	J20	4	2.5V	Serial clock signal
H36	GND	--	--	--	GND

U8 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
H37	1218_AD0	J18	4	2.5V	Address signal AD0
H38	1218_SEL	H18	4	2.5V	Mode Selection
H39	GND	--	--	--	GND
H40	NC	--	--	--	Floating
J1	GND	--	--	--	GND
J2	NC	--	--	--	Floating
J3	NC	--	--	--	Floating
J4	GND	--	--	--	GND
J5	GND	--	--	--	GND
J6	7513_LRCLK	U14	2	3.3V	IIS interface LRCLK
J7	7513_SCLK	V14	2	3.3V	IIS interface SCLK
J8	GND	--	--	--	GND
J9	7513_D2	V18	2	3.3V	RGB data signal
J10	7513_D4	W18	2	3.3V	RGB data signal
J11	GND	--	--	--	GND
J12	NC	--	--	--	Floating
J13	7513_D10	V22	2	3.3V	RGB data signal
J14	GND	--	--	--	GND
J15	7513_D15	AA24	2	3.3V	RGB data signal
J16	7513_D18	AB25	2	3.3V	RGB data signal
J17	GND	--	--	--	GND
J18	7513_D16	W25	2	3.3V	RGB data signal
J19	7513_D21	Y26	2	3.3V	RGB data signal
J20	GND	--	--	--	GND
J21	NC	--	--	--	Floating
J22	NC	--	--	--	Floating
J23	GND	--	--	--	GND
J24	NC	--	--	--	Floating
J25	NC	--	--	--	Floating
J26	GND	--	--	--	GND

U8 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
J27	NC	--	--	--	Floating
J28	NC	--	--	--	Floating
J29	GND	--	--	--	GND
J30	NC	--	--	--	Floating
J31	NC	--	--	--	Floating
J32	GND	--	--	--	GND
J33	NC	--	--	--	Floating
J34	NC	--	--	--	Floating
J35	GND	--	--	--	GND
J36	NC	--	--	--	Floating
J37	NC	--	--	--	Floating
J38	GND	--	--	--	GND
J39	NC	--	--	--	Floating
J40	GND	--	--	--	GND
K1	NC	--	--	--	Floating
K2	GND	--	--	--	GND
K3	GND	--	--	--	GND
K4	NC	--	--	--	Floating
K5	NC	--	--	--	Floating
K6	GND	--	--	--	GND
K7	54210S_LED1	T14	2	3.3V	Programmable LED
K8	54210S_LED2	T15	2	3.3V	Programmable LED
K9	GND	--	--	--	GND
K10	54210S_MDC	U15	2	3.3V	Management data clock
K11	54210S_MDIO	U16	2	3.3V	Management data I/O
K12	GND	--	--	--	GND
K13	54210S_LED3	T20	2	3.3V	Programmable LED
K14	54210S_RESET	U20	2	3.3V	Reset
K15	GND	--	--	--	GND

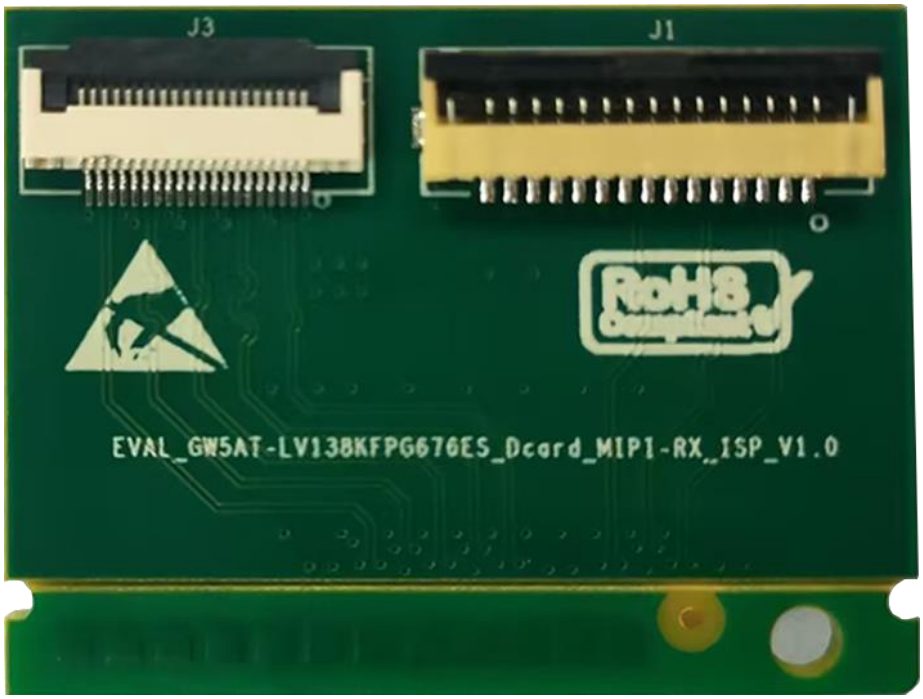
U8 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
K16	54210S_LOCK_RCLK	Y22	2	3.3V	Restore clock
K17	54210S_REC_CLK	Y23	2	3.3V	Main PLL reference clock lock
K18	GND	--	--	--	GND
K19	NC	--	--	--	Floating
K20	NC	--	--	--	Floating
K21	GND	--	--	--	GND
K22	NC	--	--	--	Floating
K23	NC	--	--	--	Floating
K24	GND	--	--	--	GND
K25	NC	--	--	--	Floating
K26	NC	--	--	--	Floating
K27	GND	--	--	--	GND
K28	NC	--	--	--	Floating
K29	NC	--	--	--	Floating
K30	GND	--	--	--	GND
K31	NC	--	--	--	Floating
K32	NC	--	--	--	Floating
K33	GND	--	--	--	GND
K34	NC	--	--	--	Floating
K35	NC	--	--	--	Floating
K36	GND	--	--	--	GND
K37	NC	--	--	--	Floating
K38	NC	--	--	--	Floating
K39	GND	--	--	--	GND
K40	NC	--	--	--	Floating

4 ISP Daughter Board

4.1 Introduction

4.1.1 Overview

Figure 4-1 EVAL_GW5AT-LV138KFPG676ES_Dcard_MIPI-RX_ISP_V1.0 Daughter Board



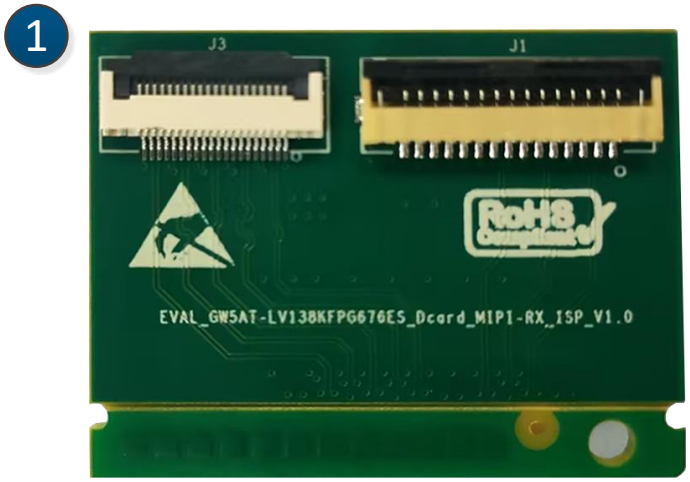
The ISP daughter board needs to be used with the DK_START_GW5AST-LV138FPG676A_V1.0 motherboard, primarily for MIPI-RX communication and ISP evaluation.

4.1.2 A Daughter Board Kit

The daughter board kit includes the following item:

- EVAL_GW5AT-LV138KFPG676ES_Dcard_MIPI-RX_ISP_V1.0 daughter board

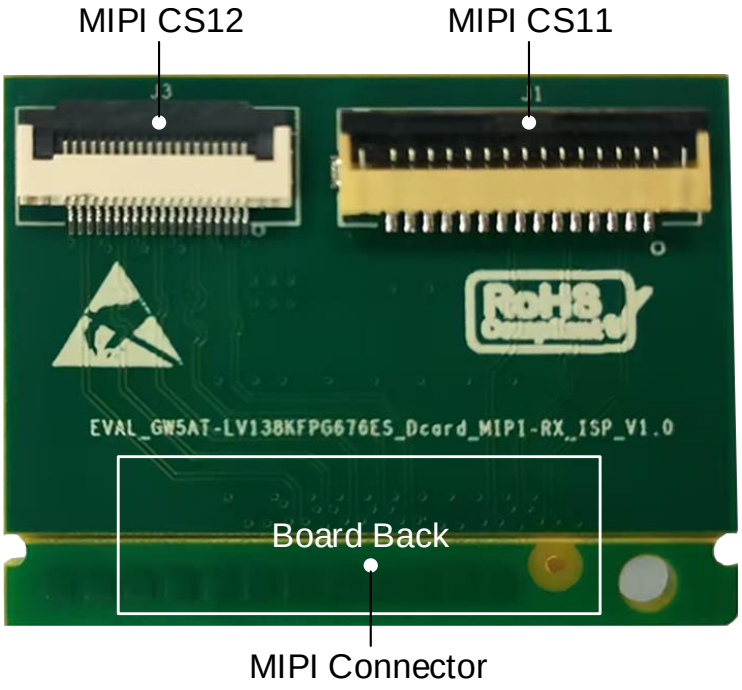
Figure 4-2 A Daughter Board Kit



① EVAL_GW5AT-LV138KFPG676ES_Dcard_MIPI-RX_ISP_V1.0 Daughter Board

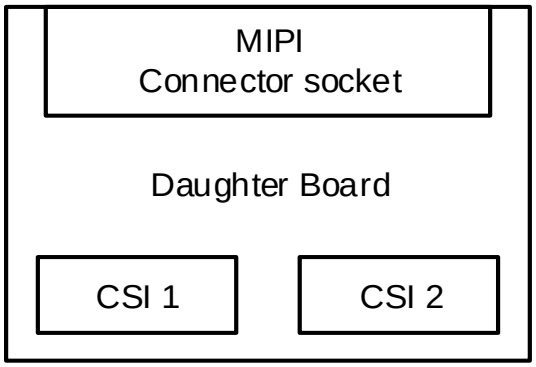
4.1.3 PCB Components

Figure 4-3 PCB Components



4.1.4 System Block Diagram

Figure 4-4 System Block Diagram



4.1.5 Features

The key features are as follows:

1. Power
   - The motherboard provides DC 3.3V power
2. MIPI CSI interface
   - Two MIPI CSI interfaces
   - CSI1 includes 2data+1clk and IIC, CLK, RST; CSI2 includes 4data+1clk
3. Board-to-board connector
   - Use 80Pin board-to-board connector with 0.5mm pitch
   - Communicate with the DK_START_GW5AST-LV138FPG676A_V1.0 motherboard

4.2 Daughter Board Circuit

4.2.1 Power Supply

The motherboard provides DC 3.3V power to the ISP daughter board through board-to-board connectors to meet the power requirements of the ISP daughter board.

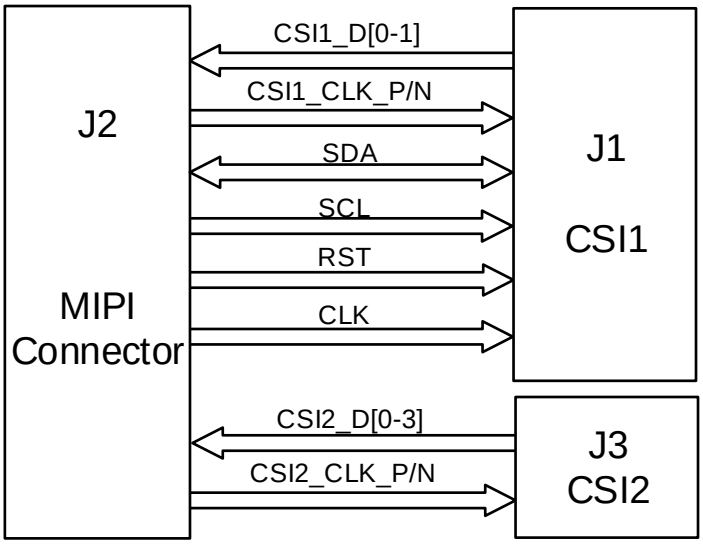
4.2.2 MIPI CSI Interface

4.2.2.1 Introduction

The ISP daughter board provides two MIPI CSI interfaces. MIPI CSI1 interface uses 15Pin FFC/FPC connectors with 1mm pitch, including 3 pairs of differential signals and 4 GPIOs, 2data+1clk, IIC, RST, CLK signals, respectively; MIPI CSI2 interface uses 20Pin FFC/FPC connectors

with 0.5mm pitch, including 5 pairs of differential signals, 4data+1clk, respectively. The connection diagram is as follows.

Figure 4-5 Connection Diagram of MIPI CSI Interface



4.2.2.2 Pin Distribution

Table 4-1 J1 Pin Distribution for MIPI CSI1 Interface

J1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	GND	--	--	--	GND
2	CSI1_D0_N	W1	MIPI	--	N-side of CSI1_D0 interface
3	CSI1_D0_P	V1	MIPI	--	P-side of CSI1_D0 interface
4	GND	--	--	--	GND
5	CSI1_D1_N	AA2	MIPI	--	N-side of CSI1_D1 interface
6	CSI1_D1_P	Y2	MIPI	--	P-side of CSI1_D1 interface
7	GND	--	--	--	GND
8	CSI1_CLK_N	AA3	MIPI	--	N-side of CSI1_CLK interface
9	CSI1_CLK_P	Y3	MIPI	--	P-side of CSI1_CLK interface
10	GND	--	--	--	GND
11	CSI1_RESET	U17	2	3.3V	Reset signal
12	CSI1_CLK	J26	4	3.3V	Clock signal
13	CSI1_SCL	J25	4	3.3V	IIC interface clock signal
14	CSI1_SDA	K16	4	3.3V	IIC interface data signal

J1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
15	AlwaysOn_3.3V	--	--	3.3V	Power

Table 4-2 J3 Pin Distribution for MIPI CSI2 Interface

J3 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	GND	--	--	--	GND
2	CSI2_D0_N	AC1	MIPI	--	N-side of CSI2_D0 interface
3	CSI2_D0_P	AB1	MIPI	--	P-side of CSI2_D0 interface
4	GND	--	--	--	GND
5	GND	--	--	--	GND
6	CSI2_D1_N	AE1	MIPI	--	N-side of CSI2_D1 interface
7	CSI2_D1_P	AD1	MIPI	--	P-side of CSI2_D1 interface
8	GND	--	--	--	GND
9	GND	--	--	--	GND
10	CSI2_CLK_N	AF2	MIPI	--	N-side of CSI2_ CLK interface
11	CSI2_CLK_P	AE2	MIPI	--	P-side of CSI2_ CLK interface
12	GND	--	--	--	GND
13	GND	--	--	--	GND
14	CSI2_D2_N	AF3	MIPI	--	N-side of CSI2_D2 interface
15	CSI2_D2_P	AE3	MIPI	--	P-side of CSI2_D2 interface
16	GND	--	--	--	GND
17	GND	--	--	--	GND
18	CSI2_D3_N	AF5	MIPI	--	N-side of CSI2_D3 interface
19	CSI2_D3_P	AE5	MIPI	--	P-side of CSI2_D3 interface
20	GND	--	--	--	GND
21	NC	--	--	--	Floating
22	NC	--	--	--	Floating

4.2.3 Board-to-board Connector

4.2.3.1 Introduction

The ISP daughter board has a board-to-board connector for communication with the DK_START_GW5AST-LV138FPG676A_V1.0 motherboard. The selected model of 80Pin board-to-board connector with 0.5mm pitch is AXK680337YG.

4.2.3.2 Pin Distribution

Table 4-3 Pin Distribution for J2 Board-to-Board Connector

J2 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	CSI1_D0_N	W1	MIPI	--	N-side of CSI1_D0 interface
2	NC	--	--	--	Floating
3	CSI1_D0_P	V1	MIPI	--	P-side of CSI1_D0 interface
4	NC	--	--	--	Floating
5	GND	--	--	--	GND
6	NC	--	--	--	Floating
7	CSI1_D1_N	AA2	MIPI	--	N-side of CSI1_D1 interface
8	NC	--	--	--	Floating
9	CSI1_D1_P	Y2	MIPI	--	P-side of CSI1_D1 interface
10	GND	--	--	--	GND
11	GND	--	--	--	GND
12	NC	--	--	--	Floating
13	CSI1_CLK_N	AA3	MIPI	--	N-side of CSI1_ CLK interface
14	NC	--	--	--	Floating
15	CSI1_CLK_P	Y3	MIPI	--	P-side of CSI1_ CLK interface
16	NC	--	--	--	Floating
17	GND	--	--	--	GND
18	NC	--	--	--	Floating

J2 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
19	NC	--	--	--	Floating
20	GND	--	--	--	GND
21	NC	--	--	--	Floating
22	NC	--	--	--	Floating
23	GND	--	--	--	GND
24	NC	--	--	--	Floating
25	NC	--	--	--	Floating
26	NC	--	--	--	Floating
27	NC	--	--	--	Floating
28	NC	--	--	--	Floating
29	GND	--	--	--	GND
30	GND	--	--	--	GND
31	CSI2_D0_N	AC1	MIPI	--	N-side of CSI2_D0 interface
32	NC	--	--	--	Floating
33	CSI2_D0_P	AB1	MIPI	--	P-side of CSI2_D0 interface
34	NC	--	--	--	Floating
35	GND	--	--	--	GND
36	NC	--	--	--	Floating
37	CSI2_D1_N	AE1	MIPI	--	N-side of CSI2_D1 interface
38	NC	--	--	--	Floating
39	CSI2_D1_P	AD1	MIPI	--	P-side of CSI2_D1 interface
40	GND	--	--	--	GND
41	GND	--	--	--	GND
42	NC	--	--	--	Floating
43	CSI2_CLK_N	AF2	MIPI	--	N-side of CSI2_ CLK interface
44	NC	--	--	--	Floating

J2 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
45	CSI2_CLK_P	AE2	MIPI	--	P-side of CSI2_ CLK interface
46	NC	--	--	--	Floating
47	GND	--	--	--	GND
48	NC	--	--	--	Floating
49	CSI2_D2_N	AF3	MIPI	--	N-side of CSI2_D2 interface
50	GND	--	--	--	GND
51	CSI2_D2_P	AE3	MIPI	--	P-side of CSI2_D2 interface
52	CSI1_RESET	U17	2	3.3V	Reset signal
53	GND	--	--	--	GND
54	CSI1_CLK	J26	4	3.3V	Clock signal
55	CSI2_D3_N	AF5	MIPI	--	N-side of CSI2_D3 interface
56	CSI1_SCL	J25	4	3.3V	IIC interface clock signal
57	CSI2_D3_P	AE5	MIPI	--	P-side of CSI2_D3 interface
58	CSI1_SDA	K16	4	3.3V	IIC interface data signal
59	GND	--	--	--	GND
60	GND	--	--	--	GND
61	GND	--	--	--	GND
62	NC	--	--	--	Floating
63	NC	--	--	--	Floating
64	NC	--	--	--	Floating
65	NC	--	--	--	Floating
66	GND	--	--	--	GND
67	NC	--	--	--	Floating
68	NC	--	--	--	Floating
69	NC	--	--	--	Floating

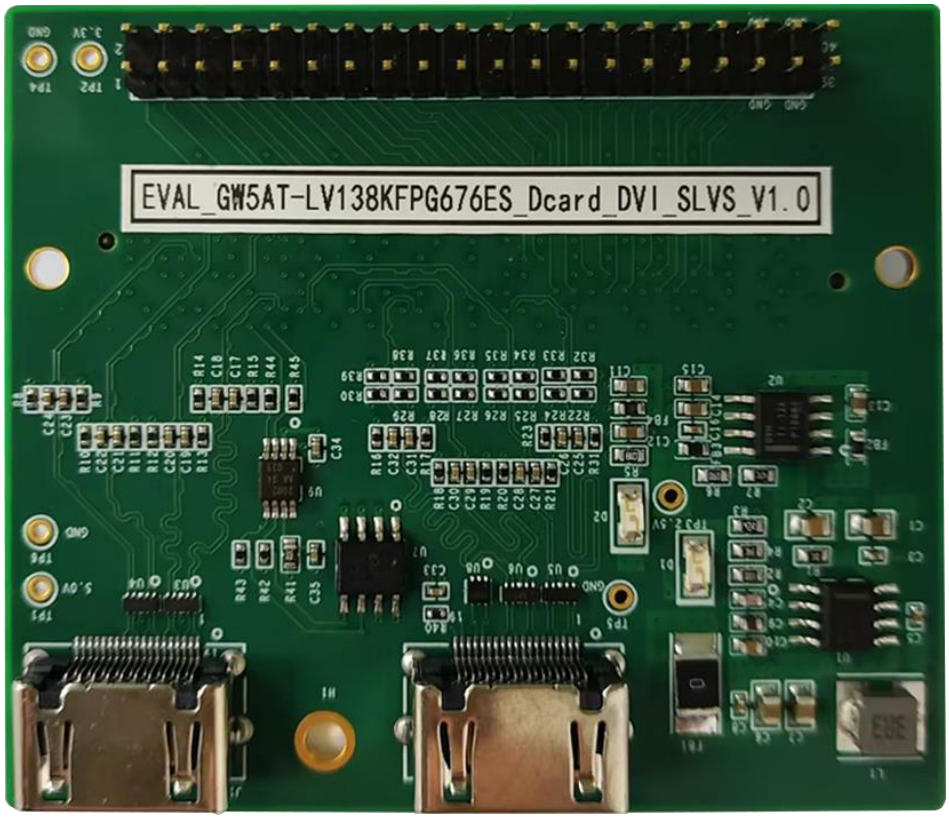
J2 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
70	NC	--	--	--	Floating
71	GND	--	--	--	GND
72	NC	--	--	--	Floating
73	NC	--	--	--	Floating
74	GND	--	--	--	GND
75	NC	--	--	--	Floating
76	AlwaysOn_3.3V	--	--	3.3V	Power
77	NC	--	--	--	Floating
78	AlwaysOn_3.3V	--	--	3.3V	Power
79	NC	--	--	--	Floating
80	AlwaysOn_3.3V	--	--	3.3V	Power

5 DVI Daughter Board

5.1 Introduction

5.1.1 Overview

Figure 5-1 EVAL_GW5AT-LV138KFPG676ES_Dcard_DVI_SLVS_V1.0 Daughter Board



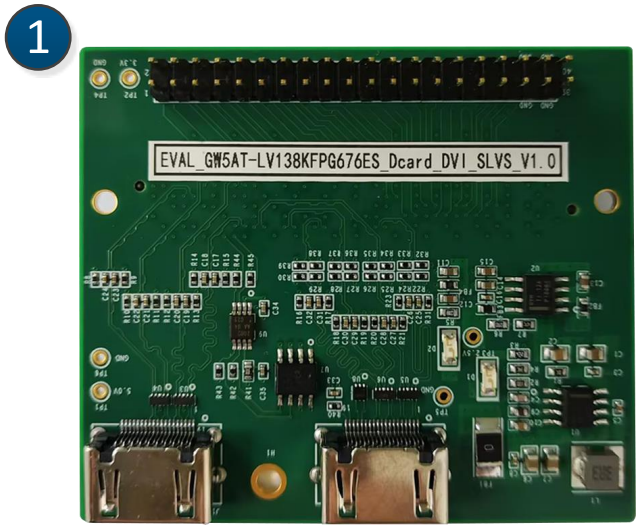
The DVI daughter board needs to be used with the DK_START_GW5AST-LV138FPG676A_V1.0 motherboard, primarily for HDMI communication and DVI evaluation.

5.1.2 A Daughter Board Kit

The daughter board kit includes the following item:

- EVAL_GW5AT-LV138KFPG676ES_Dcard_DVI_SLVS_V1.0 daughter board

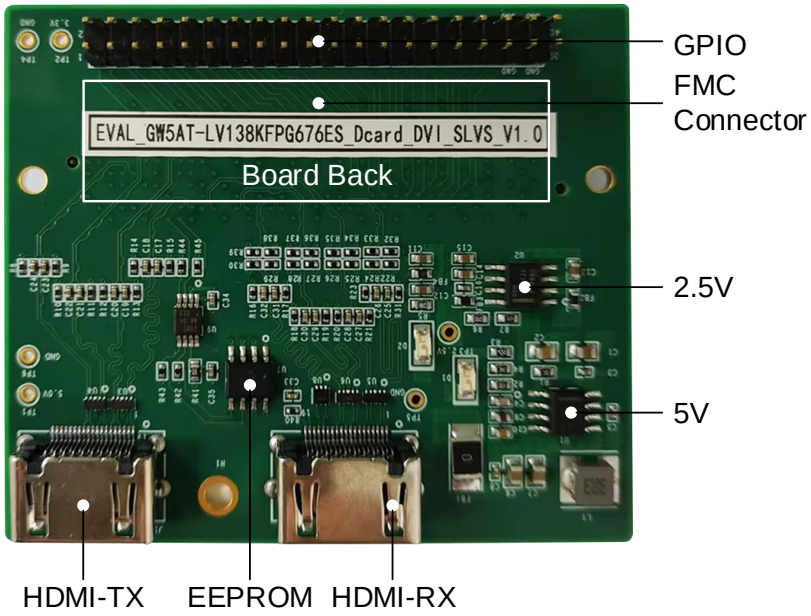
Figure 5-2 A Daughter Board Kit



① EVAL_GW5AT-LV138KFPG676ES_Dcard_DVI_SLVS_V1.0 daughter board

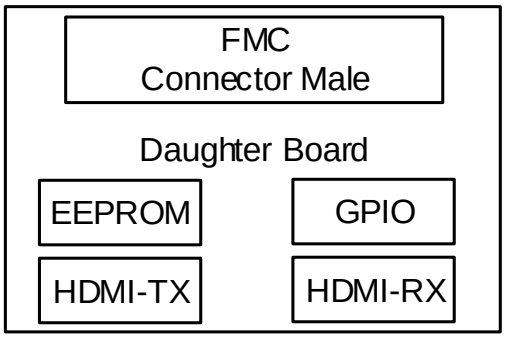
5.1.3 PCB Components

Figure 5-3 PCB Components



5.1.4 System Block Diagram

Figure 5-4 System Block Diagram



5.1.5 Features

The key features are as follows:

1. Power
   - The motherboard provides DC 12V and DC 3.3V power
   - The green Power light is on after power on
2. Memory
   - 4Kbit EEPROM
3. HDMI interface
   - One HDMI-RX interface
   - One HDMI-TX interface
4. GPIO
   - 36 GPIO interfaces
5. Board-to-board connector
   - Use 400Pin FMC connector with 1.27mm pitch
   - Communicate with the DK_START_GW5AST-LV138FPG676A_V1.0 motherboard

5.2 Daughter Board Circuit

5.2.1 Power Supply

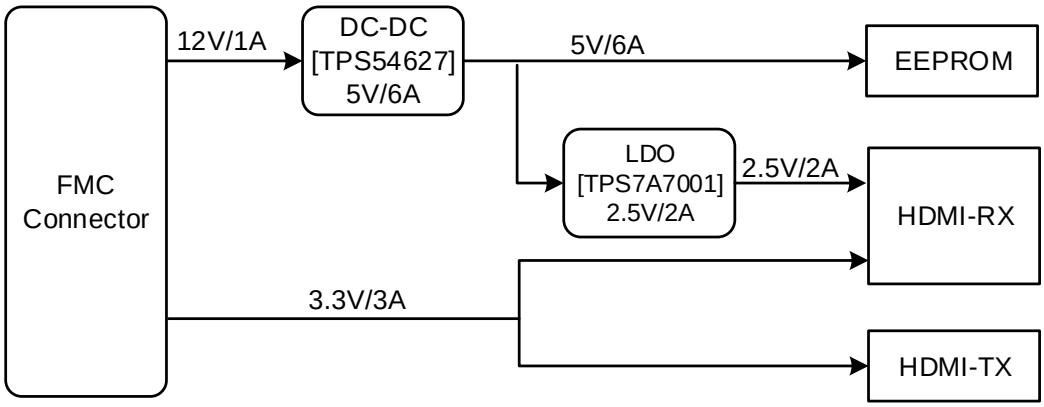
5.2.1.1 Introduction

The motherboard supplies 12V and 3.3V power to the DVI daughter board through the FMC connector.

The input 12V power generates 5V and 2.5V power supply through the power chip on the DVI daughter board to meet the power requirements of the DVI daughter board.

5.2.1.2 Power System Distribution

Figure 5-5 Power Supply System Distribution Diagram

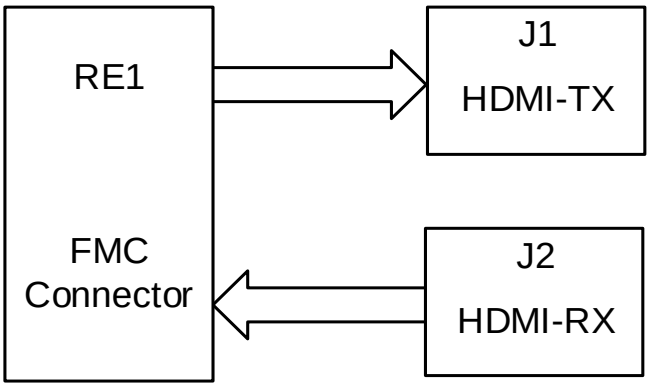


5.2.2 HDMI interface

5.2.2.1 Introduction

The DVI daughter board provides one HDMI input interface and one HDMI output interface. The HDMI I/O interfaces are both directly connected to the FPGA pins via the FMC connector and received/sent via the IP in FPGA. The connection diagram is as follows.

Figure 5-6 Connection Diagram of HDMI Interface



5.2.2.2 Pin Distribution

Table 5-1 J1 Pin Distribution for HDMI-TX Interface

J1 Pin No.	Signal Name	I/O Level	Description
1	HDMI_TXA_2p	3.3V	HDMI differential data
2	GND	--	GND
3	HDMI_TXA_2n	3.3V	HDMI differential data
4	HDMI_TXA_1p	3.3V	HDMI differential data
5	GND	--	GND

J1 Pin No.	Signal Name	I/O Level	Description
6	HDMI_TXA_1n	3.3V	HDMI differential data
7	HDMI_TXA_0p	3.3V	HDMI differential data
8	GND	--	GND
9	HDMI_TXA_0n	3.3V	HDMI differential data
10	HDMI_TXA_Cp	3.3V	HDMI differential clock
11	GND	--	GND
12	HDMI_TXA_Cn	3.3V	HDMI differential clock
13	NC	--	Floating
14	NC	--	Floating
15	NC	--	Floating
16	NC	--	Floating
17	GND	--	GND
18	NC	--	Floating
19	NC	--	Floating
20	GND	--	GND
21	GND	--	GND
22	GND	--	GND
23	GND	--	GND

Table 5-2 J2 Pin Distribution for HDMI-RX Interface

J2 Pin No.	Signal Name	I/O Level	Description
1	HDMI_RXA_2p	3.3V	HDMI differential data
2	GND	--	GND
3	HDMI_RXA_2n	3.3V	HDMI differential data
4	HDMI_RXA_1p	3.3V	HDMI differential data
5	GND	--	GND
6	HDMI_RXA_1n	3.3V	HDMI differential data
7	HDMI_RXA_0p	3.3V	HDMI differential data
8	GND	--	GND
9	HDMI_RXA_0n	3.3V	HDMI differential data
10	HDMI_RXA_Cp	3.3V	HDMI differential clock

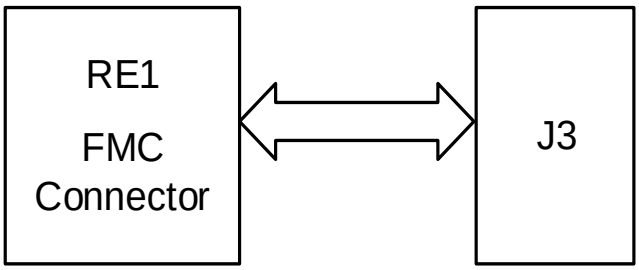
J2 Pin No.	Signal Name	I/O Level	Description
11	GND	--	GND
12	HDMI_RXA_Cn	3.3V	HDMI differential clock
13	NC	--	Floating
14	NC	--	Floating
15	HDMI_DDCA_SCL	5.0V	IIC serial clock
16	HDMI_DDCA_SDA	5.0V	IIC serial clock
17	GND	--	GND
18	NC	--	Short-circuited to pin19
19	NC	--	Short-circuited to pin18
20	GND	--	GND
21	GND	--	GND
22	GND	--	GND
23	GND	--	GND

5.2.3 GPIO

5.2.3.1 Introduction

The DVI daughter board reserves 36 GPIO interfaces for easy testing. The connection diagram is as follows.

Figure 5-7 Connection Diagram of GPIO Interface



5.2.3.2 Pin Distribution

Table 5-3 J3 Pin Distribution for GPIO Connector

J3 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	B2_FMC_E7	E17	5	3.3V	GPIO
2	B2_FMC_E6	E18	5	3.3V	GPIO
3	B2_FMC_E10	F18	5	3.3V	GPIO
4	B2_FMC_E9	F19	5	3.3V	GPIO
5	B2_FMC_E13	G19	5	3.3V	GPIO
6	B2_FMC_E12	F20	5	3.3V	GPIO
7	B2_FMC_E16	C21	5	3.3V	GPIO
8	B2_FMC_E15	E20	5	3.3V	GPIO
9	B2_FMC_E19	B21	5	3.3V	GPIO
10	B2_FMC_E18	D20	5	3.3V	GPIO
11	B2_FMC_K17	C17	5	3.3V	GPIO
12	B2_FMC_K16	B17	5	3.3V	GPIO
13	B2_FMC_F11	K21	4	3.3V	GPIO
14	B2_FMC_F10	J21	4	3.3V	GPIO
15	B2_FMC_F14	G20	4	3.3V	GPIO
16	B2_FMC_F13	G21	4	3.3V	GPIO
17	B2_FMC_F17	K22	4	3.3V	GPIO
18	B2_FMC_F16	K23	4	3.3V	GPIO
19	B2_FMC_F20	J24	4	3.3V	GPIO
20	B2_FMC_F19	H24	4	3.3V	GPIO
21	B2_FMC_F5	H26	4	3.3V	GPIO
22	B2_FMC_F4	G25	4	3.3V	GPIO
23	B2_FMC_F8	G26	4	3.3V	GPIO
24	B2_FMC_F7	L17	4	3.3V	GPIO
25	B2_FMC_J10	F25	4	3.3V	GPIO
26	B2_FMC_J9	G24	4	3.3V	GPIO
27	B2_FMC_J13	L18	4	3.3V	GPIO
28	B2_FMC_J12	F24	4	3.3V	GPIO

J3 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
29	B2_FMC_J16	E26	4	3.3V	GPIO
30	B2_FMC_J15	D26	4	3.3V	GPIO
31	B2_FMC_J19	E25	4	3.3V	GPIO
32	B2_FMC_J18	D25	4	3.3V	GPIO
33	B2_FMC_K8	F23	4	3.3V	GPIO
34	B2_FMC_K7	E23	4	3.3V	GPIO
35	B2_FMC_K11	G22	4	3.3V	GPIO
36	B2_FMC_K10	F22	4	3.3V	GPIO
37	GND	--	--	--	GND
38	GND	--	--	--	GND
39	GND	--	--	--	GND
40	GND	--	--	--	GND

5.2.4 Board-to-board connector

5.2.4.1 Introduction

The DVI daughter board has a 400Pin FMC board-to-board connector with 1.27mm pitch for communication with the DK_START_GW5AST-LV138FPG676A_V1.0 motherboard.

5.2.4.2 Pin Distribution

Table 5-4 Pin Distribution for RE1 Board-to-Board Connector

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
A1	GND	--	--	--	GND
A2	NC	--	--	--	Floating
A3	NC	--	--	--	Floating
A4	GND	--	--	--	GND
A5	GND	--	--	--	GND
A6	NC	--	--	--	Floating
A7	NC	--	--	--	Floating
A8	GND	--	--	--	GND
A9	GND	--	--	--	GND

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
A10	NC	--	--	--	Floating
A11	NC	--	--	--	Floating
A12	GND	--	--	--	GND
A13	GND	--	--	--	GND
A14	NC	--	--	--	Floating
A15	NC	--	--	--	Floating
A16	GND	--	--	--	GND
A17	GND	--	--	--	GND
A18	NC	--	--	--	Floating
A19	NC	--	--	--	Floating
A20	GND	--	--	--	GND
A21	GND	--	--	--	GND
A22	NC	--	--	--	Floating
A23	NC	--	--	--	Floating
A24	GND	--	--	--	GND
A25	GND	--	--	--	GND
A26	NC	--	--	--	Floating
A27	NC	--	--	--	Floating
A28	GND	--	--	--	GND
A29	GND	--	--	--	GND
A30	NC	--	--	--	Floating
A31	NC	--	--	--	Floating
A32	GND	--	--	--	GND
A33	GND	--	--	--	GND
A34	NC	--	--	--	Floating
A35	NC	--	--	--	Floating
A36	GND	--	--	--	GND
A37	GND	--	--	--	GND
A38	NC	--	--	--	Floating
A39	NC	--	--	--	Floating

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
A40	GND	--	--	--	GND
B1	NC	--	--	--	Floating
B2	GND	--	--	--	GND
B3	GND	--	--	--	GND
B4	NC	--	--	--	Floating
B5	NC	--	--	--	Floating
B6	GND	--	--	--	GND
B7	GND	--	--	--	GND
B8	NC	--	--	--	Floating
B9	NC	--	--	--	Floating
B10	GND	--	--	--	GND
B11	GND	--	--	--	GND
B12	NC	--	--	--	Floating
B13	NC	--	--	--	Floating
B14	GND	--	--	--	GND
B15	GND	--	--	--	GND
B16	NC	--	--	--	Floating
B17	NC	--	--	--	Floating
B18	GND	--	--	--	GND
B19	GND	--	--	--	GND
B20	NC	--	--	--	Floating
B21	NC	--	--	--	Floating
B22	GND	--	--	--	GND
B23	GND	--	--	--	GND
B24	NC	--	--	--	Floating
B25	NC	--	--	--	Floating
B26	GND	--	--	--	GND
B27	GND	--	--	--	GND
B28	NC	--	--	--	Floating
B29	NC	--	--	--	Floating

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
B30	GND	--	--	--	GND
B31	GND	--	--	--	GND
B32	NC	--	--	--	Floating
B33	NC	--	--	--	Floating
B34	GND	--	--	--	GND
B35	GND	--	--	--	GND
B36	NC	--	--	--	Floating
B37	NC	--	--	--	Floating
B38	GND	--	--	--	GND
B39	GND	--	--	--	GND
B40	NC	--	--	--	Floating
C1	GND	--	--	--	GND
C2	NC	--	--	--	Floating
C3	NC	--	--	--	Floating
C4	GND	--	--	--	GND
C5	GND	--	--	--	GND
C6	NC	--	--	--	Floating
C7	NC	--	--	--	Floating
C8	GND	--	--	--	GND
C9	GND	--	--	--	GND
C10	B2_FMC_E10	F18	5	3.3V	GPIO
C11	B2_FMC_E9	F19	5	3.3V	GPIO
C12	GND	--	--	--	GND
C13	GND	--	--	--	GND
C14	B2_FMC_E15	E20	5	3.3V	GPIO
C15	B2_FMC_E18	D20	5	3.3V	GPIO
C16	GND	--	--	--	GND
C17	GND	--	--	--	GND
C18	B2_FMC_K17	C17	5	3.3V	GPIO
C19	B2_FMC_K16	B17	5	3.3V	GPIO

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
C20	GND	--	--	--	GND
C21	GND	--	--	--	GND
C22	B2_FMC_F14	G20	4	3.3V	GPIO
C23	B2_FMC_F14	G21	4	3.3V	GPIO
C24	GND	--	--	--	GND
C25	GND	--	--	--	GND
C26	B2_FMC_F4	G25	4	3.3V	GPIO
C27	B2_FMC_J10	F25	4	3.3V	GPIO
C28	GND	--	--	--	GND
C29	GND	--	--	--	GND
C30	NC	--	--	--	Floating
C31	NC	--	--	--	Floating
C32	GND	--	--	--	GND
C33	GND	--	--	--	GND
C34	GND	--	--	--	GND
C35	VCC12P0	--	--	12V	Power
C36	GND	--	--	--	GND
C37	VCC12P0	--	--	12V	Power
C38	GND	--	--	--	GND
C39	VCC3P3	--	--	3.3V	Power
C40	GND	--	--	--	GND
D1	NC	--	--	--	Floating
D2	GND	--	--	--	GND
D3	GND	--	--	--	GND
D4	NC	--	--	--	Floating
D5	NC	--	--	--	Floating
D6	GND	--	--	--	GND
D7	GND	--	--	--	GND
D8	B2_FMC_E7	E17	5	3.3V	GPIO
D9	B2_FMC_E6	E18	5	3.3V	GPIO

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
D10	GND	--	--	--	GND
D11	B2_FMC_E13	G19	5	3.3V	GPIO
D12	B2_FMC_E12	F20	5	3.3V	GPIO
D13	GND	--	--	--	GND
D14	B2_FMC_E16	C21	5	3.3V	GPIO
D15	B2_FMC_E19	B21	5	3.3V	GPIO
D16	GND	--	--	--	GND
D17	NC	--	--	--	Floating
D18	NC	--	--	--	Floating
D19	GND	--	--	--	GND
D20	B2_FMC_F11	K21	4	3.3V	GPIO
D21	B2_FMC_F10	J21	4	3.3V	GPIO
D22	GND	--	--	--	GND
D23	B2_FMC_F17	K22	4	3.3V	GPIO
D24	B2_FMC_F16	K23	4	3.3V	GPIO
D25	GND	--	--	--	GND
D26	B2_FMC_F7	L17	4	3.3V	GPIO
D27	B2_FMC_J13	L18	4	3.3V	GPIO
D28	GND	--	--	--	GND
D29	NC	--	--	--	Floating
D30	NC	--	--	--	Floating
D31	NC	--	--	--	Floating
D32	NC	--	--	--	Floating
D33	NC	--	--	--	Floating
D34	NC	--	--	--	Floating
D35	GND	--	--	--	GND
D36	VCC3P3	--	--	3.3V	Power
D37	GND	--	--	--	GND
D38	VCC3P3	--	--	3.3V	Power
D39	GND	--	--	--	GND

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
D40	VCC3P3	--	--	3.3V	Power
E1	GND	--	--	--	GND
E2	NC	--	--	--	Floating
E3	NC	--	--	--	Floating
E4	GND	--	--	--	GND
E5	GND	--	--	--	GND
E6	HDMI_TX_0p	V23	2	2.5V	TMDS data signal
E7	HDMI_TX_0n	W23	2	2.5V	TMDS data signal
E8	GND	--	--	--	GND
E9	HDMI_TX_1p	V19	2	2.5V	TMDS data signal
E10	HDMI_TX_1n	W19	2	2.5V	TMDS data signal
E11	GND	--	--	--	Floating
E12	NC	--	--	--	Floating
E13	NC	--	--	--	Floating
E14	GND	--	--	--	GND
E15	NC	--	--	--	Floating
E16	NC	--	--	--	Floating
E17	GND	--	--	--	GND
E18	NC	--	--	--	Floating
E19	NC	--	--	--	Floating
E20	GND	--	--	--	GND
E21	NC	--	--	--	Floating
E22	NC	--	--	--	Floating
E23	GND	--	--	--	GND
E24	NC	--	--	--	Floating
E25	NC	--	--	--	Floating
E26	GND	--	--	--	GND
E27	NC	--	--	--	Floating
E28	NC	--	--	--	Floating
E29	GND	--	--	--	GND

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
E30	NC	--	--	--	Floating
E31	NC	--	--	--	Floating
E32	GND	--	--	--	GND
E33	NC	--	--	--	Floating
E34	NC	--	--	--	Floating
E35	GND	--	--	--	GND
E36	NC	--	--	--	Floating
E37	NC	--	--	--	Floating
E38	GND	--	--	--	GND
E39	NC	--	--	--	Floating
E40	GND	--	--	--	GND
F1	NC	--	--	--	Floating
F2	GND	--	--	--	GND
F3	GND	--	--	--	GND
F4	HDMI_TX_Cp	U21	2	2.5V	TMDS clock signal
F5	HDMI_TX_Cn	V21	2	2.5V	TMDS clock signal
F6	GND	--	--	--	GND
F7	NC	--	--	--	Floating
F8	NC	--	--	--	Floating
F9	GND	--	--	--	GND
F10	NC	--	--	--	Floating
F11	NC	--	--	--	Floating
F12	GND	--	--	--	GND
F13	NC	--	--	--	Floating
F14	NC	--	--	--	Floating
F15	GND	--	--	--	GND
F16	NC	--	--	--	Floating
F17	NC	--	--	--	Floating
F18	GND	--	--	--	GND
F19	NC	--	--	--	Floating

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F20	NC	--	--	--	Floating
F21	GND	--	--	--	GND
F22	NC	--	--	--	Floating
F23	NC	--	--	--	Floating
F24	GND	--	--	--	GND
F25	NC	--	--	--	Floating
F26	NC	--	--	--	Floating
F27	GND	--	--	--	GND
F28	NC	--	--	--	Floating
F29	NC	--	--	--	Floating
F30	GND	--	--	--	GND
F31	NC	--	--	--	Floating
F32	NC	--	--	--	Floating
F33	GND	--	--	--	GND
F34	NC	--	--	--	Floating
F35	NC	--	--	--	Floating
F36	GND	--	--	--	GND
F37	NC	--	--	--	Floating
F38	NC	--	--	--	Floating
F39	GND	--	--	--	GND
F40	NC	--	--	--	Floating
G1	GND	--	--	--	GND
G2	NC	--	--	--	Floating
G3	NC	--	--	--	Floating
G4	GND	--	--	--	GND
G5	GND	--	--	--	GND
G6	NC	--	--	--	Floating
G7	NC	--	--	--	Floating
G8	GND	--	--	--	GND
G9	NC	--	--	--	Floating

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
G10	NC	--	--	--	Floating
G11	GND	--	--	--	GND
G12	NC	--	--	--	Floating
G13	NC	--	--	--	Floating
G14	GND	--	--	--	GND
G15	NC	--	--	--	Floating
G16	NC	--	--	--	Floating
G17	GND	--	--	--	GND
G18	NC	--	--	--	Floating
G19	NC	--	--	--	Floating
G20	GND	--	--	--	GND
G21	NC	--	--	--	Floating
G22	NC	--	--	--	Floating
G23	GND	--	--	--	GND
G24	B2_FMC_F20	J24	4	3.3V	GPIO
G25	B2_FMC_F19	H24	4	3.3V	GPIO
G26	GND	--	--	--	GND
G27	B2_FMC_J9	G24	4	3.3V	GPIO
G28	B2_FMC_J12	F24	4	3.3V	GPIO
G29	GND	--	--	--	GND
G30	B2_FMC_J19	E25	4	3.3V	GPIO
G31	B2_FMC_J18	D25	4	3.3V	GPIO
G32	GND	--	--	--	GND
G33	B2_FMC_K11	G22	4	3.3V	GPIO
G34	B2_FMC_K10	F22	4	3.3V	GPIO
G35	GND	--	--	--	GND
G36	NC	--	--	--	Floating
G37	NC	--	--	--	Floating
G38	GND	--	--	--	GND
G39	NC	--	--	--	Floating

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
G40	GND	--	--	--	GND
H1	NC	--	--	--	Floating
H2	NC	--	--	--	Floating
H3	GND	--	--	--	GND
H4	NC	--	--	--	Floating
H5	NC	--	--	--	Floating
H6	GND	--	--	--	GND
H7	NC	--	--	--	Floating
H8	NC	--	--	--	Floating
H9	GND	--	--	--	GND
H10	NC	--	--	--	Floating
H11	NC	--	--	--	Floating
H12	GND	--	--	--	GND
H13	NC	--	--	--	Floating
H14	NC	--	--	--	Floating
H15	GND	--	--	--	GND
H16	NC	--	--	--	Floating
H17	NC	--	--	--	Floating
H18	GND	--	--	--	GND
H19	NC	--	--	--	Floating
H20	NC	--	--	--	Floating
H21	GND	--	--	--	GND
H22	NC	--	--	--	Floating
H23	NC	--	--	--	Floating
H24	GND	--	--	--	GND
H25	B2_FMC_F5	H26	4	3.3V	GPIO
H26	B2_FMC_F8	G26	4	3.3V	GPIO
H27	GND	--	--	--	GND
H28	B2_FMC_J16	E26	4	3.3V	GPIO
H29	B2_FMC_J15	D26	4	3.3V	GPIO

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
H30	GND	--	--	--	GND
H31	B2_FMC_K8	F23	4	3.3V	GPIO
H32	B2_FMC_K7	E23	4	3.3V	GPIO
H33	GND	--	--	--	GND
H34	NC	--	--	--	Floating
H35	NC	--	--	--	Floating
H36	GND	--	--	--	GND
H37	NC	--	--	--	Floating
H38	NC	--	--	--	Floating
H39	GND	--	--	--	GND
H40	NC	--	--	--	Floating
J1	GND	--	--	--	GND
J2	NC	--	--	--	Floating
J3	NC	--	--	--	Floating
J4	GND	--	--	--	GND
J5	GND	--	--	--	GND
J6	NC	--	--	--	Floating
J7	NC	--	--	--	Floating
J8	GND	--	--	--	GND
J9	HDMI_TX_2p	V18	2	2.5V	TMDS data signal
J10	HDMI_TX_2n	W18	2	2.5V	TMDS data signal
J11	GND	--	--	--	GND
J12	NC	--	--	--	Floating
J13	NC	--	--	--	Floating
J14	GND	--	--	--	GND
J15	NC	--	--	--	Floating
J16	NC	--	--	--	Floating
J17	GND	--	--	--	GND
J18	NC	--	--	--	Floating
J19	NC	--	--	--	Floating

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
J20	GND	--	--	--	GND
J21	NC	--	--	--	Floating
J22	NC	--	--	--	Floating
J23	GND	--	--	--	GND
J24	NC	--	--	--	Floating
J25	NC	--	--	--	Floating
J26	GND	--	--	--	GND
J27	NC	--	--	--	Floating
J28	NC	--	--	--	Floating
J29	GND	--	--	--	GND
J30	NC	--	--	--	Floating
J31	NC	--	--	--	Floating
J32	GND	--	--	--	GND
J33	NC	--	--	--	Floating
J34	NC	--	--	--	Floating
J35	GND	--	--	--	GND
J36	NC	--	--	--	Floating
J37	NC	--	--	--	Floating
J38	GND	--	--	--	GND
J39	NC	--	--	--	Floating
J40	GND	--	--	--	GND
K1	NC	--	--	--	Floating
K2	GND	--	--	--	GND
K3	GND	--	--	--	GND
K4	NC	--	--	--	Floating
K5	NC	--	--	--	Floating
K6	GND	--	--	--	GND
K7	HDMI_SCL	T14	2	2.5V	DDC clock line
K8	HDMI_SDA	T15	2	2.5V	DDC data line
K9	GND	--	--	--	GND

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
K10	HDMI_RX_1p	U15	2	2.5V	TMDS data signal
K11	HDMI_RX_1n	U16	2	2.5V	TMDS data signal
K12	GND	--	--	--	GND
K13	HDMI_RX_0p	T20	2	2.5V	TMDS data signal
K14	HDMI_RX_0n	U20	2	2.5V	TMDS data signal
K15	GND	--	--	--	GND
K16	HDMI_RX_Cp	Y22	2	2.5V	TMDS data signal
K17	HDMI_RX_Cn	Y23	2	2.5V	TMDS data signal
K18	GND	--	--	--	GND
K19	NC	--	--	--	Floating
K20	NC	--	--	--	Floating
K21	GND	--	--	--	GND
K22	HDMI_RX_2p	T19	2	2.5V	TMDS data signal
K23	HDMI_RX_2n	U19	2	2.5V	TMDS data signal
K24	GND	--	--	--	GND
K25	NC	--	--	--	Floating
K26	NC	--	--	--	Floating
K27	GND	--	--	--	GND
K28	NC	--	--	--	Floating
K29	NC	--	--	--	Floating
K30	GND	--	--	--	GND
K31	NC	--	--	--	Floating
K32	NC	--	--	--	Floating
K33	GND	--	--	--	GND
K34	NC	--	--	--	Floating
K35	NC	--	--	--	Floating
K36	GND	--	--	--	GND
K37	NC	--	--	--	Floating
K38	NC	--	--	--	Floating
K39	GND	--	--	--	GND

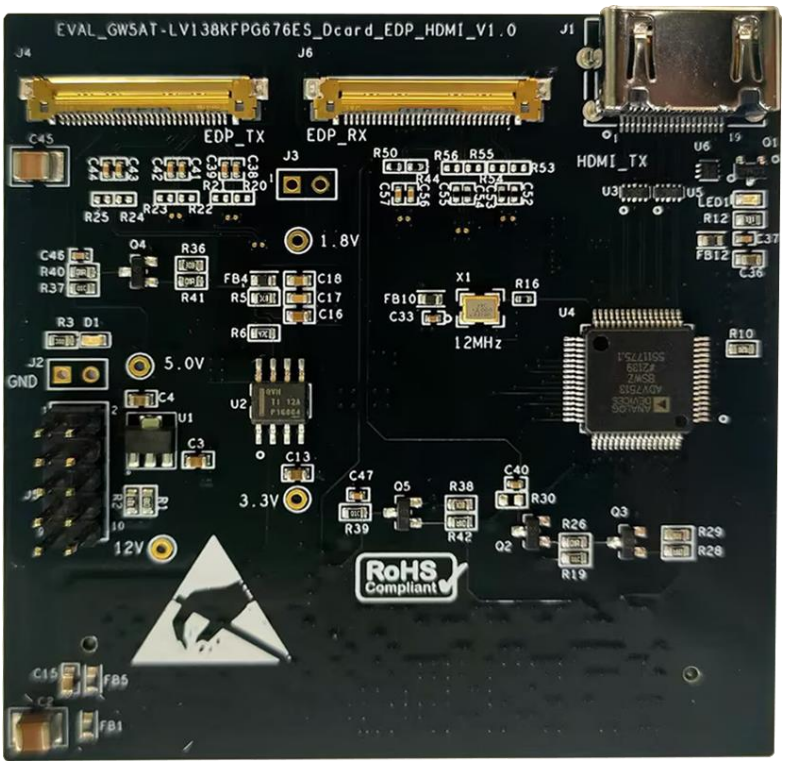
RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
K40	NC	--	--	--	Floating

6 EDP Daughter Board

6.1 Introduction

6.1.1 Overview

Figure 6-1 EVAL_GW5AT-LV138KFPG676ES_Dcard_EDP_HDMI_V1.0 Daughter Board



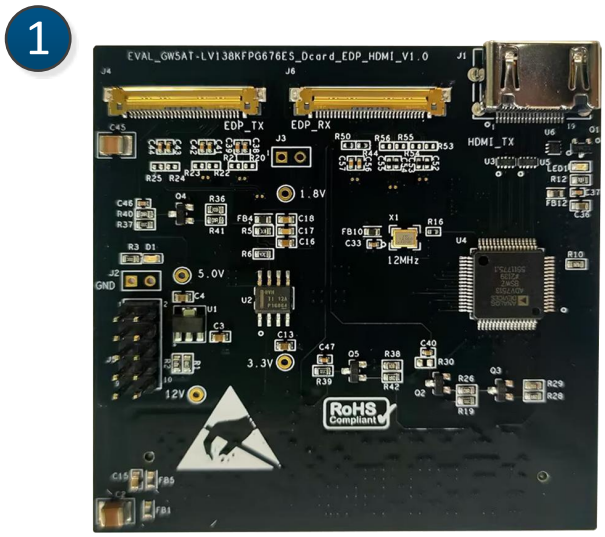
The EDP daughter board needs to be used with the DK_START_GW5AST-LV138FPG676A_V1.0 motherboard, primarily for EDP communication and HDMI communication.

6.1.2 A Daughter Board Kit

The daughter board kit includes the following item:

- EVAL_GW5AT-LV138KFPG676ES_Dcard_EDP_HDMI_V1.0

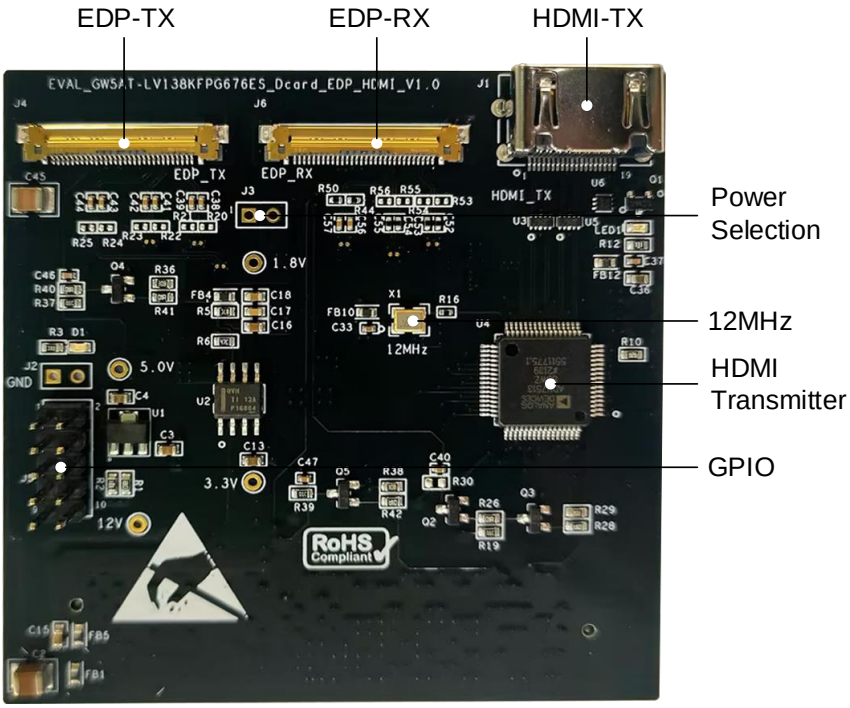
Figure 6-2 A Daughter Board Kit



① EVAL_GW5AT-LV138KFPG676ES_Dcard_EDP_HDMI_V1.0 daughter board

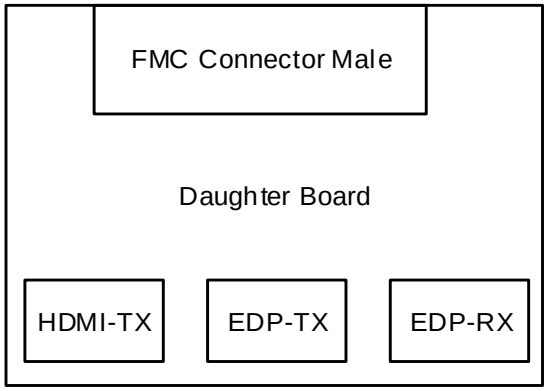
6.1.3 PCB Components

Figure 6-3 PCB Components



6.1.4 System Block Diagram

Figure 6-4 System Block Diagram



6.1.5 Features

The key features are as follows:

1. Power
   - The motherboard provides DC 12V and DC 3.3V power
   - The green Power light is on after power on
2. EDP interface
   - One EDP-RX interface
   - One EDP-TX interface
3. HDMI interface
   - One HDMI-TX interface for HDMI-TX communication via the ADV7513 encoding chip
4. Board-to-board connector
   - Use 80Pin board-to-board connector with 0.5mm pitch
   - Communicate with the DK_START_GW5AST-LV138FPG676A_V1.0 motherboard

6.2 Daughter Board Circuit

6.2.1 Power Supply

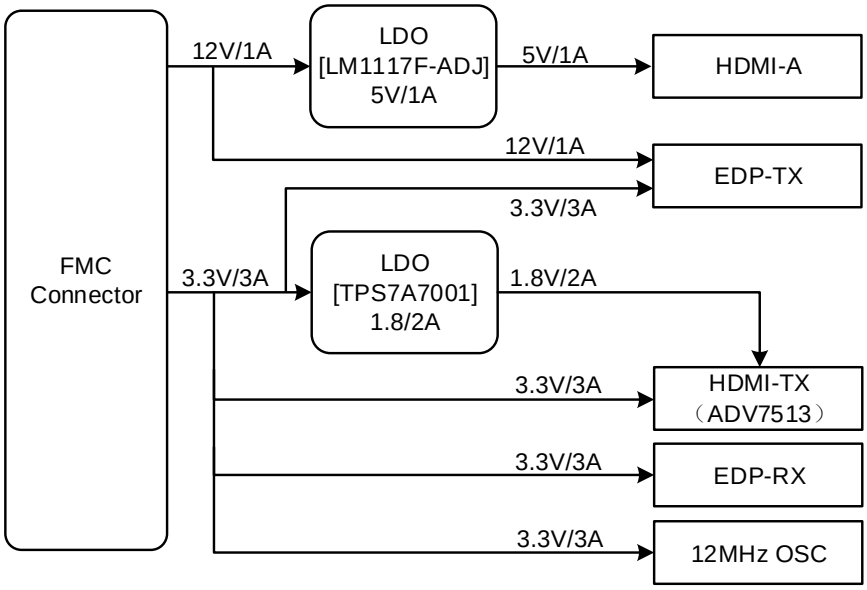
6.2.1.1 Introduction

The motherboard supplies 12V and 3.3V power to the daughter board through the FMC connector.

The input 12V and 3.3V power generates 5V and 1.8V power supply through the power chip on the daughter board to meet the power requirements of the daughter board.

6.2.1.2 Power System Distribution

Figure 6-5 Power Supply System Distribution Diagram



6.2.2 EDP interface

6.2.2.1 Introduction

The EDP daughter board provides one EDP input interface and one EDP output interface. The connection diagram is as follows.

Figure 6-6 Connection Diagram of EDP-TX Interface

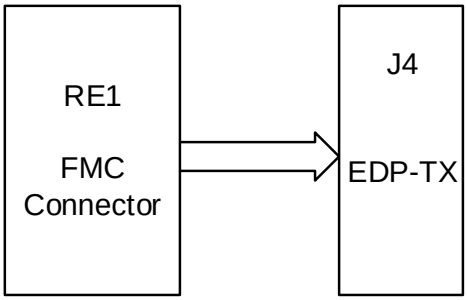
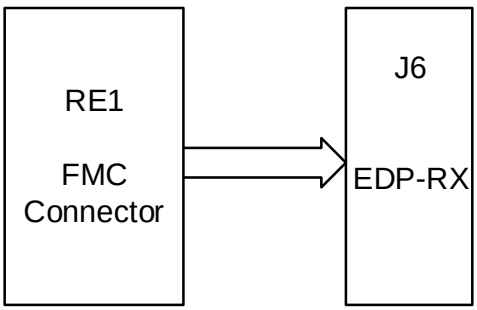


Figure 6-7 Connection Diagram of EDP-RX Interface



6.2.2.2 Pin Distribution

Table 6-1 J4 Pin Distribution for EDP-TX Interface

J4 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	NC	--	--	--	Floating
2	GND	--	--	--	GND
3	EDPTX_LA_1N	AF9	Q1	--	EDP Data Transmit
4	EDPTX_LA_1P	AE9	Q1	--	EDP Data Transmit
5	GND	--	--	--	GND
6	EDPTX_LA_0N	AD8	Q1	--	EDP Data Transmit
7	EDPTX_LA_0P	AC8	Q1	--	EDP Data Transmit
8	GND	--	--	--	GND
9	EDPTX_AUX_P_1	E16	5	1.8V	Auxiliary channel
10	EDPTX_AUX_N_1	D16	5	1.8V	Auxiliary channel
11	GND	--	--	--	GND
12	VCCS_PAD	D18	5	1.8V	EDP screen test
13	VCCS_PAD	D18	5	1.8V	EDP screen test
14	NC	--	--	--	Floating
15	GND	--	--	--	GND
16	GND	--	--	--	GND
17	EDPTX_HPD1	B17	5	1.8V	Hot Plug Detect
18	GND	--	--	--	GND
19	GND	--	--	--	GND
20	GND	--	--	--	GND
21	GND	--	--	--	GND
22	LED_EN	C18	5	1.8V	Self-test enable
23	LED_PWM	A17	5	1.8V	PWM backlight control
24	NC	--	--	--	Floating
25	NC	--	--	--	Floating

J4 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
26	VCC12P0	--	--	12V	Power
27	VCC12P0	--	--	12V	Power
28	VCC12P0	--	--	12V	Power
29	VCC12P0	--	--	12V	Power
30	NC	--	--	--	Floating
31	GND	--	--	--	GND
32	GND	--	--	--	GND
33	GND	--	--	--	GND
34	GND	--	--	--	GND

Table 6-2 J6 Pin Distribution for EDP-RX Interface

J6 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	NC	--	--	--	Floating
2	GND	--	--	--	GND
3	EDP2RX_LA_1N	AD14	Q1	--	EDP Data Receive
4	EDP2RX_LA_1P	AC14	Q1	--	EDP Data Receive
5	GND	--	--	--	GND
6	EDP2RX_LA_0N	AF13	Q1	--	EDP Data Receive
7	EDP2RX_LA_0P	AE13	Q1	--	EDP Data Receive
8	GND	--	--	--	GND
9	EDP2RX_AUX_P_1	C21	5	1.8V	Auxiliary channel
10	EDP2RX_AUX_N_1	B21	5	1.8V	Auxiliary channel
11	GND	--	--	--	GND
12	NC	--	--	--	Floating
13	NC	--	--	--	Floating

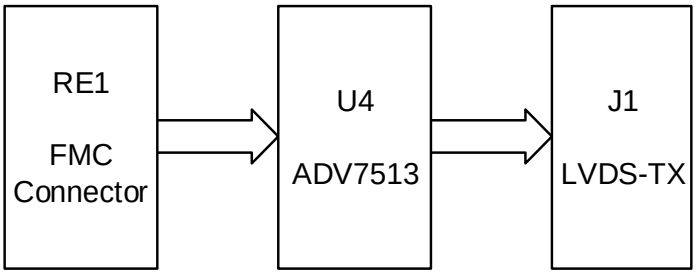
J6 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
14	NC	--	--	--	Floating
15	GND	--	--	--	GND
16	GND	--	--	--	GND
17	EDPRX_HPD1	C17	5	1.8V	Hot Plug Detect
18	GND	--	--	--	GND
19	GND	--	--	--	GND
20	GND	--	--	--	GND
21	GND	--	--	--	GND
22	NC	--	--	--	Floating
23	NC	--	--	--	Floating
24	NC	--	--	--	Floating
25	NC	--	--	--	Floating
26	NC	--	--	--	Floating
27	NC	--	--	--	Floating
28	NC	--	--	--	Floating
29	NC	--	--	--	Floating
30	NC	--	--	--	Floating
31	GND	--	--	--	GND
32	GND	--	--	--	GND
33	GND	--	--	--	GND
34	GND	--	--	--	GND

6.2.3 HDMI interface

6.2.3.1 Introduction

The EDP daughter board provides one HDMI output Interface. HDMI-TX communication is implemented via the ADV7513 encoding chip. The connection diagram is as follows.

Figure 6-8 Connection Diagram of HDMI-TX Interface



6.2.3.2 Pin Distribution

Table 6-3 J1 Pin Distribution for HDMI-TX Interface

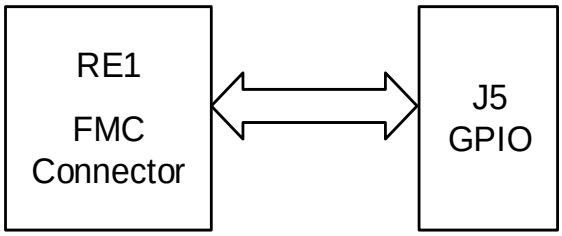
J1 Pin No.	Signal Name	I/O Level	Description
1	HDMI_TXA2P	3.3V	HDMI differential data
2	GND	--	GND
3	HDMI_TXA2N	3.3V	HDMI differential data
4	HDMI_TXA1P	3.3V	HDMI differential data
5	GND	--	GND
6	HDMI_TXA1N	3.3V	HDMI differential data
7	HDMI_TXA0P	3.3V	HDMI differential data
8	GND	--	GND
9	HDMI_TXA0N	3.3V	HDMI differential data
10	HDMI_TXACP	3.3V	HDMI differential clock
11	GND	--	GND
12	HDMI_TXACN	3.3V	HDMI differential clock
13	HDMI_CEC	3.3V	CEC control signal
14	NC	--	Floating
15	HDMI_DDC_SCL	5V	I2C serial clock
16	HDMI_DDC_SDA	5V	I2C serial data
17	GND	--	GND
18	HDMI_5V	5V	Power
19	HDMI_HPD	5V	Hot Plug Detect
20	GND	--	GND
21	GND	--	GND
22	GND	--	GND
23	GND	--	GND

6.2.4 GPIO

6.2.4.1 Introduction

The EDP daughter board reserves six 3.3V GPIO expansion interfaces for easy testing. The connection diagram is as follows.

Figure 6-9 Connection Diagram of GPIO Interface



6.2.4.2 Pin Distribution

Table 6-4 J5 Pin Distribution for GPIO Connector

J5 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	GND	--	--	--	GND
2	GND	--	--	--	GND
3	GW_G20	G20	4	3.3V	GPIO
4	GW_K21	K21	4	3.3V	GPIO
5	GW_G21	G21	4	3.3V	GPIO
6	GW_J21	J21	4	3.3V	GPIO
7	GW_F23	G25	4	3.3V	GPIO
8	GW_E23	F25	4	3.3V	GPIO
9	GND	--	--	--	GND
10	GND	--	--	--	GND

6.2.5 Board-to-board connector

6.2.5.1 Introduction

The EDP daughter board has a 400Pin FMC board-to-board connector with 1.27mm pitch for communication with the DK_START_GW5AST-LV138FPG676A_V1.0 motherboard.

6.2.5.2 Pin Distribution

Table 6-5 Pin Distribution for RE1 Board-to-Board Connector

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
A1	GND	--	--	--	GND
A2	EDP2RX_LANE_0P	AE13	Q1	--	EDP receive data
A3	EDP2RX_LANE_0N	AF13	Q1	--	EDP receive data
A4	GND	--	--	--	GND
A5	GND	--	--	--	GND
A6	NC	--	--	--	Floating
A7	NC	--	--	--	Floating
A8	GND	--	--	--	GND
A9	GND	--	--	--	GND
A10	NC	--	--	--	Floating
A11	NC	--	--	--	Floating
A12	GND	--	--	--	GND
A13	GND	--	--	--	GND
A14	NC	--	--	--	Floating
A15	NC	--	--	--	Floating
A16	GND	--	--	--	GND
A17	GND	--	--	--	GND
A18	NC	--	--	--	Floating
A19	NC	--	--	--	Floating
A20	GND	--	--	--	GND
A21	GND	--	--	--	GND
A22	EDPTX_LANE_1P	AE9	Q1	--	EDP transmit data
A23	EDPTX_LANE_1N	AF9	Q1	--	EDP transmit data
A24	GND	--	--	--	GND
A25	GND	--	--	--	GND
A26	NC	--	--	--	Floating
A27	NC	--	--	--	Floating
A28	GND	--	--	--	GND

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
A29	GND	--	--	--	GND
A30	NC	--	--	--	Floating
A31	NC	--	--	--	Floating
A32	GND	--	--	--	GND
A33	GND	--	--	--	GND
A34	NC	--	--	--	Floating
A35	NC	--	--	--	Floating
A36	GND	--	--	--	GND
A37	GND	--	--	--	GND
A38	NC	--	--	--	Floating
A39	NC	--	--	--	Floating
A40	GND	--	--	--	GND
B1	NC	--	--	--	Floating
B2	GND	--	--	--	GND
B3	GND	--	--	--	GND
B4	NC	--	--	--	Floating
B5	NC	--	--	--	Floating
B6	GND	--	--	--	GND
B7	GND	--	--	--	GND
B8	NC	--	--	--	Floating
B9	NC	--	--	--	Floating
B10	GND	--	--	--	GND
B11	GND	--	--	--	GND
B12	NC	--	--	--	Floating
B13	NC	--	--	--	Floating
B14	GND	--	--	--	GND
B15	GND	--	--	--	GND
B16	NC	--	--	--	Floating
B17	NC	--	--	--	Floating
B18	GND	--	--	--	GND

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
B19	GND	--	--	--	GND
B20	NC	--	--	--	Floating
B21	NC	--	--	--	Floating
B22	GND	--	--	--	GND
B23	GND	--	--	--	GND
B24	NC	--	--	--	Floating
B25	NC	--	--	--	Floating
B26	GND	--	--	--	GND
B27	GND	--	--	--	GND
B28	NC	--	--	--	Floating
B29	NC	--	--	--	Floating
B30	GND	--	--	--	GND
B31	GND	--	--	--	GND
B32	NC	--	--	--	Floating
B33	NC	--	--	--	Floating
B34	GND	--	--	--	GND
B35	GND	--	--	--	GND
B36	NC	--	--	--	Floating
B37	NC	--	--	--	Floating
B38	GND	--	--	--	GND
B39	GND	--	--	--	GND
B40	NC	--	--	--	Floating
C1	GND	--	--	--	GND
C2	EDPTX_LANE_0P	AC8	Q1	--	EDP transmit data
C3	EDPTX_LANE_0N	AD8	Q1	--	EDP transmit data
C4	GND	--	--	--	GND
C5	GND	--	--	--	GND
C6	EDP2RX_LANE_1P	AC14	Q1	--	EDP receive data
C7	EDP2RX_LANE_1N	AD14	Q1	--	EDP receive data
C8	GND	--	--	--	GND

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
C9	GND	--	--	--	GND
C10	NC	--	--	--	Floating
C11	NC	--	--	--	Floating
C12	GND	--	--	--	GND
C13	GND	--	--	--	GND
C14	NC	--	--	--	Floating
C15	NC	--	--	--	Floating
C16	GND	--	--	--	GND
C17	GND	--	--	--	GND
C18	EDPRX_HPD1	C17	5	1.8V	Hot Plug Detect
C19	EDPTX_HPD1	B17	5	1.8V	Hot Plug Detect
C20	GND	--	--	--	GND
C21	GND	--	--	--	GND
C22	GW_G20	G20	4	3.3V	GPIO
C23	GW_G21	G21	4	3.3V	GPIO
C24	GND	--	--	--	GND
C25	GND	--	--	--	GND
C26	GW_F23	G25	4	3.3V	GPIO
C27	GW_E23	F25	4	3.3V	GPIO
C28	GND	--	--	--	GND
C29	GND	--	--	--	GND
C30	NC	--	--	--	Floating
C31	NC	--	--	--	Floating
C32	GND	--	--	--	GND
C33	GND	--	--	--	GND
C34	GND	--	--	--	GND
C35	FMC_VCC12P0	--	--	12V	Power
C36	GND	--	--	--	GND
C37	FMC_VCC12P0	--	--	12V	Power
C38	GND	--	--	--	GND

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
C39	FMC_VCC3P3	--	--	3.3V	Power
C40	GND	--	--	--	GND
D1	NC	--	--	--	Floating
D2	GND	--	--	--	GND
D3	GND	--	--	--	GND
D4	NC	--	--	--	Floating
D5	NC	--	--	--	Floating
D6	GND	--	--	--	GND
D7	GND	--	--	--	GND
D8	NC	--	--	--	Floating
D9	NC	--	--	--	Floating
D10	GND	--	--	--	GND
D11	NC	--	--	--	Floating
D12	NC	--	--	--	Floating
D13	GND	--	--	--	GND
D14	EDP2RX_AUX_CH_P_1	C21	5	1.8V	Auxiliary channel
D15	EDP2RX_AUX_CH_N_1	B21	5	1.8V	Auxiliary channel
D16	GND	--	--	--	GND
D17	NC	--	--	--	Floating
D18	NC	--	--	--	Floating
D19	GND	--	--	--	GND
D20	GW_K21	K21	4	3.3V	GPIO
D21	GW_J21	J21	4	3.3V	GPIO
D22	GND	--	--	--	GND
D23	NC	--	--	--	Floating
D24	NC	--	--	--	Floating
D25	GND	--	--	--	GND
D26	NC	--	--	--	Floating
D27	NC	--	--	--	Floating

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
D28	GND	--	--	--	GND
D29	NC	--	--	--	Floating
D30	NC	--	--	--	Floating
D31	NC	--	--	--	Floating
D32	NC	--	--	--	Floating
D33	NC	--	--	--	Floating
D34	NC	--	--	--	Floating
D35	GND	--	--	--	GND
D36	NC	--	--	--	Floating
D37	GND	--	--	--	GND
D38	FMC_VCC3P3	--	--	3.3V	Power
D39	GND	--	--	--	GND
D40	FMC_VCC3P3	--	--	3.3V	Power
E1	GND	--	--	--	GND
E2	7513_MCLK	Y21	2	3.3V	IIS interface MCLK
E3	NC	--	--	--	Floating
E4	GND	--	--	--	GND
E5	GND	--	--	--	GND
E6	7513_IIS0	V23	2	3.3V	IIS interface data signal
E7	NC	--	--	--	Floating
E8	GND	--	--	--	GND
E9	7513_SCLK	V19	2	3.3V	IIS interface SCLK
E10	NC	--	--	--	Floating
E11	GND	--	--	--	GND
E12	7513_LRCLK	AA22	2	3.3V	IIS interface LRCLK
E13	NC	--	--	--	Floating
E14	GND	--	--	--	GND
E15	7513_SDA	Y25	2	3.3V	I2C serial interface data

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
E16	7513_SCL	AA25	2	3.3V	I2C serial interface clock
E17	GND	--	--	--	GND
E18	7513_INT	V26	2	3.3V	Interrupt signal
E19	NC	--	--	--	Floating
E20	GND	--	--	--	GND
E21	NC	--	--	--	Floating
E22	NC	--	--	--	Floating
E23	GND	--	--	--	GND
E24	NC	--	--	--	Floating
E25	NC	--	--	--	Floating
E26	GND	--	--	--	GND
E27	NC	--	--	--	Floating
E28	NC	--	--	--	Floating
E29	GND	--	--	--	GND
E30	NC	--	--	--	Floating
E31	NC	--	--	--	Floating
E32	GND	--	--	--	GND
E33	NC	--	--	--	Floating
E34	NC	--	--	--	Floating
E35	GND	--	--	--	GND
E36	NC	--	--	--	Floating
E37	NC	--	--	--	Floating
E38	GND	--	--	--	GND
E39	NC	--	--	--	Floating
E40	GND	--	--	--	GND
F1	NC	--	--	--	Floating
F2	GND	--	--	--	GND
F3	GND	--	--	--	GND
F4	NC	--	--	--	Floating

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F5	NC	--	--	--	Floating
F6	GND	--	--	--	GND
F7	7513_VSYNC	V16	2	3.3V	Vertical synchronization signal
F8	7513_D0	V17	2	3.3V	RGB data signal
F9	GND	--	--	--	GND
F10	7513_D3	W20	2	3.3V	RGB data signal
F11	7513_D6	Y20	2	3.3V	RGB data signal
F12	GND	--	--	--	GND
F13	7513_D9	AB24	2	3.3V	RGB data signal
F14	7513_D12	AC24	2	3.3V	RGB data signal
F15	GND	--	--	--	GND
F16	7513_D15	AB26	2	3.3V	RGB data signal
F17	7513_D18	AC26	2	3.3V	RGB data signal
F18	GND	--	--	--	GND
F19	7513_D21	U25	2	3.3V	RGB data signal
F20	NC	--	--	--	Floating
F21	GND	--	--	--	GND
F22	NC	--	--	--	Floating
F23	NC	--	--	--	Floating
F24	GND	--	--	--	GND
F25	NC	--	--	--	Floating
F26	NC	--	--	--	Floating
F27	GND	--	--	--	GND
F28	NC	--	--	--	Floating
F29	NC	--	--	--	Floating
F30	GND	--	--	--	GND
F31	NC	--	--	--	Floating
F32	NC	--	--	--	Floating
F33	GND	--	--	--	GND

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F34	NC	--	--	--	Floating
F35	NC	--	--	--	Floating
F36	GND	--	--	--	GND
F37	NC	--	--	--	Floating
F38	NC	--	--	--	Floating
F39	GND	--	--	--	GND
F40	NC	--	--	--	Floating
G1	GND	--	--	--	GND
G2	NC	--	--	--	Floating
G3	NC	--	--	--	Floating
G4	GND	--	--	--	GND
G5	GND	--	--	--	GND
G6	Panel_ON	D18	5	1.8V	EDP screen test signal
G7	BL_ENABLE	C18	5	1.8V	Backlight enabled
G8	GND	--	--	--	GND
G9	NC	--	--	--	Floating
G10	NC	--	--	--	Floating
G11	GND	--	--	--	GND
G12	BL_PWM_OUT	A17	5	1.8V	PWM backlight output
G13	NC	--	--	--	Floating
G14	GND	--	--	--	GND
G15	EDPTX_AUX_CH_P_1	E16	5	1.8V	Auxiliary channel
G16	EDPTX_AUX_CH_N_1	D16	5	1.8V	Auxiliary channel
G17	GND	--	--	--	GND
G18	NC	--	--	--	Floating
G19	NC	--	--	--	Floating
G20	GND	--	--	--	GND

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
G21	NC	--	--	--	Floating
G22	NC	--	--	--	Floating
G23	GND	--	--	--	GND
G24	NC	--	--	--	Floating
G25	NC	--	--	--	Floating
G26	GND	--	--	--	GND
G27	NC	--	--	--	Floating
G28	NC	--	--	--	Floating
G29	GND	--	--	--	GND
G30	NC	--	--	--	Floating
G31	NC	--	--	--	Floating
G32	GND	--	--	--	GND
G33	NC	--	--	--	Floating
G34	NC	--	--	--	Floating
G35	GND	--	--	--	GND
G36	NC	--	--	--	Floating
G37	NC	--	--	--	Floating
G38	GND	--	--	--	GND
G39	NC	--	--	--	Floating
G40	GND	--	--	--	GND
H1	NC	--	--	--	Floating
H2	NC	--	--	--	Floating
H3	GND	--	--	--	GND
H4	NC	--	--	--	Floating
H5	NC	--	--	--	Floating
H6	GND	--	--	--	GND
H7	NC	--	--	--	Floating
H8	NC	--	--	--	Floating
H9	GND	--	--	--	GND
H10	NC	--	--	--	Floating

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
H11	NC	--	--	--	Floating
H12	GND	--	--	--	GND
H13	NC	--	--	--	Floating
H14	NC	--	--	--	Floating
H15	GND	--	--	--	GND
H16	NC	--	--	--	Floating
H17	NC	--	--	--	Floating
H18	GND	--	--	--	GND
H19	NC	--	--	--	Floating
H20	NC	--	--	--	Floating
H21	GND	--	--	--	GND
H22	NC	--	--	--	Floating
H23	NC	--	--	--	Floating
H24	GND	--	--	--	GND
H25	NC	--	--	--	Floating
H26	NC	--	--	--	Floating
H27	GND	--	--	--	GND
H28	NC	--	--	--	Floating
H29	NC	--	--	--	Floating
H30	GND	--	--	--	GND
H31	NC	--	--	--	Floating
H32	NC	--	--	--	Floating
H33	GND	--	--	--	GND
H34	NC	--	--	--	Floating
H35	NC	--	--	--	Floating
H36	GND	--	--	--	GND
H37	NC	--	--	--	Floating
H38	NC	--	--	--	Floating
H39	GND	--	--	--	GND
H40	NC	--	--	--	Floating

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
J1	GND	--	--	--	GND
J2	NC	--	--	--	Floating
J3	NC	--	--	--	Floating
J4	GND	--	--	--	GND
J5	GND	--	--	--	GND
J6	7513_HSYNC	U14	2	3.3V	Horizontal synchronization signal
J7	7513_D1	V14	2	3.3V	RGB data signal
J8	GND	--	--	--	GND
J9	7513_D4	V18	2	3.3V	RGB data signal
J10	7513_D7	W18	2	3.3V	RGB data signal
J11	GND	--	--	--	GND
J12	7513_D10	U22	2	3.3V	RGB data signal
J13	7513_D13	V22	2	3.3V	RGB data signal
J14	GND	--	--	--	GND
J15	7513_D16	AA24	2	3.3V	RGB data signal
J16	7513_D19	AB25	2	3.3V	RGB data signal
J17	GND	--	--	--	GND
J18	7513_D22	W25	2	3.3V	RGB data signal
J19	NC	--	--	--	Floating
J20	GND	--	--	--	GND
J21	NC	--	--	--	Floating
J22	NC	--	--	--	Floating
J23	GND	--	--	--	GND
J24	NC	--	--	--	Floating
J25	NC	--	--	--	Floating
J26	GND	--	--	--	GND
J27	NC	--	--	--	Floating
J28	NC	--	--	--	Floating
J29	GND	--	--	--	GND

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
J30	NC	--	--	--	Floating
J31	NC	--	--	--	Floating
J32	GND	--	--	--	GND
J33	NC	--	--	--	Floating
J34	NC	--	--	--	Floating
J35	GND	--	--	--	GND
J36	NC	--	--	--	Floating
J37	NC	--	--	--	Floating
J38	GND	--	--	--	GND
J39	NC	--	--	--	Floating
J40	GND	--	--	--	GND
K1	NC	--	--	--	Floating
K2	GND	--	--	--	GND
K3	GND	--	--	--	GND
K4	NC	--	--	--	Floating
K5	NC	--	--	--	Floating
K6	GND	--	--	--	GND
K7	7513_DE	T14	2	3.3V	Data enable signal
K8	7513_D2	T15	2	3.3V	RGB data signal
K9	GND	--	--	--	GND
K10	7513_D5	U15	2	3.3V	RGB data signal
K11	7513_D8	U16	2	3.3V	RGB data signal
K12	GND	--	--	--	GND
K13	7513_D11	T20	2	3.3V	RGB data signal
K14	7513_D14	U20	2	3.3V	RGB data signal
K15	GND	--	--	--	GND
K16	7513_CLK	K21	4	3.3V	Video output clock
K17	NC	--	--	--	Floating
K18	GND	--	--	--	GND
K19	7513_D17	T17	2	3.3V	RGB data signal

RE1 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
K20	7513_D20	T18	2	3.3V	RGB data signal
K21	GND	--	--	--	GND
K22	7513_D23	T19	2	3.3V	RGB data signal
K23	NC	--	--	--	RGB data signal
K24	GND	--	--	--	GND
K25	NC	--	--	--	Floating
K26	NC	--	--	--	Floating
K27	GND	--	--	--	GND
K28	NC	--	--	--	Floating
K29	NC	--	--	--	Floating
K30	GND	--	--	--	GND
K31	NC	--	--	--	Floating
K32	NC	--	--	--	Floating
K33	GND	--	--	--	GND
K34	NC	--	--	--	Floating
K35	NC	--	--	--	Floating
K36	GND	--	--	--	GND
K37	NC	--	--	--	Floating
K38	NC	--	--	--	Floating
K39	GND	--	--	--	GND
K40	NC	--	--	--	Floating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PROGRAMMING FOR THE FUTURE