

Title		
DK_MOTOR_GW5AS-EV25UG256C211		
Size	Document Number	Rev
A3	0	1.1
Date:	Tuesday, September 10, 2024	Sheet 1 of 10

5

4

3

2

1

D

D

C

C

B

B

A

A

SCHEMATIC	CONTENT	PAGE
BLOCK DIAGRAM	BLOCK DIAGRAM	01
COVER PAGE	COVER PAGE	02
POWER	DC5V/DC3.3V,DC5V/DC1.2V	03
FPGA	FPGA,SPI FLASH,EEPROM,OSC,AT-Link	04-06
ETHERNET PHY	PHY1,PHY2	07
FOC1	RS422,RS485,PWM	08
FOC2	RS422,RS485,PWM	09
USB-LVDS	FPGA DOWNLOAD,MCU USB,LVDS	10

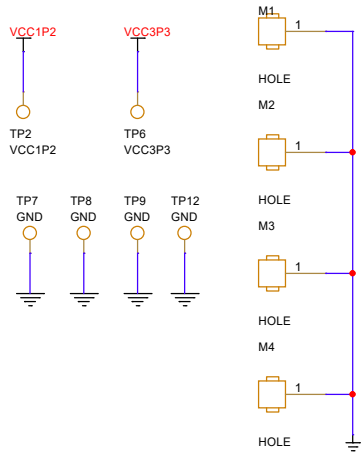
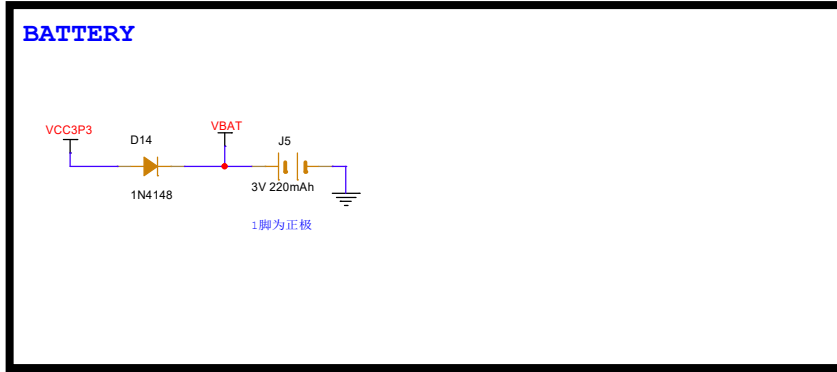
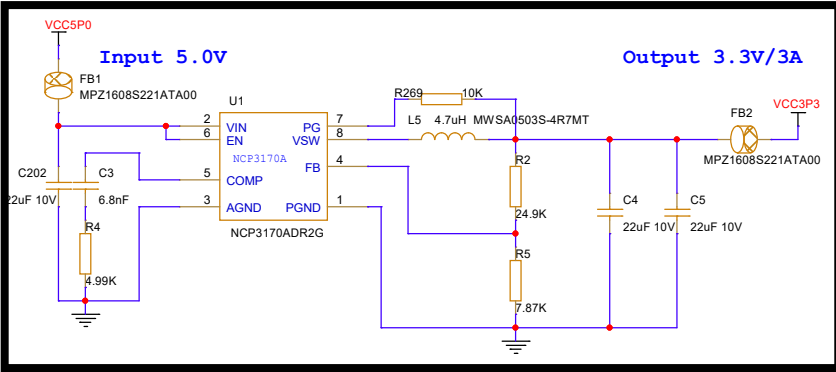
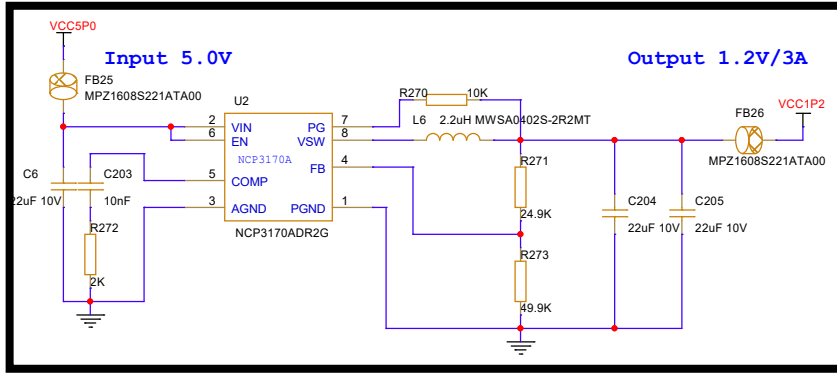
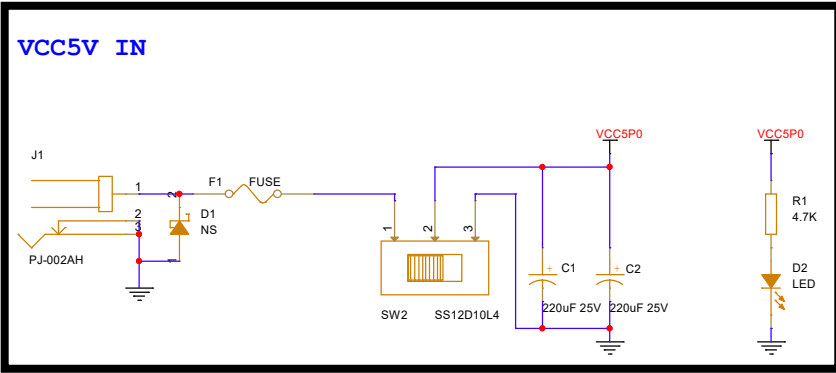
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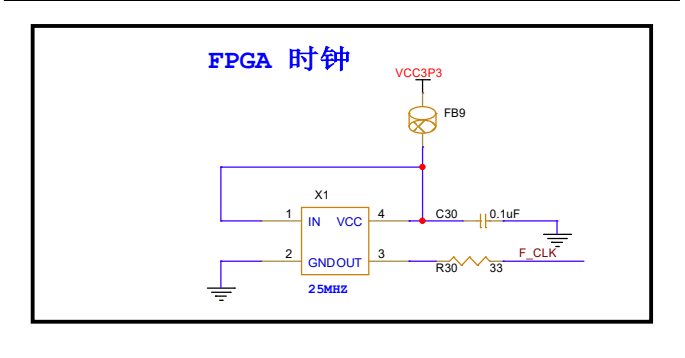
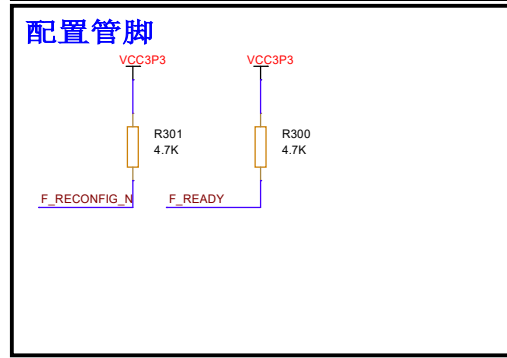
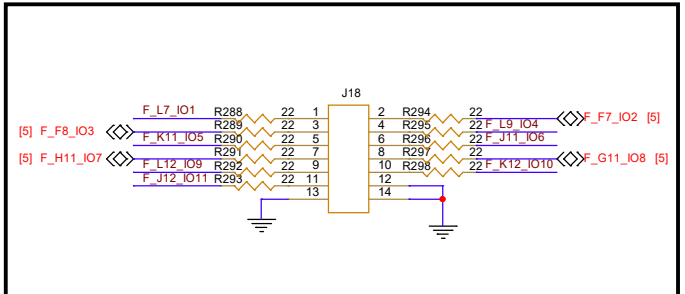
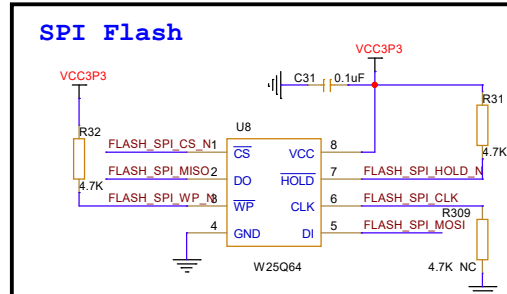
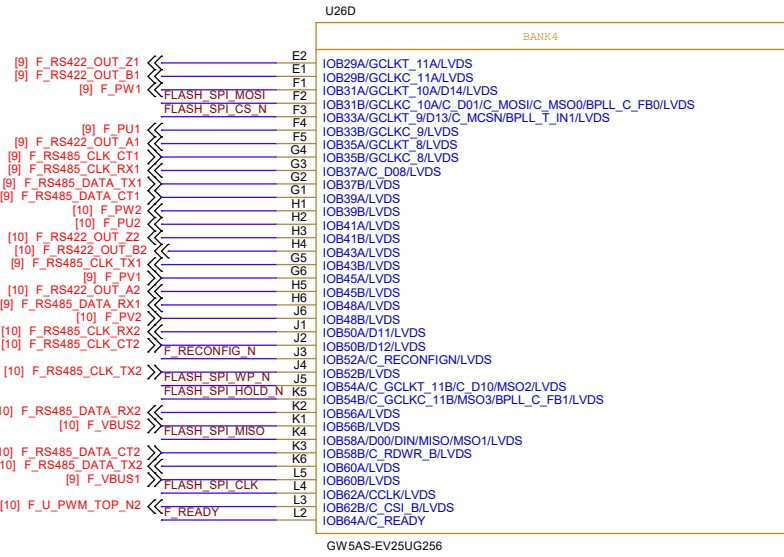
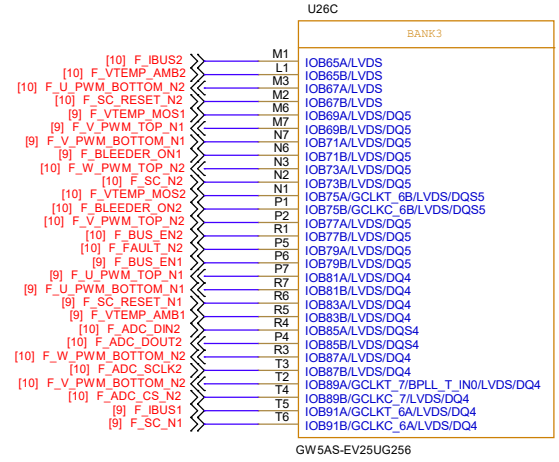
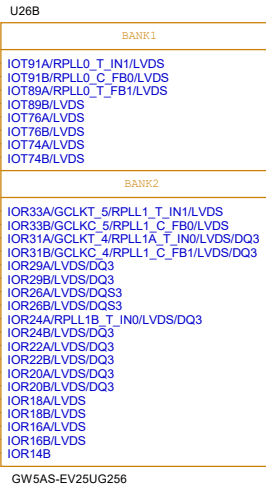
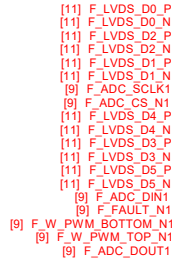
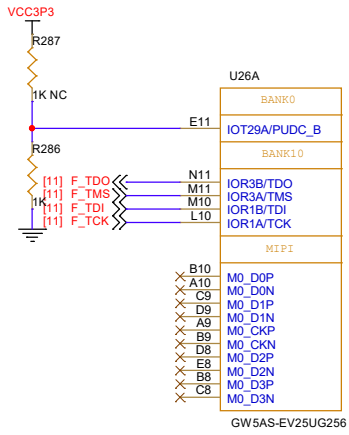
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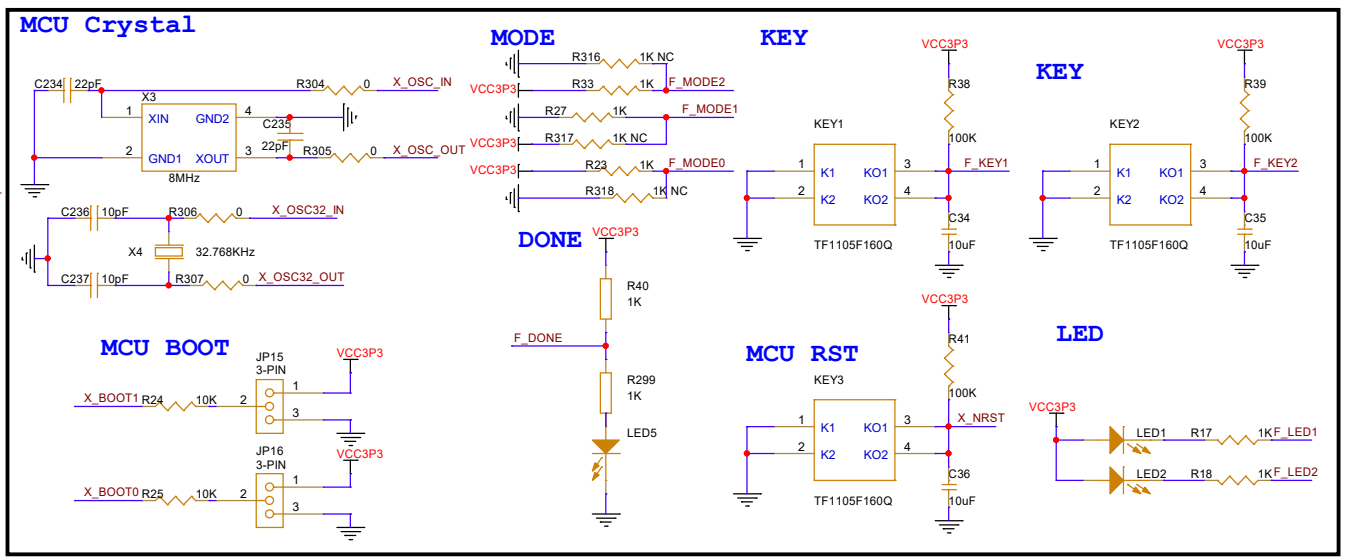
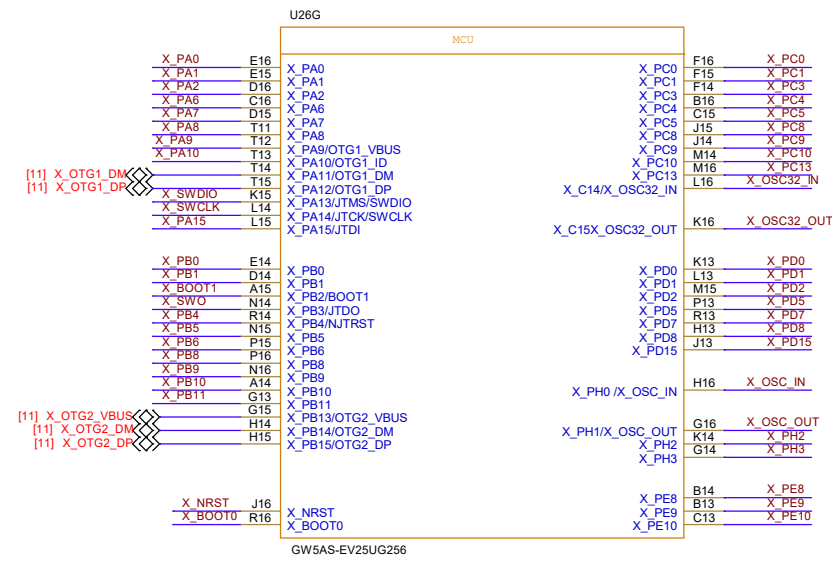
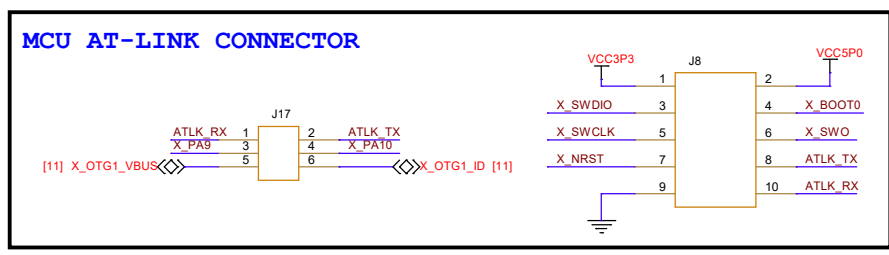
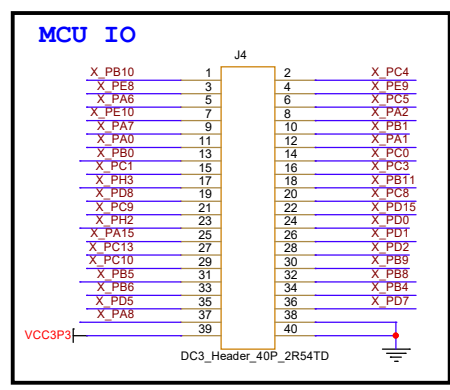
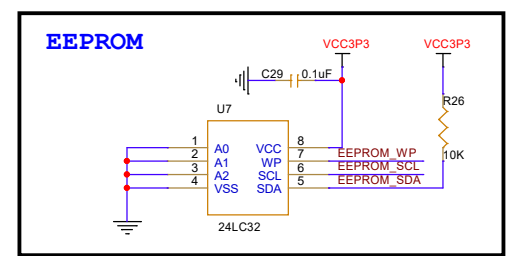
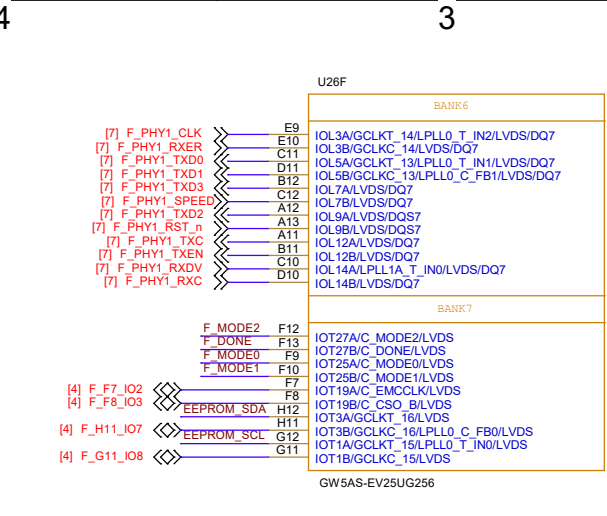
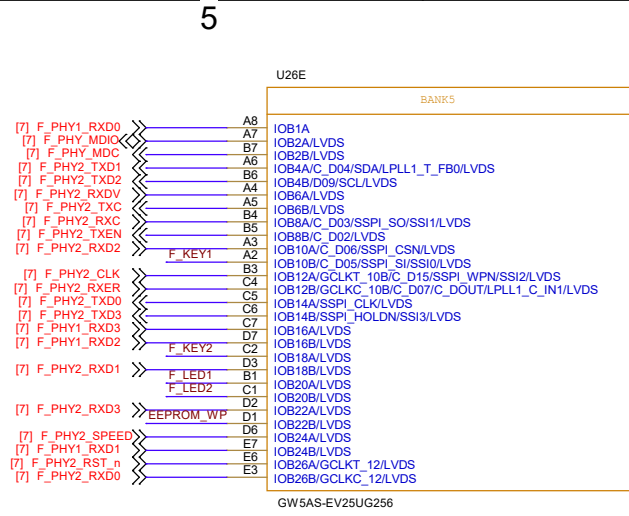
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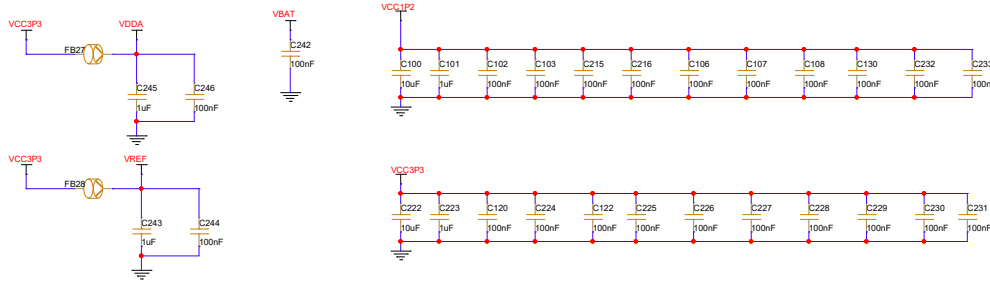
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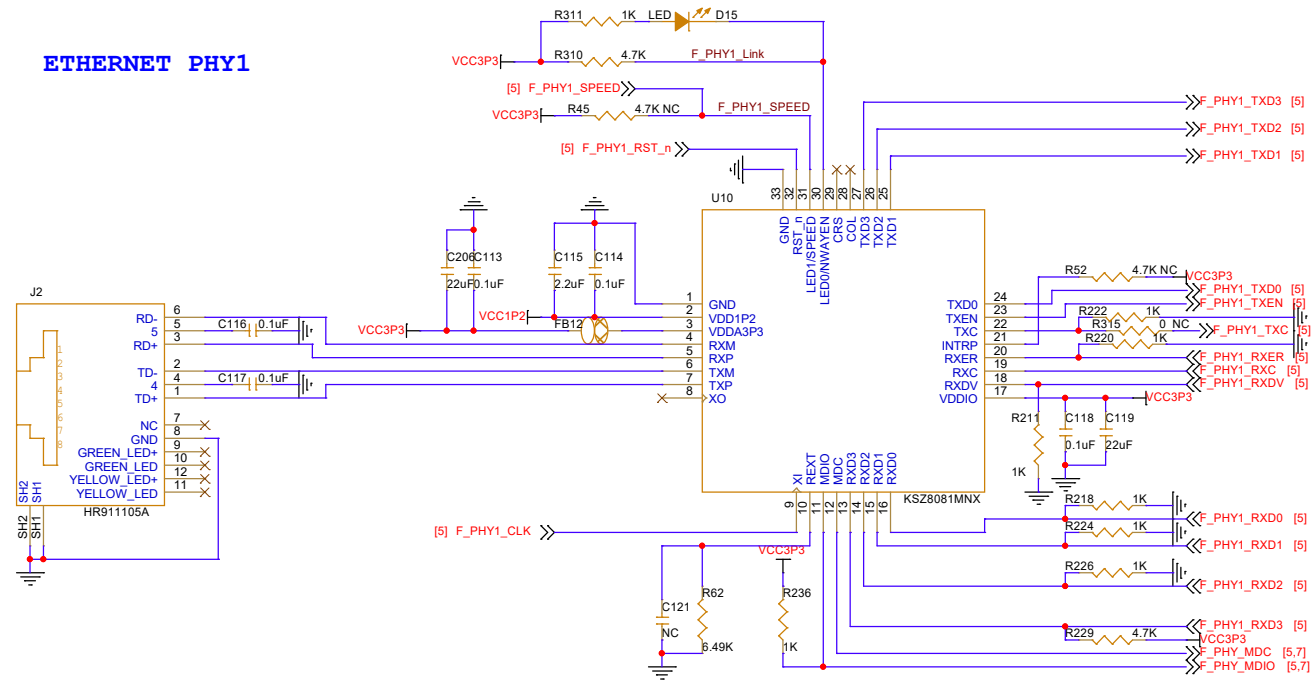
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DK_MOTOR_GW5AS-EV25UG256C211		
Size	Document Number	Rev
A3	POWER	1.1
Date:	Tuesday, September 10, 2024	Sheet 3 of 10



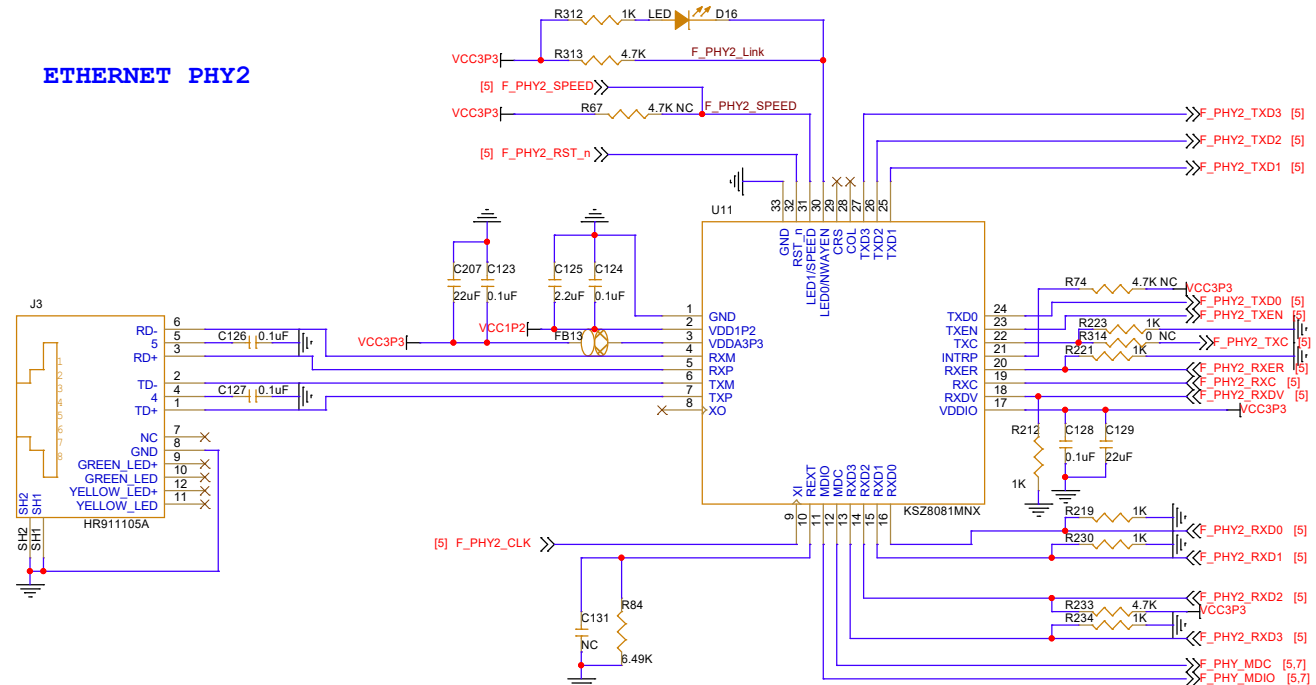




ETHERNET PHY1

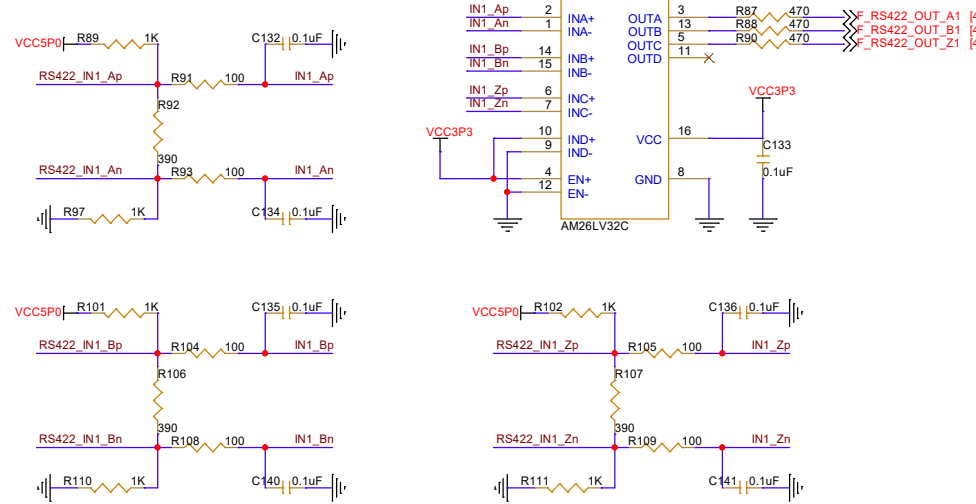


ETHERNET PHY2

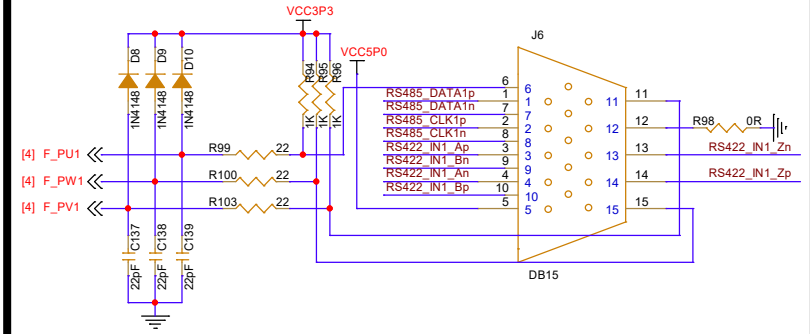


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DK_MOTOR_GW5AS-EV25UG256C211		
Size	Document Number	Rev
A3	ETHERNET PHY	1.1
Date:	Tuesday, September 10, 2024	Sheet 7 of 10

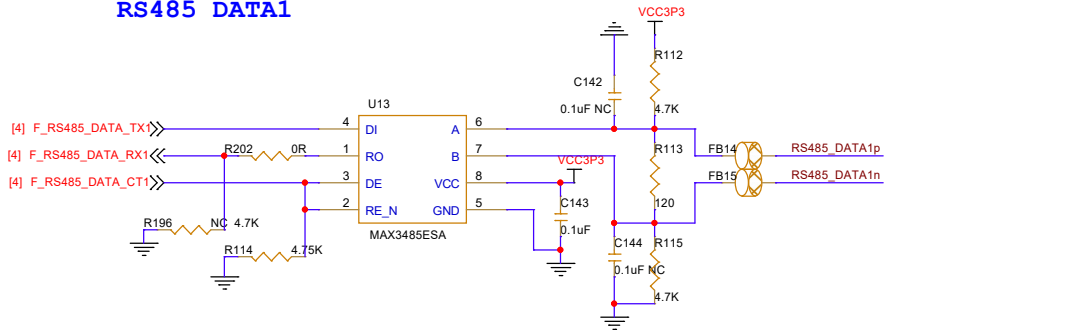
RS422 1



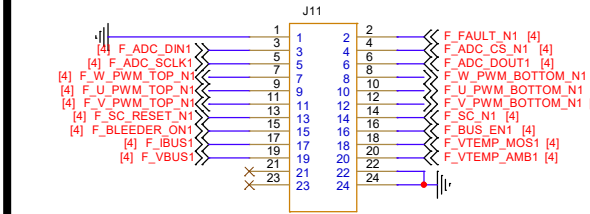
MOTOR1



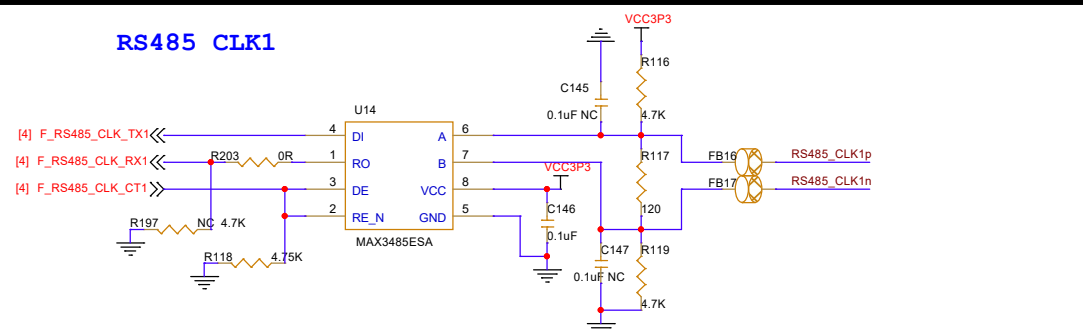
RS485 DATA1



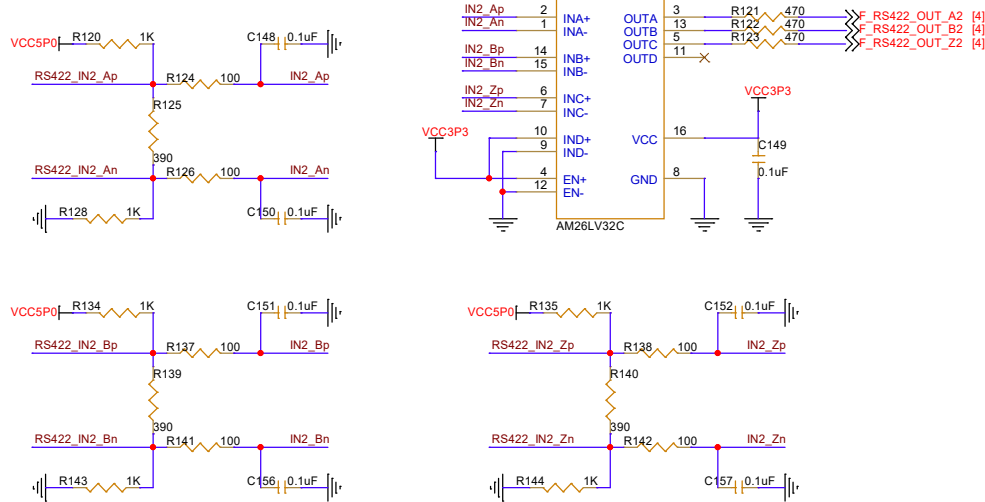
PWM1



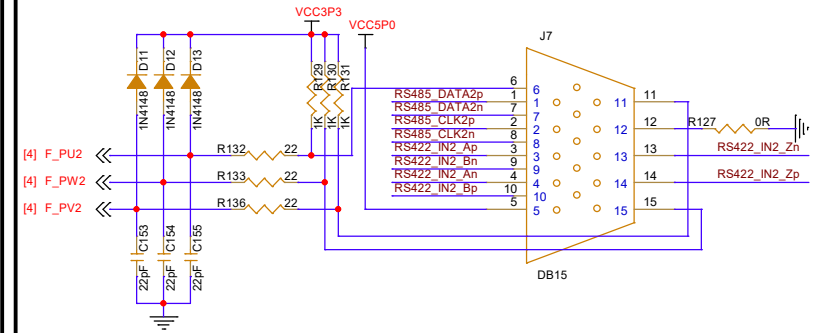
RS485 CLK1



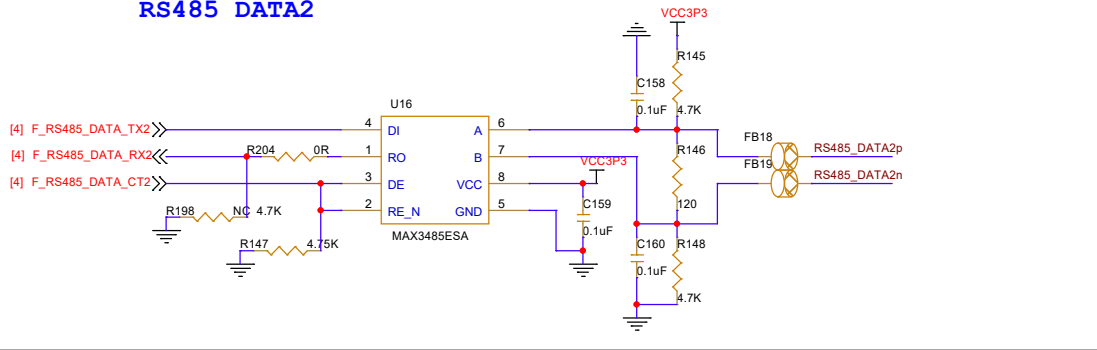
RS422 2



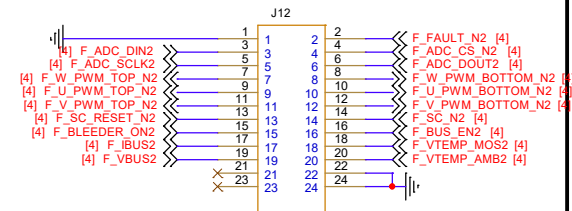
MOTOR2



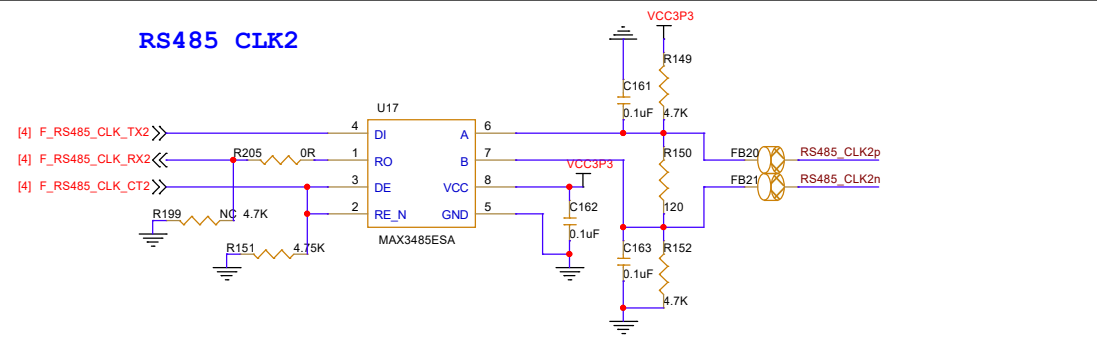
RS485 DATA2



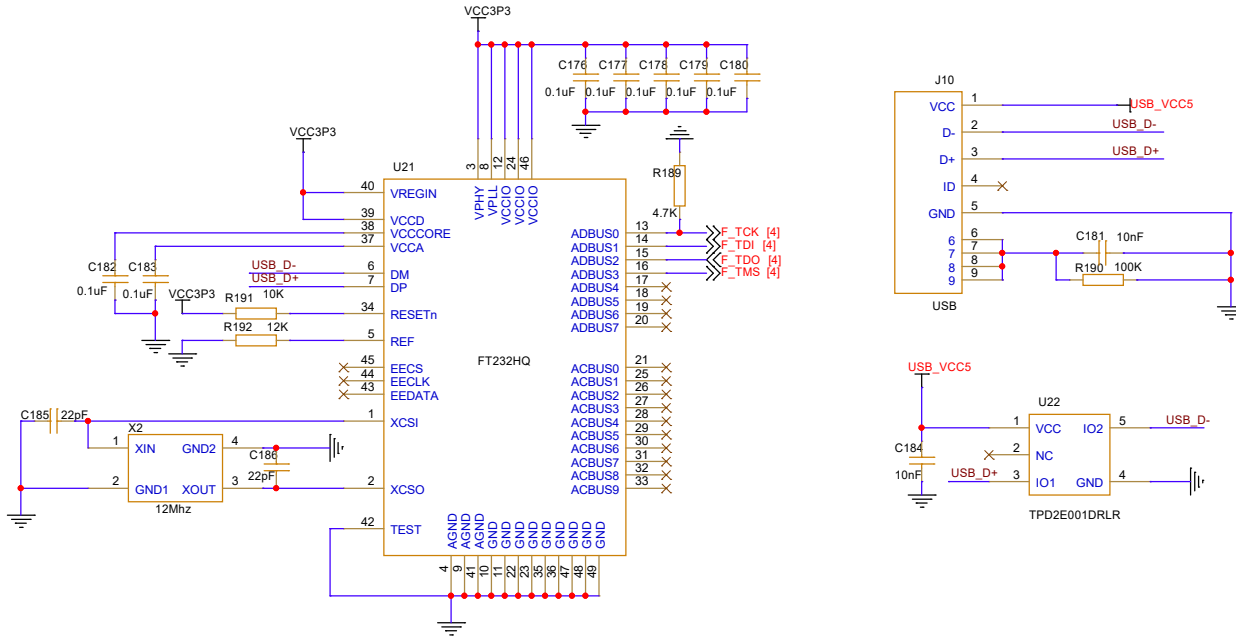
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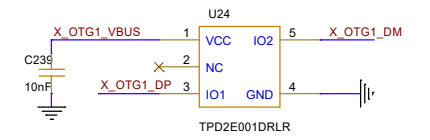
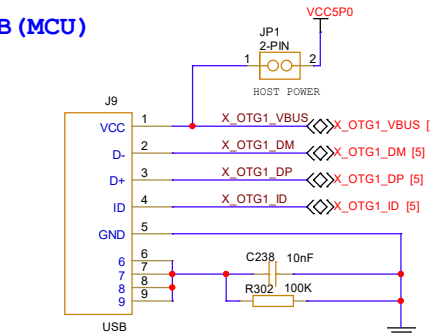
RS485 CLK2



USB to JTAG (FPGA)



USB (MCU)



LVDS

