DK_Motor_GW5AS-EV25UG256C2I1_V1.1

User Guide

DBUG422-1.0.2E, 02/14/2025

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Revision History

Date	Version	Description
07/19/2024	1.0E	Initial version published.
09/13/2024	1.0.1E	The development board name updated.
02/14/2025	1.0.2E	The description of “F_PHY1_RST_n” and “F_PHY2_RST_n” signals in “Table 3-3 Pin Distribution of Ethernet Interface 1” and “Table 3-4 Pin Distribution of Ethernet Interface 2” updated.

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1 About This Guide

1.1 Purpose

The DK_Motor_GW5AS-EV25UG256C2I1_V1.1 development board (hereinafter referred to as “the development board”) user guide consists of following three parts:

- A brief introduction to the features of the development board
- An introduction to the development board system architecture and hardware resources
- An introduction to the hardware circuits, functions and pin distribution

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- DS1103, Arora V 25K FPGA Products Data Sheet
- UG1115, GW5AS-25 Pinout
- UG1106, GW5AS series of FPGA Products Package and Pinout User Guide
- UG714, Arora V 25K FPGA Products Programming and Configuration User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable Input/Output
JTAG	Joint Test Action Group
LVDS	Low-Voltage Differential Signaling
MCU	Microcontroller Unit
OTG	USB On-The-Go
PWM	Pulse-width Modulation

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

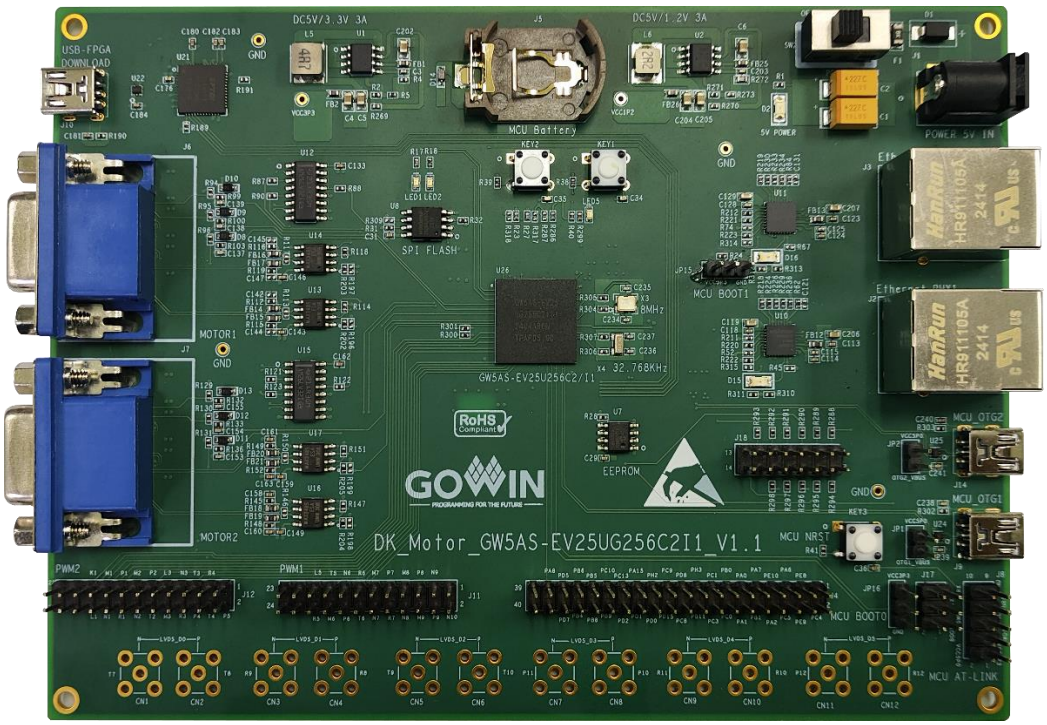
Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Development Board Introduction

2.1 Overview

Figure 2-1 DK_Motor_GW5AS-EV25UG256C2I1_V1.1 Development Board



Gowin GW5AS-25 devices are the 5 series products of Arora family, which integrate the latest generation of embedded ARM core processor Cortex-M4, include abundant internal resources, high-performance DSP with a new architecture that supports AI operations, high-speed LVDS interface and abundant BSRAM resources. At the same time, it provides a variety of packages and is suitable for applications such as low power, high performance and compatibility design.

The DK_Motor_GW5AS-EV25UG256C2I1_V1.1 development board

integrates 2 Ethernet interfaces to support 10M/100M industrial Ethernet communication. A wide range of external interfaces are designed, including LVDS interfaces, PWM interfaces, motor communication interfaces, GPIO interfaces, MCU download interfaces, FPGA download interfaces, etc.

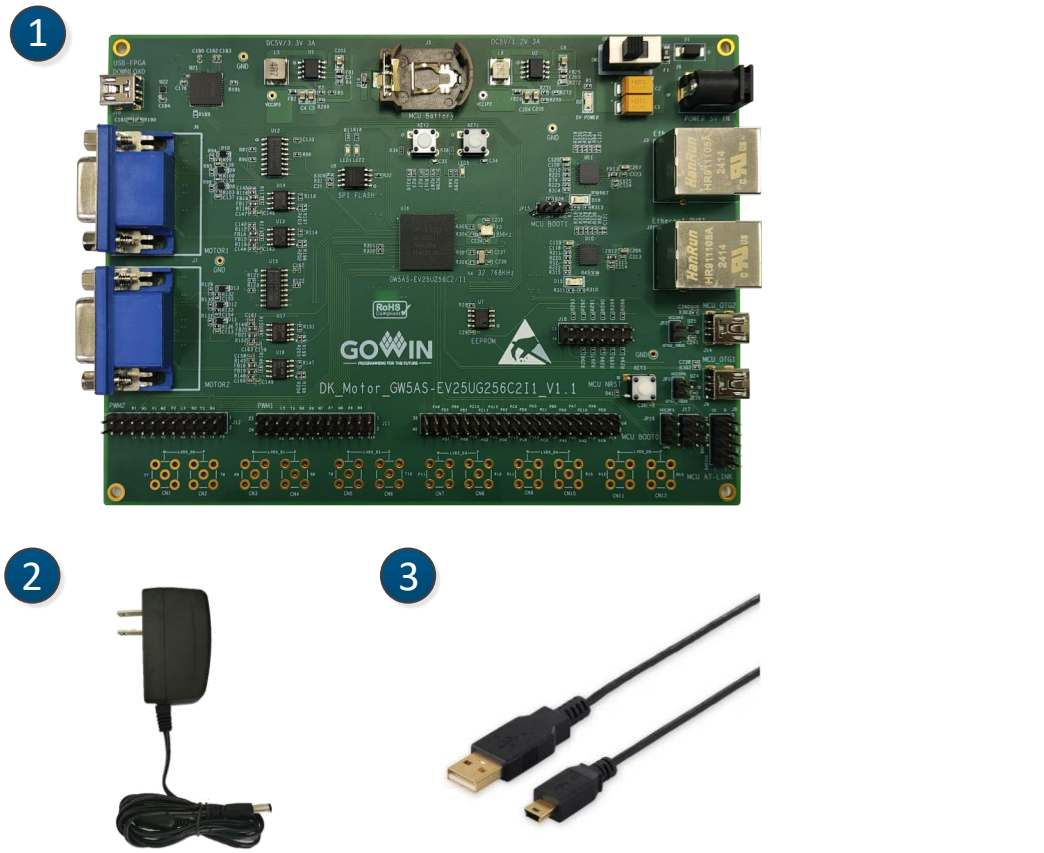
The development board adopts Gowin GW5AS-EV25UG256 FPGA device. For the internal resources of the chip, see *DS1103, Arora V 25K FPGA Products Data Sheet*.

2.2 A Development Board Kit

The development board kit includes the following items:

1. DK_Motor_GW5AS-EV25UG256C2I1_V1.1 development board
2. 5V power (Input: AC 100-240V~50/60Hz 0.5A, output: DC5V 2A)
3. Mini USB-B Cable

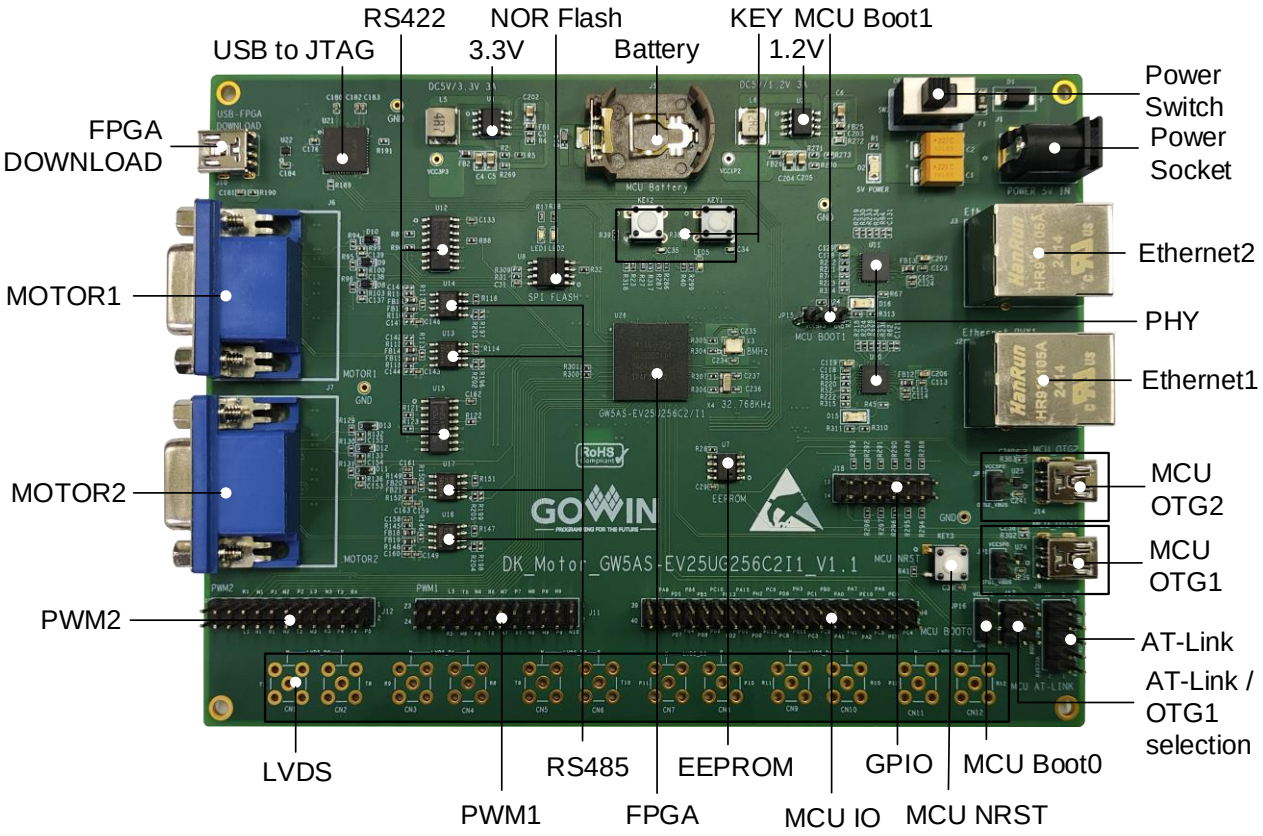
Figure 2-2 A Development Board Kit



① DK_Motor_GW5AS-EV25UG256C2I1_V1.1 development board
② 5V power supply
③ Mini USB-B Cable

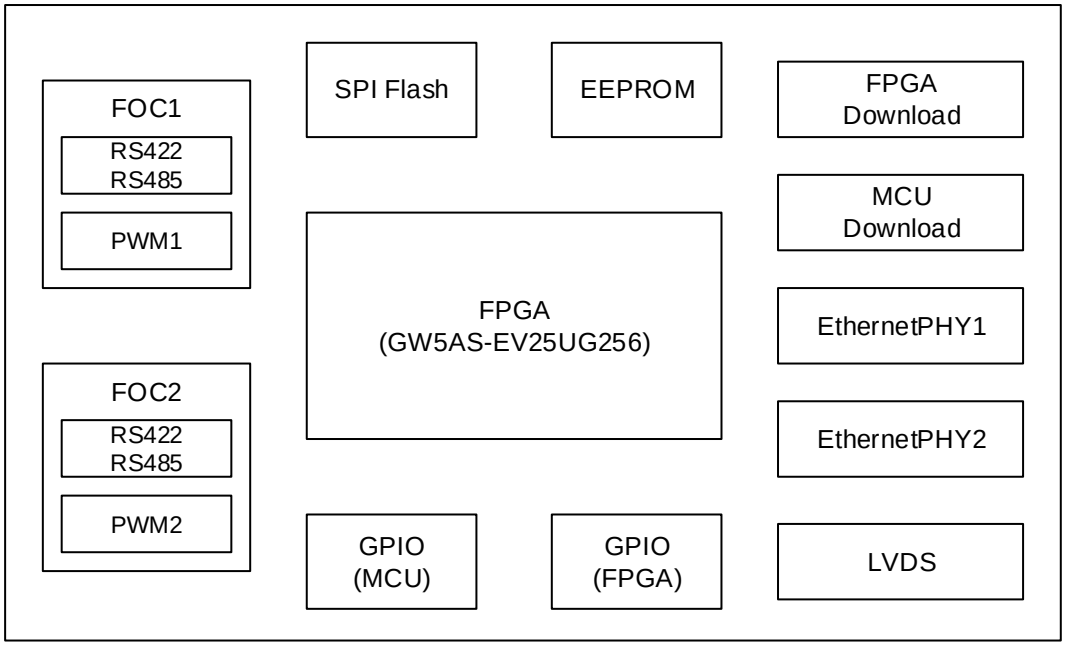
2.3 PCB Components

Figure 2-3 PCB Components



2.4 System Block Diagram

Figure 2-4 System Block Diagram



2.5 Features

The key features are as follows:

- FPGA Device
  - Gowin GW5AS-EV25UG256 FPGA
  - Max. user I/O: 144
- Download and Boot
  - Integrate USB download circuit on the board, download through Mini USB-B interface
  - External SPI Flash Boot
  - The DONE light is on after loading
- Power
  - External DC5V/2A Power
  - The Power light is on after power on
  - The development board can generate 3.3V, 1.2V power
- System Clock
  - 25MHz clock
- Memory Device
  - 32Kbit EEPROM
  - 64Mbit NOR SPI Flash
- LVDS Interface
  - 6-pair LVDS differential pairs
- Ethernet Interface
  - 2-lane Ethernet interfaces
  - MII interface, supporting 10BASE-T and 100BASE-TX
  - RJ45 connector with internal network transformer internally
- PWM Interface
  - 2-lane PWM interfaces for transmitting PWM signals
- Motor control interface
  - 2-lane motor control interfaces
  - Each lane motor control interface contains 3-lane RS422 differential signals, 1-lane RS485 differential data signal, 1-lane differential clock signal, and 3 GPIOs.
- MCU-related interface
  - 2-lane OTG interfaces with mini USB-B port with electrostatic protection
  - 1-lane AT-LINK interface
  - 1-lane MCU reset key
  - 37 MCU IOs powered by 3.3V

  - 1-lane 8MHz differential clock
  - 1-lane 32.768KHz differential clock
- AT-Link/OTG1 Selection Interface
  - 1-lane AT-Link/OTG1 selection interface
  - Select AT-Link interface or OTG1 interface via jumper
- Key & LED
  - 2 keys
  - 2 LEDs
- GPIO
  - 11 GPIOs with 3.3V

3 Development Board Circuit

3.1 FPGA

Overview

For the resources of GW5AS series of FPGA Products, refer to *DS1103, Arora V 25K FPGA Products Data Sheet*.

I/O BANK Introduction

For the I/O BANK, package, and pinout information, see *UG1106, GW5AS series of FPGA Products Package and Pinout User Guide* for more details.

3.2 Power Supply

3.2.1 Introduction

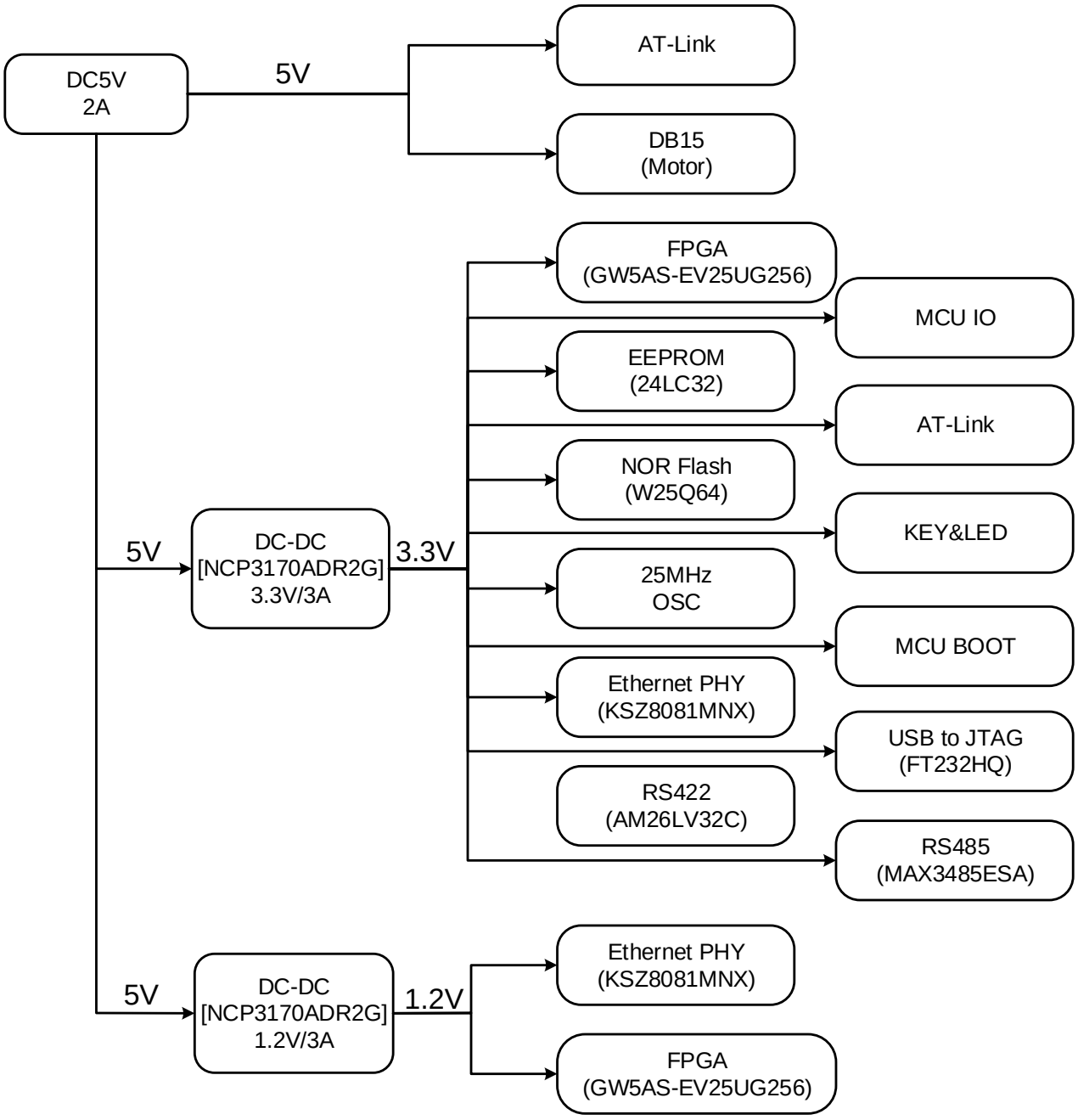
The development board needs to be powered by a 5V power adapter.

The input parameter of the adapter is AC 100-240V~50/60MHz 0.5A, and the output parameter is DC 5V 2A.

The input 5V power generates 3.3V and 1.2V power supply through the power chip on the development board to meet the power requirements of the development board.

3.2.2 Power Distribution

Figure 3-1 Power Distribution Diagram



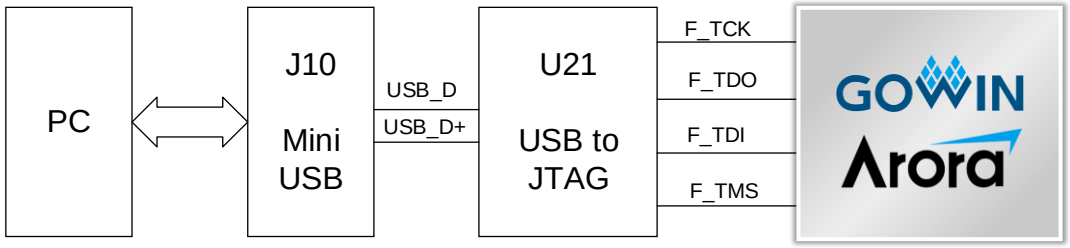
3.3 Download Module

3.3.1 Introduction

The development board has a Mini USB-B download port (J10) designed to program the programs to external SPI FLASH or download them to SRAM.

The download connection diagram is show in Figure 3-2.

Figure 3-2 Connection Diagram of Download



3.3.2 Pin Distribution

Table 3-1 JTAG Pin Distribution

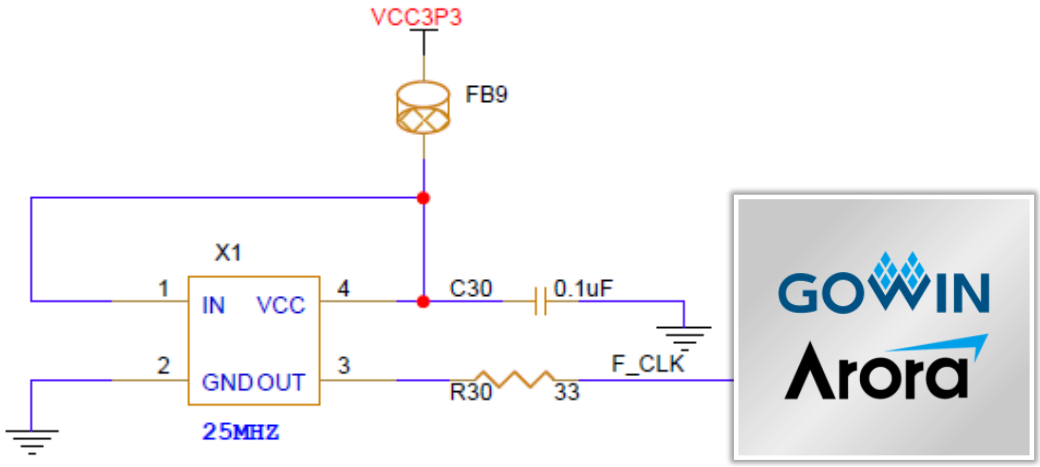
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_TCK	L10	10	3.3V	JTAG signals
F_TDO	N11	10	3.3V	
F_TDI	M10	10	3.3V	
F_TMS	M11	10	3.3V	

3.4 Clock

3.4.1 Introduction

The FPGA clock source is introduced by a 25MHz single-ended clock signal. The clock pin distribution is as shown in Figure 3-3.

Figure 3-3 Clock Connection Diagram



3.4.2 Pin Distribution

Table 3-2 Clock Pin Distribution

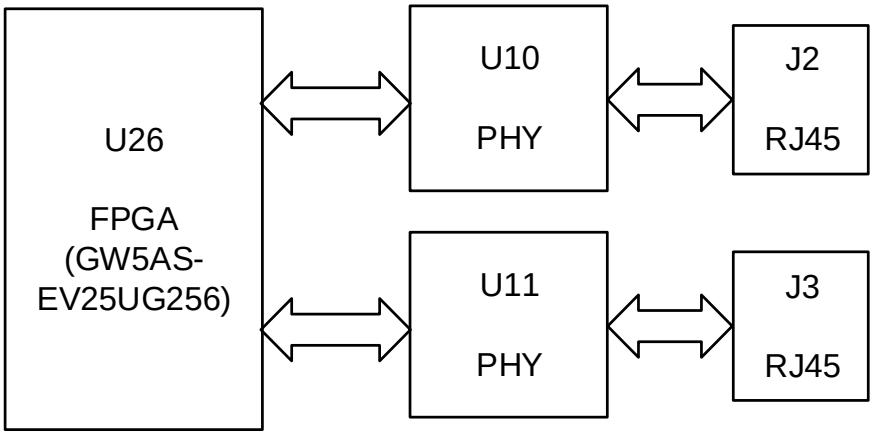
Signal Name	FPGA (U1) Pin No.	BANK	I/O Level	Description
F_CLK	L8	1	3.3V	Frequency 25MHz

3.5 Ethernet Interface

3.5.1 Introduction

The development board provides 2-lane Ethernet interfaces, supporting MII (10BASE-T/100BASE-TX) interfaces. Use the RJ45 connector with internal network transformer. The connection diagram is shown in Figure 3-4.

Figure 3-4 Ethernet Interface Connection Diagram



3.5.2 Pin Distribution

Table 3-3 Pin Distribution of Ethernet Interface 1

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_PHY1_TXD0	C11	6	3.3V	MII transmit data
F_PHY1_TXD1	D11	6	3.3V	MII transmit data
F_PHY1_TXD2	A12	6	3.3V	MII transmit data
F_PHY1_TXD3	B12	6	3.3V	MII transmit data
F_PHY1_TXC	A11	6	3.3V	MII transmit clock
F_PHY1_TXEN	B11	6	3.3V	MII transmit error
F_PHY1_RXD0	A8	5	3.3V	MII receive data
F_PHY1_RXD1	E7	5	3.3V	MII receive data
F_PHY1_RXD2	D7	5	3.3V	MII receive data
F_PHY1_RXD3	C7	5	3.3V	MII receive data
F_PHY1_RXC	D10	6	3.3V	MII receive clock
F_PHY1_RXER	E10	6	3.3V	MII receiving error
F_PHY1_RXDV	C10	6	3.3V	MII receive data, valid
F_PHY1_CLK	E9	6	3.3V	Clock input
F_PHY_MDIO	A7	5	3.3V	MII data input/output
F_PHY_MDC	B7	5	3.3V	MII clock input
F_PHY1_SPEED	C12	6	3.3V	MII rate
F_PHY1_RST_n	A13	6	3.3V	Reset signal

Table 3-4 Pin Distribution of Ethernet Interface 2

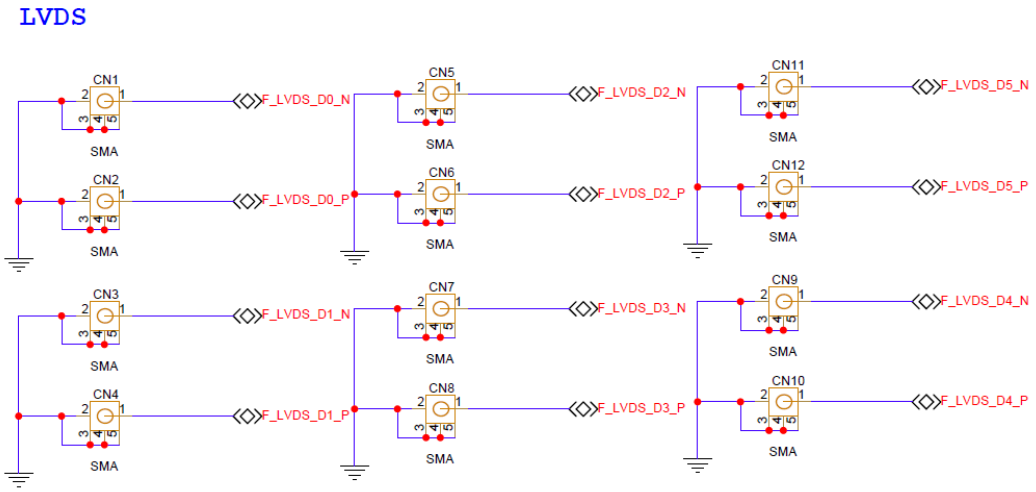
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_PHY2_TXD0	C5	5	3.3V	MII transmit data
F_PHY2_TXD1	A6	5	3.3V	MII transmit data
F_PHY2_TXD2	B6	5	3.3V	MII transmit data
F_PHY2_TXD3	C6	5	3.3V	MII transmit data
F_PHY2_TXC	A5	5	3.3V	MII transmit clock
F_PHY2_TXEN	B5	5	3.3V	MII transmit error
F_PHY2_RXD0	E3	5	3.3V	MII receive data
F_PHY2_RXD1	D3	5	3.3V	MII receive data
F_PHY2_RXD2	A3	5	3.3V	MII receive data
F_PHY2_RXD3	D2	5	3.3V	MII receive data
F_PHY2_RXC	B4	5	3.3V	MII receive clock
F_PHY2_RXER	C4	5	3.3V	MII receiving error
F_PHY2_RXDV	A4	5	3.3V	MII receive data, valid
F_PHY2_CLK	E9	6	3.3V	Clock input
F_PHY_MDIO	A7	5	3.3V	MII data input/output
F_PHY_MDC	B7	5	3.3V	MII clock input
F_PHY2_SPEED	D6	5	3.3V	MII rate
F_PHY2_RST_n	E6	5	3.3V	Reset signal

3.6 LVDS Interface

3.6.1 Introduction

The LVDS interfaces consist of 12 SMA connectors including six pairs of differential signals. The interface schematic is as shown in Figure 3-5.

Figure 3-5 Schematic of LVDS Interfaces



3.6.2 Pin Distribution

Table 3-5 Pin Distribution of LVDS Interfaces

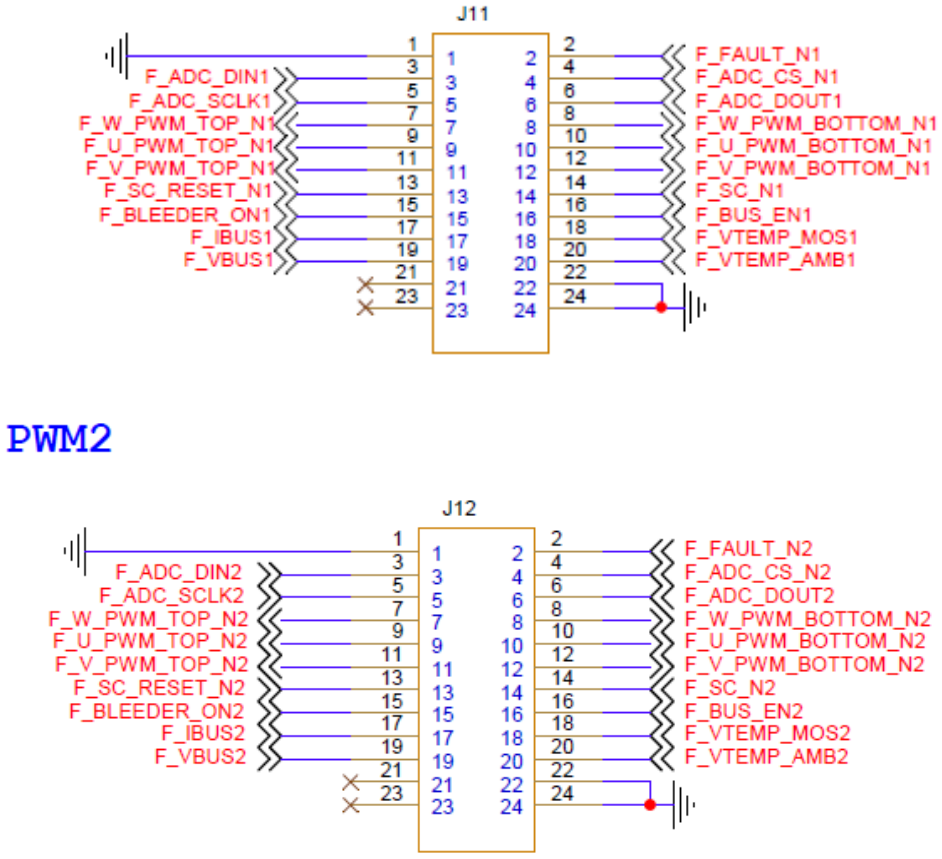
Device Number	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
CN1	F_LVDS_D0_N	T7	2	3.3V	LVDS differential signal 0-
CN2	F_LVDS_D0_P	T8	2	3.3V	LVDS differential signal 0+
CN3	F_LVDS_D1_N	R9	2	3.3V	LVDS differential signal 1-
CN4	F_LVDS_D1_P	R8	2	3.3V	LVDS differential signal 1+
CN5	F_LVDS_D2_N	T9	2	3.3V	LVDS differential signal 2-
CN6	F_LVDS_D2_P	T10	2	3.3V	LVDS differential signal 2+
CN7	F_LVDS_D3_N	P11	2	3.3V	LVDS differential signal 3-
CN8	F_LVDS_D3_P	P10	2	3.3V	LVDS differential signal 3+
CN9	F_LVDS_D4_N	R11	2	3.3V	LVDS differential signal 4-
CN10	F_LVDS_D4_P	R10	2	3.3V	LVDS differential signal 4+
CN11	F_LVDS_D5_N	P12	2	3.3V	LVDS differential signal 5-
CN12	F_LVDS_D5_P	R12	2	3.3V	LVDS differential signal 5+

3.7 PWM Interface

3.7.1 Introduction

There are 2-lane PWM interfaces on the development board. These pins can also be used as GPIOs. The PWM interface schematic is as shown in Figure 3-6.

Figure 3-6 Schematic of PWM Interfaces



3.7.2 Pin Distribution

Table 3-6 J11 Pin Distribution for PWM Interface 1

J11 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	GND	-	-	-	GND
2	F_FAULT_N1	N10	2	3.3V	Reserved IO
3	F_ADC_DIN1	N9	2	3.3V	ADC data input
4	F_ADC_CS_N1	P9	2	3.3V	ADC enable signal
5	F_ADC_SCLK1	P8	2	3.3V	ADC clock signal
6	F_ADC_DOUT1	M9	2	3.3V	ADC data output
7	F_W_PWM_TOP_N1	M8	2	3.3V	Phase W PWM upper leg control signal
8	F_W_PWM_BOTTOM_N1	N8	2	3.3V	Phase W PWM upper leg control signal
9	F_U_PWM_TOP_N1	P7	3	3.3V	Phase U PWM upper leg control signal
10	F_U_PWM_BOTTOM_N1	R7	3	3.3V	Phase U PWM upper leg control signal
11	F_V_PWM_TOP_N1	M7	3	3.3V	Phase V PWM upper leg control signal
12	F_V_PWM_BOTTOM_N1	N7	3	3.3V	Phase V PWM upper leg control signal
13	F_SC_RESET_N1	R6	3	3.3V	Reserved IO
14	F_SC_N1	T6	3	3.3V	Reserved IO
15	F_BLEEDER_ON1	N6	3	3.3V	Reserved IO
16	F_BUS_EN1	P6	3	3.3V	Reserved IO
17	F_IBUS1	T5	3	3.3V	Reserved IO
18	F_VTEMP_MOS1	M6	3	3.3V	Reserved IO
19	F_VBUS1	L5	4	3.3V	Reserved IO
20	F_VTEMP_AMB1	R5	3	3.3V	Reserved IO
21	NC	-	-	-	Floating
22	GND	-	-	-	GND
23	NC	-	-	-	Floating

J11 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
24	GND	-	-	-	GND

Table 3-7 J12 Pin Distribution for PWM Interface 2

J12 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	GND	-	-	-	GND
2	F_FAULT_N2	P5	3	3.3V	Reserved IO
3	F_ADC_DIN2	R4	3	3.3V	ADC data input
4	F_ADC_CS_N2	T4	3	3.3V	ADC enable signal
5	F_ADC_SCLK2	T3	3	3.3V	ADC clock signal
6	F_ADC_DOUT2	P4	3	3.3V	ADC data output
7	F_W_PWM_TOP_N2	N3	3	3.3V	Phase W PWM upper leg control signal
8	F_W_PWM_BOTTOM_N2	R3	3	3.3V	Phase W PWM upper leg control signal
9	F_U_PWM_TOP_N2	L4	4	3.3V	Phase U PWM upper leg control signal
10	F_U_PWM_BOTTOM_N2	M3	3	3.3V	Phase U PWM upper leg control signal
11	F_V_PWM_TOP_N2	P2	3	3.3V	Phase V PWM upper leg control signal
12	F_V_PWM_BOTTOM_N2	T2	3	3.3V	Phase V PWM upper leg control signal
13	F_SC_RESET_N2	M2	3	3.3V	Reserved IO
14	F_SC_N2	N2	3	3.3V	Reserved IO
15	F_BLEEDER_ON2	P1	3	3.3V	Reserved IO
16	F_BUS_EN2	R1	3	3.3V	Reserved IO
17	F_IBUS2	M1	3	3.3V	Reserved IO
18	F_VTEMP_MOS2	N1	3	3.3V	Reserved IO
19	F_VBUS2	K1	4	3.3V	Reserved IO
20	F_VTEMP_AMB2	L1	3	3.3V	Reserved IO
21	NC	-	-	-	Floating
22	GND	-	-	-	GND

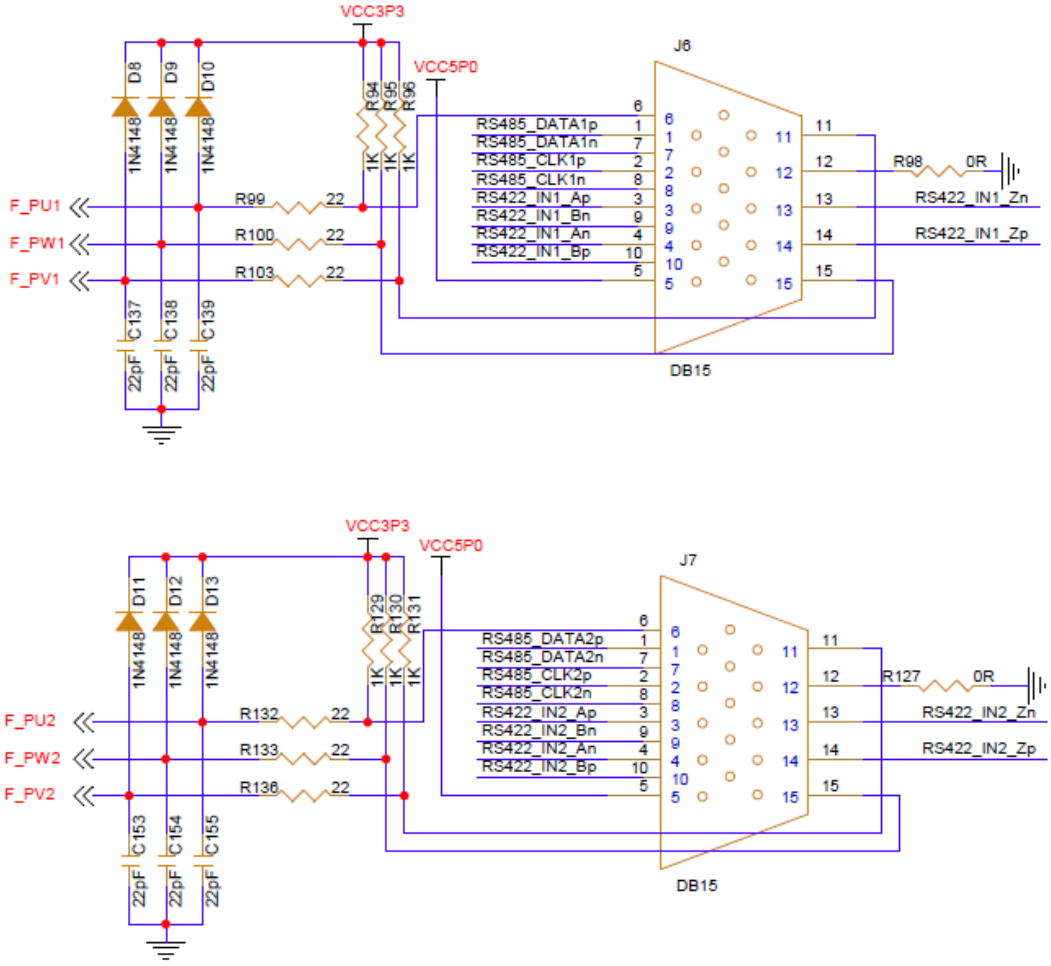
J12 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
23	NC	-	-	-	Floating
24	GND	-	-	-	GND

3.8 Motor Control Interface

3.8.1 Introduction

There are 2-lane motor control interfaces on the board. Each lane motor control interface contains three-lane RS422 differential signals, one-lane RS485 differential data signal, one-lane differential clock signal, and three GPIOs for FPGA-motor communication. The schematic of motor control interfaces is as shown in Figure 3-7.

Figure 3-7 Schematic of Motor Control Interfaces



3.8.2 Pin Distribution

Table 3-8 Pin Distribution of Motor Control Interface 1

J6 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	RS485_DATA1P	-	-	-	RS485 data signal
2	RS485_CLK1P	-	-	-	RS485 clock signal
3	RS422_IN1_Ap	-	-	-	Incremental encoder phase A pulse signal+
4	RS422_IN1_An	-	-	-	Incremental encoder phase A pulse signal-
5	VCC5P0	-	-	5V	Power
6	F_PU1	F4	4	3.3V	Incremental Encoder U Signal
7	RS485_DATA1N	-	-	-	RS485 data signal
8	RS485_CLK1N	-	-	-	RS485 clock signal
9	RS422_IN1_Bn	-	-	-	Incremental encoder phase B pulse signal+
10	RS422_IN1_Bp	-	-	-	Incremental encoder phase B pulse signal-
11	F_PV1	G6	4	3.3V	Incremental encoder V signal
12	GND	-	-	-	GND
13	RS422_IN1_Zn	-	-	-	Incremental encoder phase Z pulse signal-
14	RS422_IN1_Zp	-	-	-	Incremental encoder phase Z pulse signal+
15	F_PW1	F1	4	3.3V	Incremental Encoder W Signal

Table 3-9 Pin Distribution of Motor Control Interface 1

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_PU1	F4	4	3.3V	Incremental Encoder U Signal
F_PW1	F1	4	3.3V	Incremental Encoder W Signal
F_PV1	G6	4	3.3V	Incremental Encoder V Signal
F_RS422_OUT_A1	F5	4	3.3V	Incremental Encoder Phase A Pulse Signal
F_RS422_OUT_B1	E1	4	3.3V	Incremental Encoder Phase B Pulse Signal
F_RS422_OUT_Z1	E2	4	3.3V	Incremental Encoder Phase Z Pulse Signal
F_RS485_DATA_TX1	G2	4	3.3V	RS485 Transceiver Transmitting Signal
F_RS485_DATA_RX1	H6	4	3.3V	RS485 Transceiver Receiving Signal
F_RS485_DATA_CT1	G1	4	3.3V	RS485 Transceiver Signal Direction Control
F_RS485_CLK_TX1	G5	4	3.3V	RS485 Transceiver Transmitting Signal
F_RS485_CLK_RX1	G3	4	3.3V	RS485 Transceiver Receiving Signal
F_RS485_CLK_CT1	G4	4	3.3V	RS485 Transceiver Signal Direction Control

Table 3-10 Pin Distribution of Motor Control Interface 2

J7 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	RS485_DATA2p	-	-	-	RS485 data signal
2	RS485_CLK2p	-	-	-	RS485 clock signal
3	RS422_IN2_Ap	-	-	-	Incremental encoder phase A pulse signal+
4	RS422_IN2_An	-	-	-	Incremental encoder phase A pulse signal-
5	VCC5P0	-	-	5V	Power
6	F_PU2	H2	4	3.3V	Incremental Encoder U Signal
7	RS485_DATA2n	-	-	-	RS485 data signal

J7 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
8	RS485_CLK2n	-	-	-	RS485 clock signal
9	RS422_IN2_Bn	-	-	-	Incremental encoder phase B pulse signal+
10	RS422_IN2_Bp	-	-	-	Incremental encoder phase B pulse signal-
11	F_PV2	J6	4	3.3V	Incremental Encoder V Signal
12	GND	-	-	-	GND
13	RS422_IN2_Zn	-	-	-	Incremental encoder phase Z pulse signal-
14	RS422_IN2_Zp	-	-	-	Incremental encoder phase Z pulse signal+
15	F_PW2	H1	4	3.3V	Incremental Encoder W Signal

Table 3-11 Pin Distribution of Motor Control Interface 2

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_PU2	H2	4	3.3V	Incremental Encoder U Signal
F_PW2	H1	4	3.3V	Incremental Encoder W Signal
F_PV2	J6	4	3.3V	Incremental Encoder V Signal
F_RS422_OUT_A2	H5	4	3.3V	Incremental Encoder Phase A Pulse Signal
F_RS422_OUT_B2	H4	4	3.3V	Incremental Encoder Phase B Pulse Signal
F_RS422_OUT_Z2	H3	4	3.3V	Incremental Encoder Phase Z Pulse Signal
F_RS485_DATA_TX2	K6	4	3.3V	RS485 Transceiver Transmitting Signal
F_RS485_DATA_RX2	K2	4	3.3V	RS485 Transceiver Receiving Signal
F_RS485_DATA_CT2	K3	4	3.3V	RS485 Transceiver Signal Direction Control
F_RS485_CLK_TX2	J4	4	3.3V	RS485 Transceiver Transmitting Signal

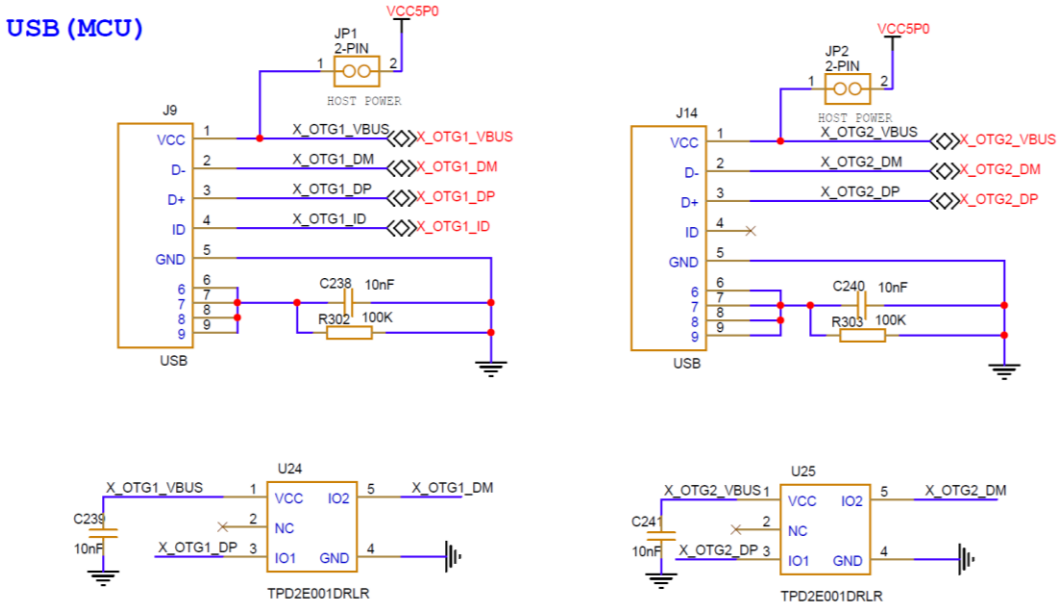
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_RS485_CLK_RX2	J1	4	3.3V	RS485 Transceiver Receiving Signal
F_RS485_CLK_CT2	J2	4	3.3V	RS485 Transceiver Signal Direction Control

3.9 OTG Interface

3.9.1 Introduction

The development board has 2-lane OTG interfaces with a mini USB-B port with electrostatic protection for online debugging and downloading or connecting to a master/slave for communication. The OTG interface schematic is as shown in Figure 3-8.

Figure 3-8 Schematic of OTG Interfaces



3.9.2 Pin Distribution

Table 3-12 J9 Pin Distribution for OTG Interface 1

J9 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	X_OTG1_VBUS	-	-	3.3V	Voltage detection
2	X_OTG1_DM	T14	MCU	3.3V	OTG data signal
3	X_OTG1_DP	T15	MCU	3.3V	OTG data signal
4	X_OTG1_ID	-	-	3.3V	OTG master/slave identification
5	GND	-	-	-	GND

Table 3-13 J14 Pin Distribution for OTG Interface 2

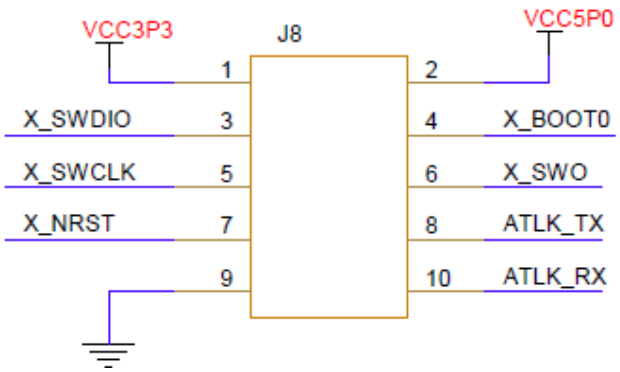
J14 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	X_OTG2_VBUS	G15	MCU	3.3V	Voltage detection
2	X_OTG2_DM	H14	MCU	3.3V	OTG data signal
3	X_OTG2_DP	H15	MCU	3.3V	OTG data signal
4	NC	-	-	-	Floating
5	GND	-	-	-	GND

3.10 AT-Link Interface

3.10.1 Introduction

There is 1-lane AT-Link interface on the board to connect to the master for debugging programming. The schematic of AT-Link interfaces is as shown in Figure 3-9.

Figure 3-9 Schematic of AT-Link Interface



3.10.2 Pin Distribution

Table 3-14 J8 Pin Distribution for AT-Link Interface

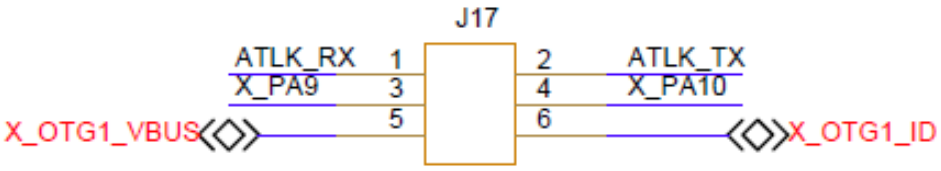
J8 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	VCC3P3	-	-	3.3V	Power
2	VCC5P0	-	-	5V	Power
3	X_SWDIO	K15	MCU	3.3V	Serial data input/output
4	X_BOOT0	R16	MCU	3.3V	Boot
5	X_SWCLK	L14	MCU	3.3V	Serial clock input
6	X_SWO	N14	MCU	3.3V	Single bus output
7	X_NRST	J16	MCU	3.3V	Reset
8	ATLK_TX	-	-	3.3V	AT-Link serial port TX signal
9	GND	-	-	-	GND
10	ATLK_RX	-	-	3.3V	AT-Link serial port RX signal

3.11 AT-Link/OTG 1 Selection Interface

3.11.1 Introduction

There is 1-lane AT-Link/OTG 1 selection interface on the board. When the OTG 1 is selected by the jumper, PA9 and PA10 are connected to the OTG 1 (J9) interface; and when the AT-Link interface is selected by the jumper, the OTG 1 interface is disconnected and AT-Link (J8) interface is connected. The schematic of AT-Link/OTG 1 selection interface is shown in Figure 3-10.

Figure 3-10 Schematic of AT-Link/OTG 1 Selection Interface



3.11.2 Pin Distribution

Table 3-15 J17 Pin Distribution for AT-Link/OTG 1 Selection Interface

J17 Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	ATLK_RX	-	-	3.3V	AT-Link serial port RX signal
2	ATLK_TX	-	-	3.3V	AT-Link serial port TX signal
3	X_PA9	T12	MCU	3.3V	GPIO
4	X_PA10	T13	MCU	3.3V	GPIO
5	X_OTG1_VBUS	-	-	3.3V	Voltage detection
6	X_OTG1_ID	-	-	3.3V	OTG master/slave identification

3.12 GPIO

3.12.1 Introduction

There is one 14-pin double-row pin header and two 40-pin double-row pin headers on the board, which respectively route out 11 GPIOs and 37 MCUs to facilitate user testing. The schematic of GPIO interfaces is shown in below.

Figure 3-11 Schematic of GPIO Interface

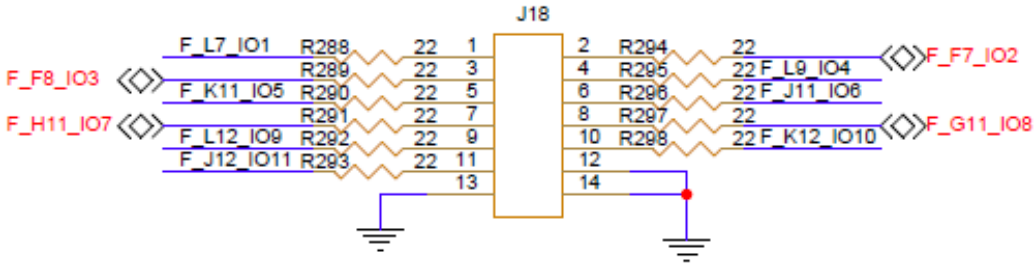
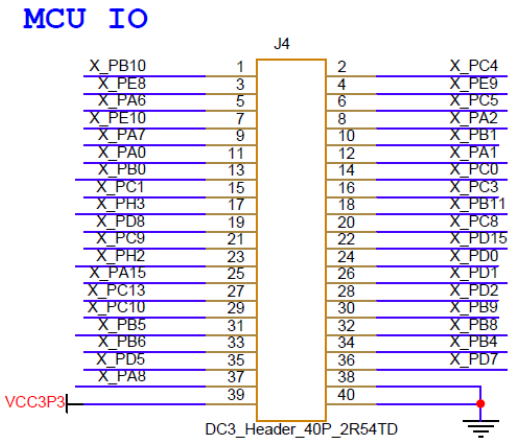


Figure 3-12 Schematic of MCU IO Interface



3.12.2 Pin Distribution

Table 3-16 GPIO Pin Distribution

Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	F_L7_IO1	L7	1	3.3V	GPIO
2	F_F7_IO2	F7	7	3.3V	GPIO
3	F_F8_IO3	F8	7	3.3V	GPIO
4	F_L9_IO4	L9	1	3.3V	GPIO
5	F_K11_IO5	K11	1	3.3V	GPIO
6	F_J11_IO6	J11	1	3.3V	GPIO
7	F_H11_IO7	H11	7	3.3V	GPIO
8	F_G11_IO8	G11	7	3.3V	GPIO
9	F_L12_IO9	L12	1	3.3V	GPIO
10	F_K12_IO10	K12	1	3.3V	GPIO
11	F_J12_IO11	J12	1	3.3V	GPIO
12	GND	-	-	-	GND
13	GND	-	-	-	GND
14	GND	-	-	-	GND

Table 3-17 IO Pin Distribution of MCU

Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	X_PB10	A14	MCU	3.3V	MCU IO
2	X_PC4	B16	MCU	3.3V	MCU IO
3	X_PE8	B14	MCU	3.3V	MCU IO
4	X_PE9	B13	MCU	3.3V	MCU IO
5	X_PA6	C16	MCU	3.3V	MCU IO
6	X_PC5	C15	MCU	3.3V	MCU IO
7	X_PE10	C13	MCU	3.3V	MCU IO
8	X_PA2	D16	MCU	3.3V	MCU IO
9	X_PA7	D15	MCU	3.3V	MCU IO
10	X_PB1	D14	MCU	3.3V	MCU IO
11	X_PA0	E16	MCU	3.3V	MCU IO
12	X_PA1	E15	MCU	3.3V	MCU IO
13	X_PB0	E14	MCU	3.3V	MCU IO

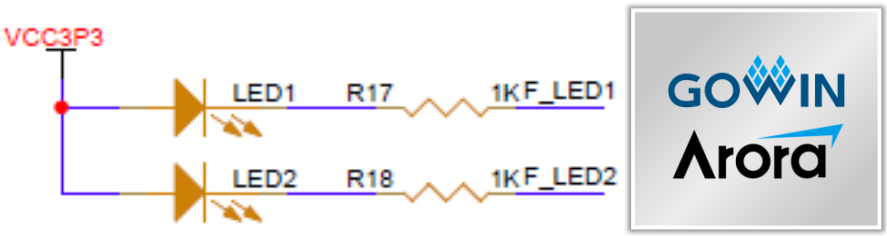
Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
14	X_PC0	F16	MCU	3.3V	MCU IO
15	X_PC1	F15	MCU	3.3V	MCU IO
16	X_PC3	F14	MCU	3.3V	MCU IO
17	X_PH3	G14	MCU	3.3V	MCU IO
18	X_PB11	G13	MCU	3.3V	MCU IO
19	X_PD8	H13	MCU	3.3V	MCU IO
20	X_PC8	J15	MCU	3.3V	MCU IO
21	X_PC9	J14	MCU	3.3V	MCU IO
22	X_PD15	J13	MCU	3.3V	MCU IO
23	X_PH2	K14	MCU	3.3V	MCU IO
24	X_PD0	K13	MCU	3.3V	MCU IO
25	X_PA15	L15	MCU	3.3V	MCU IO
26	X_PD1	J13	MCU	3.3V	MCU IO
27	X_PC13	M16	MCU	3.3V	MCU IO
28	X_PD2	M15	MCU	3.3V	MCU IO
29	X_PC10	M14	MCU	3.3V	MCU IO
30	X_PB9	N16	MCU	3.3V	MCU IO
31	X_PB5	N15	MCU	3.3V	MCU IO
32	X_PB8	P16	MCU	3.3V	MCU IO
33	X_PB6	P15	MCU	3.3V	MCU IO
34	X_PB4	R14	MCU	3.3V	MCU IO
35	X_PD5	P13	MCU	3.3V	MCU IO
36	X_PD7	R13	MCU	3.3V	MCU IO
37	X_PA8	T11	MCU	3.3V	MCU IO
38	GND	-	-	-	GND
39	VCC3P3	-	-	3.3V	Power
40	GND	-	-	-	GND

3.13 LED & Key

3.13.1 Introduction

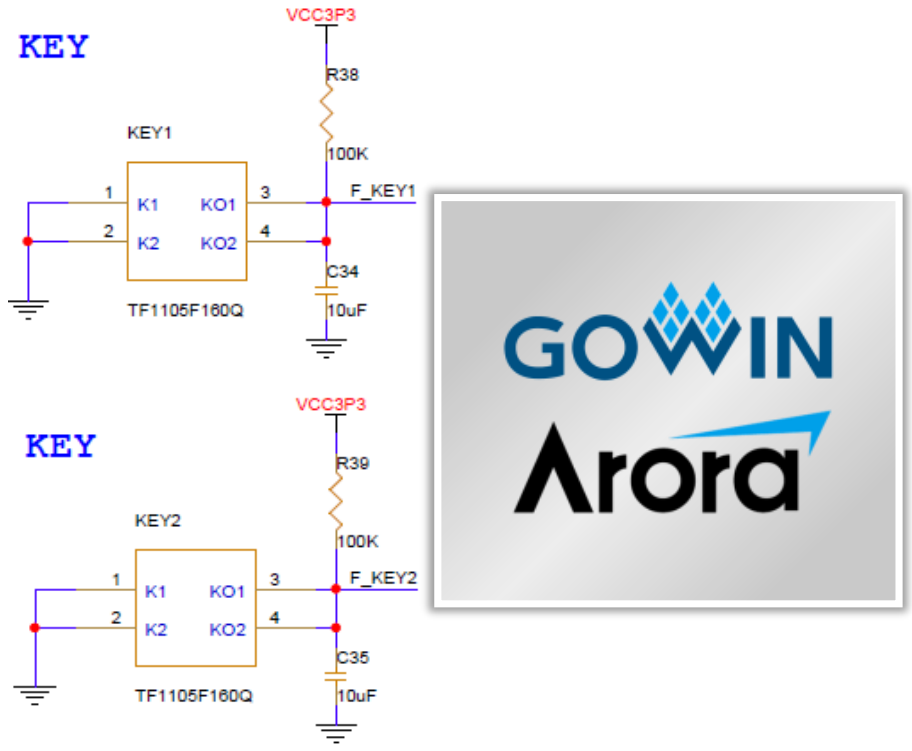
The development board includes two user LEDs. The user LEDs are connected to the IO of FPGA BANK5 and can be switched on and off via the program. The user LEDs will be on when the IO voltage is high. The user LEDs will be off when the IO voltage is low. The connection diagram is shown in Figure 3-13.

Figure 3-13 Connection Diagram of LED



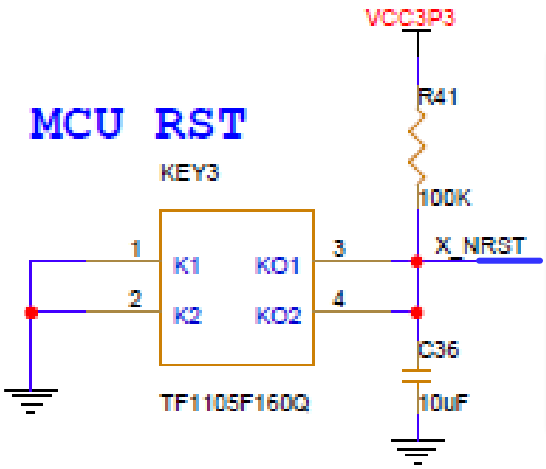
There are two user keys on the development board. The user keys are respectively connected to the general IOs of FPGA BANK5. The corresponding IO input voltage of the FPGA is low when the key is pressed while high when the key is not pressed. The connection diagram is shown in Figure 3-14.

Figure 3-14 Connection Diagram of Key



There is one reset key on the development board. The corresponding IO input voltage of the FPGA is low when the key is pressed while high when the key is not pressed. The connection diagram is shown in Figure 3-15.

Figure 3-15 Connection Diagram of MCU Reset Key



3.13.2 Pin Distribution

Table 3-18 Pin Distribution of LED & Key

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_LED1	B1	5	3.3V	LED
F_LED2	C1	5	3.3V	LED
F_KEY1	A2	5	3.3V	Key
F_KEY2	C2	5	3.3V	Key

Table 3-19 Pin Distribution of MCU Reset Key

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
X_NRST	J16	MCU	3.3V	MCU reset key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