



Gowin FP Sqrt IP

User Guide

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Revision History

Date	Version	Description
05/09/2024	1.0E	Initial version published.

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1 About This Guide

1.1 Purpose

The purpose of Gowin FP Sqrt IP User Guide is to help you learn the features and usage of Gowin FP Sqrt IP by providing the descriptions of functions, ports, timing, GUI and reference design. The software screenshots and the supported products listed in this manual are based on Gowin Software 1.9.9 Beta-4. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI website. You can find the related documents at www.gowinsemi.com:

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS821, GW1NS series of FPGA Products Data Sheet](#)
- [DS861, GW1NSR series of FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS971, GW2AN-18X & 9X Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS981, GW5AST series of FPGA Products Data Sheet](#)
- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
ALU	Arithmetic Logical Unit
LUT	Look-up Table
Sqrt	Square Root
IP	Intellectual Property

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Introduction to Gowin FP Sqrt IP

Gowin FP Sqrt IP can obtain the square root of single-precision floating-point numbers. This IP supports optional output ports, such as overflow zero and NaN (Not a Number), and is designed to use fewer logic resources to perform the computation of floating-point square root.

Table 2-1 Gowin FP Sqrt IP

Gowin FP Sqrt IP	
Logic Resource	Please refer to Table 2-2
Delivered Doc.	
Design Files	Verilog
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.9 Beta-4 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Features

- Can obtain the square root of single-precision floating-point numbers
- Supports optional output port

2.3 Max. Frequency

The max. frequency of Gowin FP Sqrt IP is mainly determined by speed grade of the selected devices.

2.4 Latency

The latency of Gowin FP Sqrt IP is determined by the configuration parameters.

2.5 Resource Utilization

Gowin FP Sqrt IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades.

Take GW2A-55 FPGA as an example. See Table 2-2 for the resource utilization. For the applications on the other GOWINSEMI devices, please refer to the later release.

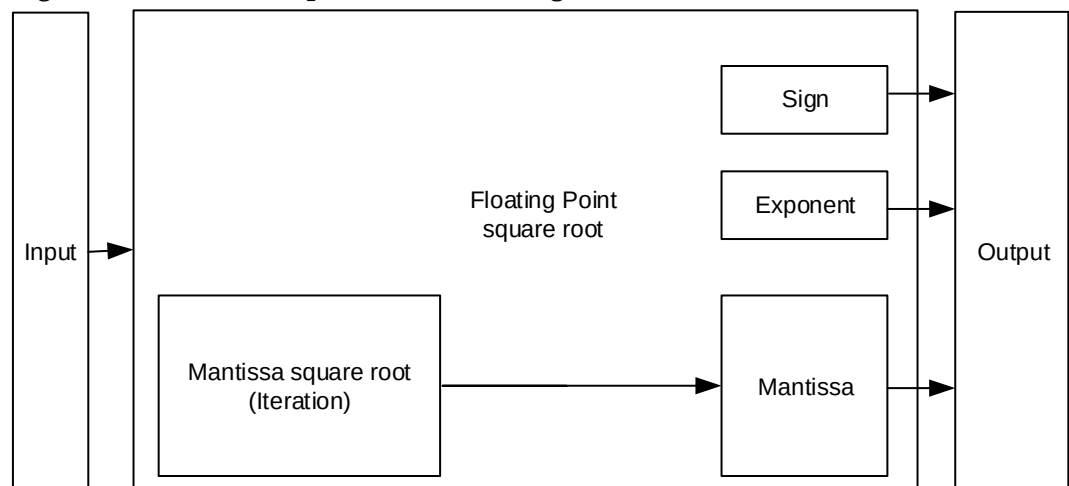
Table 2-2 Gowin FP Sqrt IP Resource Utilization

Device	Speed Grade	Resource Name	Resource Utilization
GW2A-55	C8/I7	Registers	1774
		LUTs	1552
		ALUs	2684
		I/O Buf	70

3 Functional Description

Gowin FP Sqrt IP can obtain the square root of single-precision floating-point numbers. Users can configure parameters according to their requirements when generating this module. The structure diagram is shown as Figure 3-1.

Figure 3-1 Gowin FP Sqrt IP Structure Diagram



4 Port Description

The IO ports of Gowin FP Sqrt IP are shown in Figure 4-1. For the details, you can see Table 4-1.

Figure 4-1 Gowin FP Sqrt IP IO Diagram

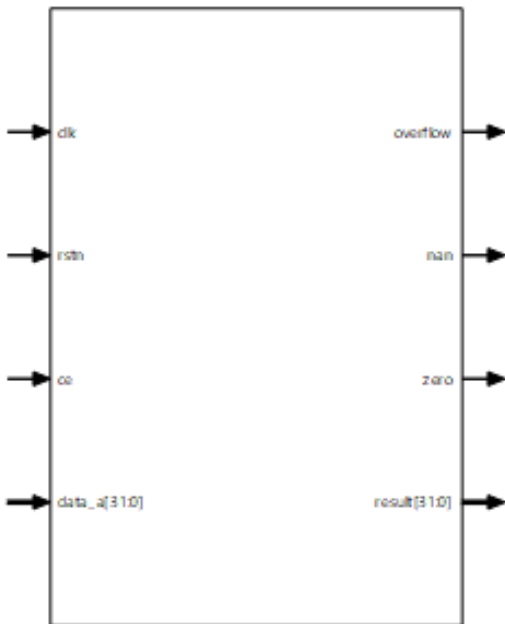


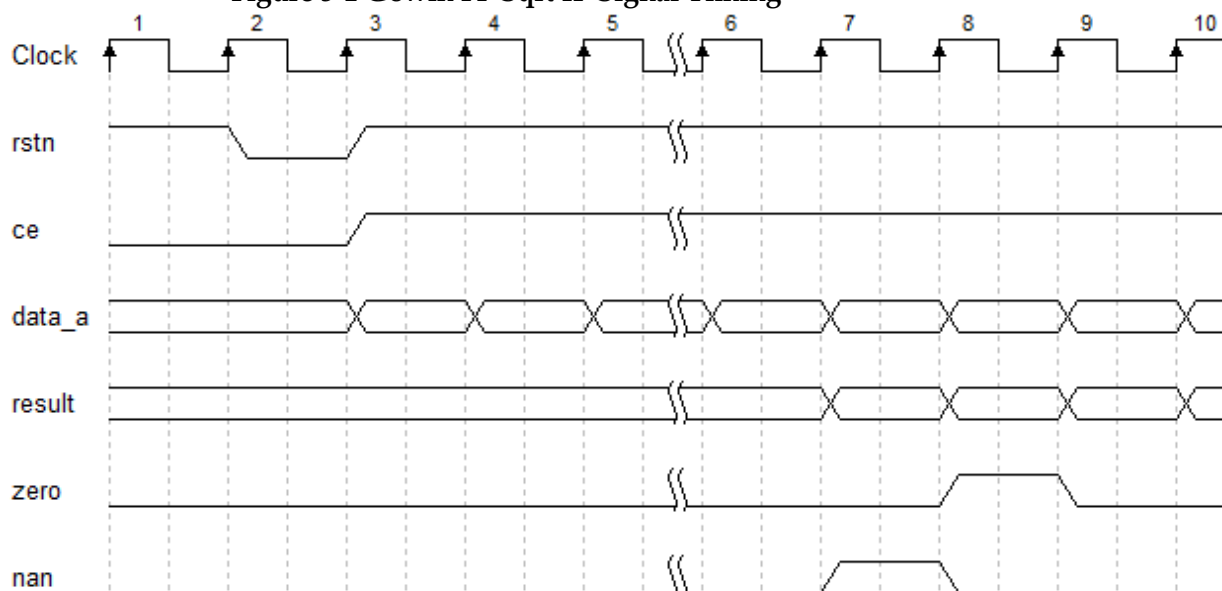
Table 4-1 Gowin FP Sqrt IP Port List

Signal	I/O	Description
clk	Input	Clock signal
rstn	Input	Reset signal, active-low
ce	Input	Clock enable signal, active-high (optional)
data_a	Input	Input a
overflow	Output	Overflow
nan	Output	NaN
zero	Output	Zero
result	Output	Output result

5 Timing Description

The timing of Gowin FP Sqrt IP is as shown in Figure 5-1.

Figure 5-1 Gowin FP Sqrt IP Signal Timing



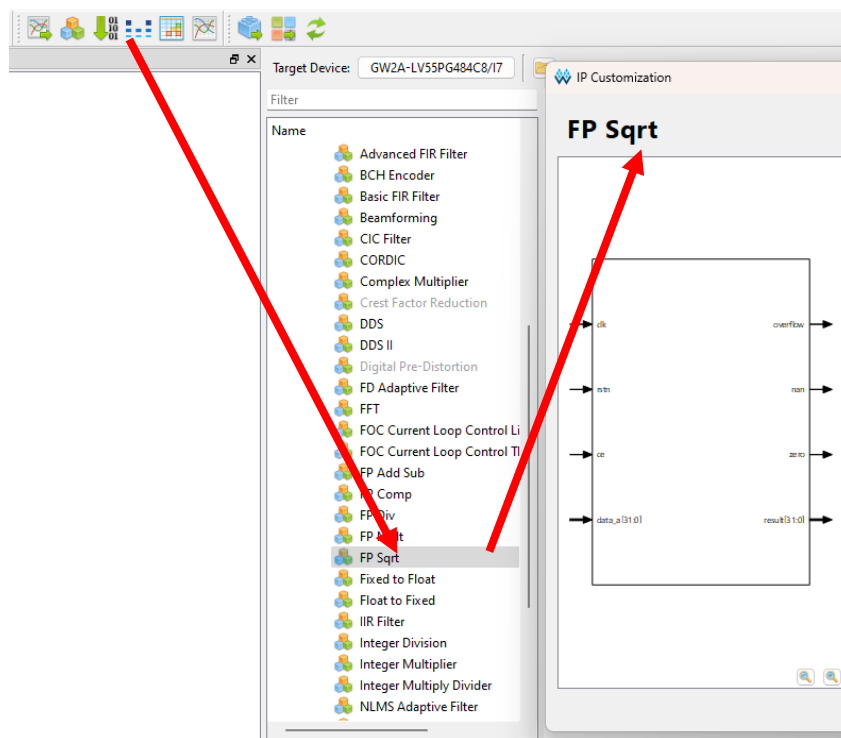
As shown in the figure above, after inputting two single-precision floating-point numbers, the square root of the first number along with its data type is output with a delay of 25 clock cycles.

6 Call and Configure

6.1 IP Generation

Click "Tools > IP Core Generator > DSP and Mathematics" to call and configure FP Sqrt; toolbar icon is also available to open the IP as shown in Figure 6-1.

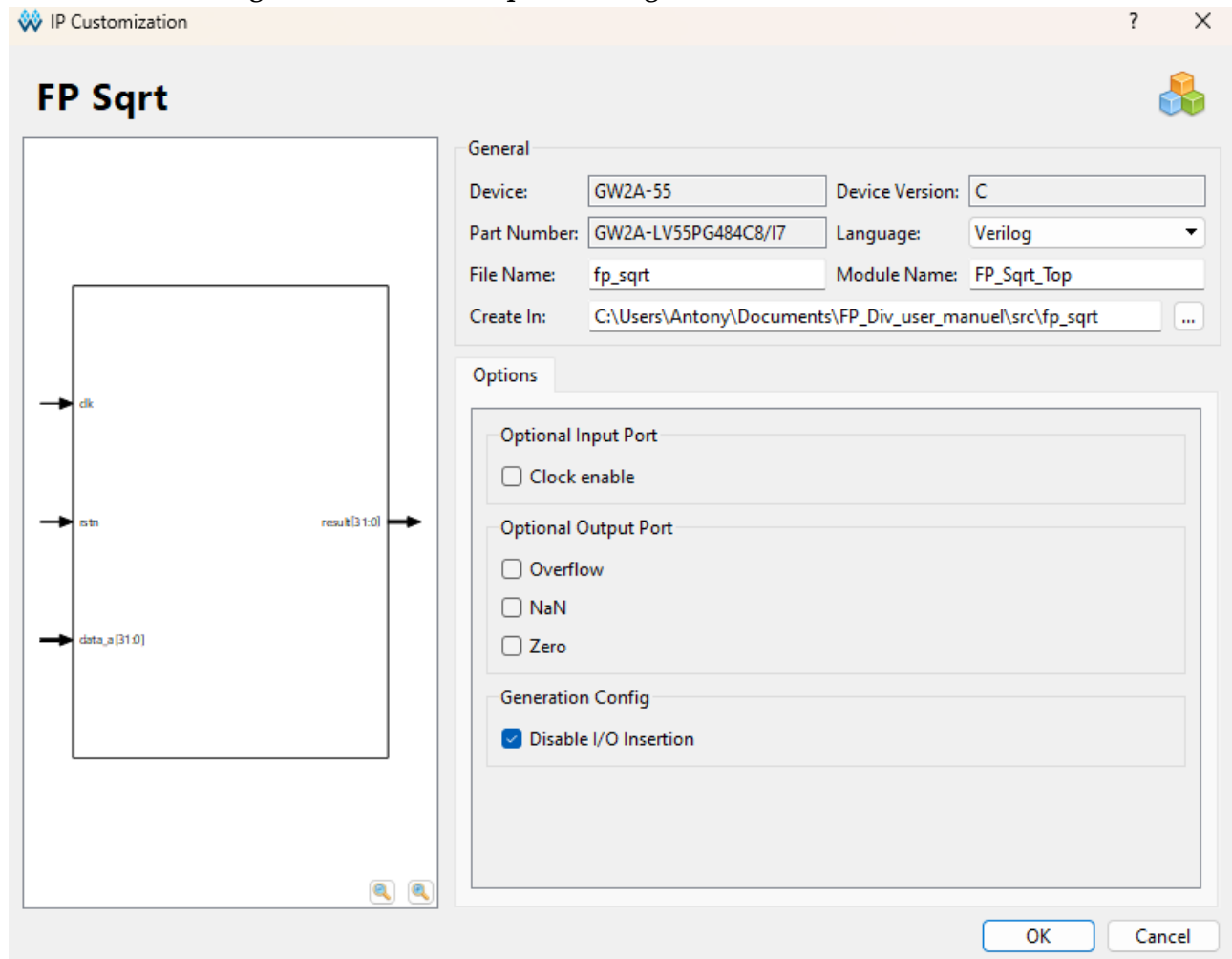
Figure 6-1 Open the IP via Toolbar Icon



6.2 IP Configuration

Gowin FP Sqrt IP configuration interface is shown in Figure 6-2.

Figure 6-2 Gowin FP Sqrt IP Configuration Interface



This manual takes GW2A-LV55PG484C8/I7 part number as an example.

- You can configure the path of generated IP core folder in the "Create In" text box.
- You can configure the generated IP file name in the "File Name" text box.
- You can configure the generated IP module name in the "Module Name" text box.

7 Reference Design

Please refer to the related test cases in Gowin FP Sqrt IP [RefDesign](#).

8 Documents Delivered

The delivery file of Gowin FP Sqrt IP includes documentation and reference design.

8.1 Documentation

The folder contains the user guide in PDF version.

Table 8-1 Gowin FP Sqrt IP Doc. List

Name	Description
IPUG1184, Gowin FP Sqrt IP User Guide	Gowin FP Sqrt IP User Guide, namely this one.

8.2 Reference Design

Gowin FP Sqrt IP RefDesign folder contains the netlist file, user reference design, constraints file, top-level file, and project file, etc.

Table 8-2 Gowin FP Sqrt IP RefDesign Folder Content List

Name	Description
top.v	The top module of reference design
FP_Sqrt.cst	Project physical constraints file
FP_Sqrt.sdc	Project timing constraints file
FP_Sqrt.rao	Online logic analyzer file
fp_Sqrt.v	Generate FP Sqrt IP top-level file, encrypted

