



Gowin ASRC IP

User Guide

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Revision History

Date	Version	Description
04/15/2020	1.0E	Initial version published.
02/02/2024	1.0.1E	A note of clock frequency added.
09/05/2024	1.0.2E	Descriptions of 3.3 Latency updated.
04/11/2025	1.1E	Sampling compatible frequency updated.
06/17/2026	1.2E	● Updated compatible sampling frequency. ● Updated descriptions of port bit width and channel number. ● Updated Table 3-1 Resource Utilization.

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1 About This Guide

1.1 Purpose

The purpose of Gowin ASRC IP User Guide is to help users learn the features and usage of Gowin ASRC IP by providing the descriptions of the product, functions, GUI and reference design. The software screenshots in this manual are based on V 1.9.12.03. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1239, GW5AST series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)
- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1118, GW5ART series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
ASRC	Asynchronous Sample Rate Converter
DSP	Digital Signal Processing
FD Filter	Fractional Delay Filter
FIR Filter	Finite Impulse Response Filter
IP	Intellectual Property
LIF	Lagrange Interpolation Filter
LUT	Look-up Table
RAM	Random Access Memory
SRC	Sample Rate Conversion

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Introduction to Gowin ASRC IP

The Gowin ASRC IP is designed to convert audio data from one sampling frequency to another.

Table 2-1 Gowin ASRC IP Overview

Gowin ASRC IP	
Logic Resource	Please refer to Table 3-1.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software

Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Introduction to ASRC Algorithm

2.2.1 Sample Ratio Formula

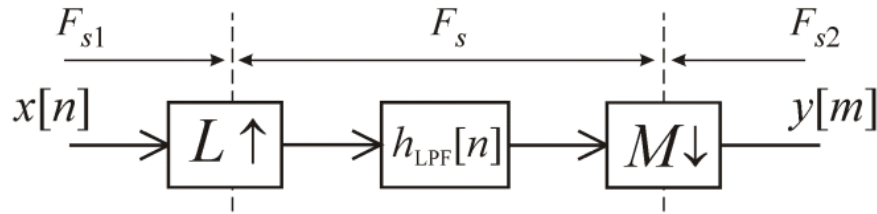
The sample ratio formula is as follow:

$$Ratio = \frac{f_{s-out}}{f_{s-in}} = \frac{t_{s-in}}{t_{s-out}}$$

The f_{s-in} is the input sample frequency; f_{s-out} is the output sample frequency; t_{s-in} is the input sample period and t_{s-out} is the output sample period.

2.2.2 Introduction to Traditional SRC Algorithm

Figure 2-1 Traditional SRC Algorithm Diagram



There are two disadvantages of traditional SRC algorithm.

First of all, Traditional SRC algorithm can obtain the converted data through the up-sampling, low-pass filtering and down-sampling. The up-sampling and down-sampling ratios need to meet the following formula:

$$L = F_{s2} / \gcd(F_{s1}, F_{s2})$$

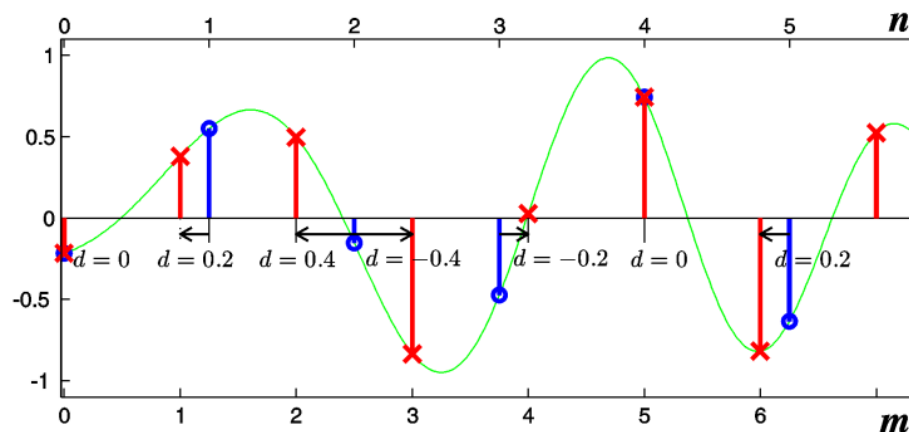
$$M = F_{s1} / \gcd(F_{s1}, F_{s2})$$

That is, L and M need to satisfy a certain common multiple. When the values of L and M are large, such as L=160 and M=147, larger values of L and M will require narrower band factors and the design of interpolation filters with more inserted values. However, the filters also need to have smaller delays and faster response designs, leading to increased design complexity.

Secondly, since L and M are fixed values, once there is a change in the input sampling clock and output sampling clock (i.e., a change in the sampling ratio), it will be impossible to meet the final output requirements.

2.2.3 Introduction to ASRC Algorithm

Figure 2-2 Fractional Delay Diagram of ASRC Algorithm



The ASRC algorithm uses a Fractional Delay (FD) Filter to calculate the fractional delay between the output sample position and the nearest input sample position. Through resampling conversion, it outputs the resampled data.

The formula of the fraction delay is as follow:

$$D[m] = D[m - 1] - F_{s1}/F_{s2} + \Delta n[m] \in$$

The $F_{s1}/F_{s2} = M/L$, and $\Delta n[m]$ is the number of new samples required to calculate the next sample in the input buffer.

Compared with the traditional SRC algorithm, by calculating the ratio $F_{s1}/F_{s2} = M/L$, when $M=1$, the FD filters need a smaller L to satisfy the design requirement.

Meanwhile, the ASRC algorithm processes sampled data based on calculated position delays, so any variation in the input and output sampling clocks will be reflected in the processing accordingly.

2.2.4 Lagrange Interpolation Filter

The FD filter can be realized by Lagrange Interpolation Filter.

The formula of N-order Lagrange interpolation is as follow:

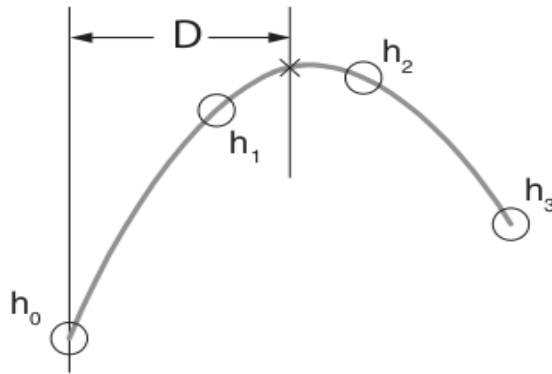
$$y(x) = \sum_{k=0}^N l_k(x) f(x_k)$$

Where,

$$l_k(x) = \frac{(x-x_0)\dots(x-x_{k-1})(x-x_{k+1})\dots(x-x_N)}{(x_k-x_0)\dots(x_k-x_{k-1})(x_k-x_{k+1})\dots(x_k-x_N)}.$$

The Lagrange interpolation filter calculates the sampled filter coefficients by performing Lagrange interpolation on the filter coefficients. It then obtains the output sampling data by filtering and resampling. As shown in Figure 2-3, first-order Lagrange interpolation can obtain the output sampling point through two sampling points, while third-order Lagrange interpolation can obtain the output sampling point through four points.

Figure 2-3 Schematic Diagram of Filter Coefficient Processing Using Lagrange Interpolation



The formula of third-order Lagrange interpolation is as follow:

$$H = \frac{(D-2)(D-3)}{2} \left(\frac{-(D-1)h_0}{3} + Dh_1 \right) + \frac{D(D-1)}{2} \left(-(D-3)h_2 + \frac{(D-2)h_3}{3} \right)$$

The D is coefficient delay, and h_0 , h_1 , h_2 , h_3 are filter coefficients.

3 Features and Performance

3.1 Features

- Fully asynchronous
- Supports 4 or 8 channels, 32-bit audio data input and output
- Supports automatic conversion ratio detection
- Supports input sample frequency with range from 8 kHz to 384 kHz
- Supports output sample frequency with range from 8 kHz to 384 kHz
- Continuous conversion ratio: 1:8 (downsampling) to 8:1 (upsampling)
- Low latency

3.2 Max. Frequency

The maximum frequency of Gowin ASRC IP is mainly determined by the speed grade of the devices and the configuration parameters.

3.3 Latency

The latency of Gowin ASRC IP is determined by the configuration parameters.

- If upsampling, the delay depends on the input sampling frequency, and the delay is calculated as follows: latency = phase delay (32) + FIFO delay (16) = 48 input sampling cycles. When operating in auto-detect sampling ratio mode, an additional latency of approximately 128 input sampling cycles is added.
- If downsampling, the delay is calculated as follows: latency = phase delay ($32 * \frac{f_{Sout}}{f_{Sin}}$) + FIFO delay (16), in the unit of input sample cycles.

When operating in auto-detect sampling ratio mode, an additional latency of approximately 128 input sampling cycles is added.

Examples are as follows:

- If converting from 48 kHz to 48 kHz, latency = $32 + 16 = 48$ input sample cycles.
- If converting from 48 kHz to 96 kHz, latency = $32 + 16 = 48$ input sample cycles.
- If converting from 48 kHz to 44.1 kHz, latency = $32 \times 44.1/48 + 16 = 45.4$ input sample cycles.

3.4 Resource Utilization

Gowin ASRC IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different density, speed, grade or the different modes of IP configuration.

Take the GW5A-25 devices as an example. See Table 3-1 for the resource utilization. For the applications on the other GOWINSEMI devices, please refer to the later release.

Table 3-1 Resource Utilization

Device	Speed Grade	Resource	Resource Utilization	Note
GW5A-25	ES	LUT	2327	4 channels; Supports a maximum sampling frequency of 192 kHz.
		ALU	826	
		REG	1766	
		BSRAM	11	
		DSP	10	
GW5A-25	ES	LUT	3056	4 channels; Supports a maximum sampling frequency of 384 kHz.
		ALU	1113	
		REG	2180	
		BSRAM	14	
		DSP	20	
GW5A-25	ES	LUT	2857	8 channels; Supports a maximum sampling frequency of 192 kHz.
		ALU	986	
		REG	2092	
		BSRAM	18	
		DSP	12	
GW5A-25	ES	LUT	3765	8 channels; Supports a maximum sampling frequency of 384
		ALU	1273	
		REG	2540	

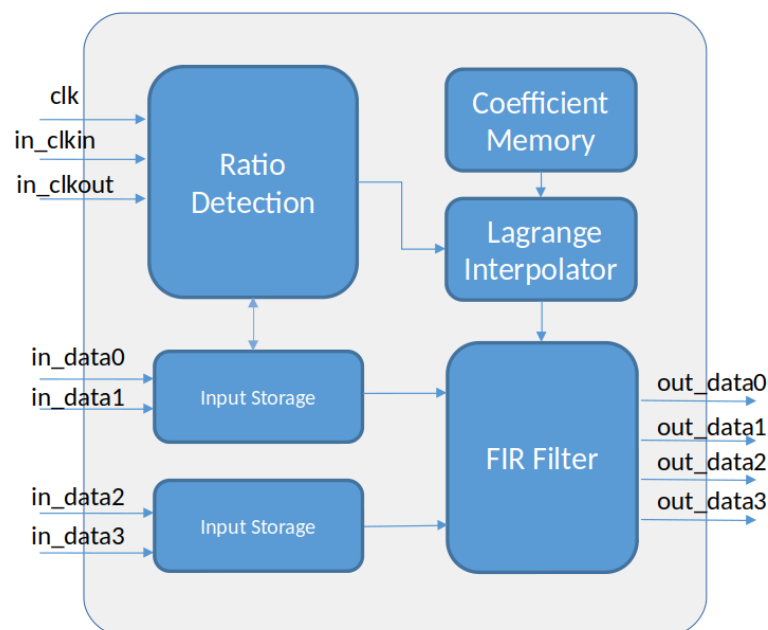
Device	Speed Grade	Resource	Resource Utilization	Note
		BSRAM	21	kHz.
		DSP	24	

4 Functional Description

4.1 Structure and Function of Gowin ASRC IP

Gowin ASRC IP implementation block diagram is shown in Figure 4-1.

Figure 4-1 Gowin ASRC IP Implementation Block Diagram (4 Channels)



It consists of the following modules.

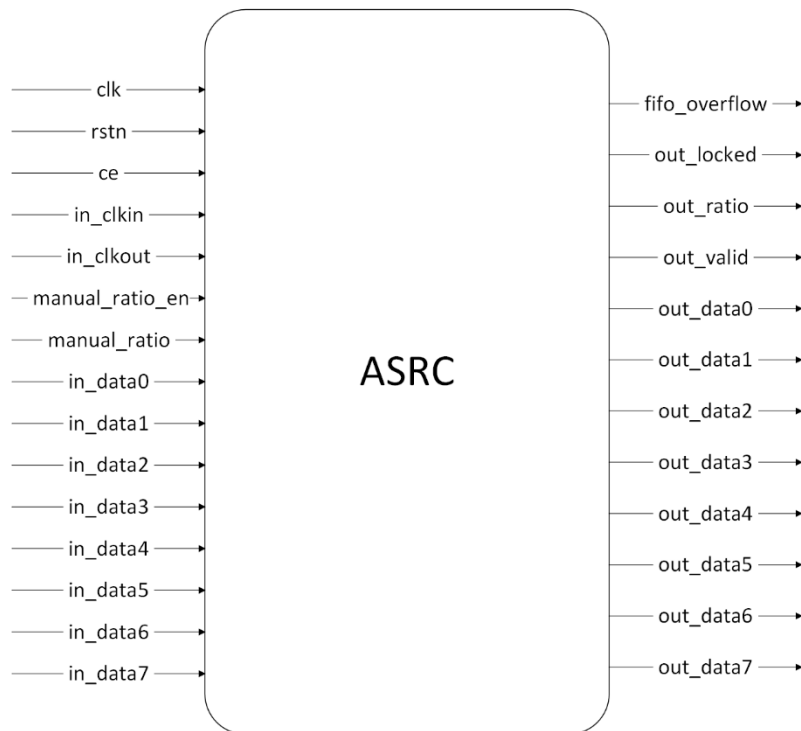
1. **Ratio Detection:** It calculates the sampling rate based on the input sampling clock and the output sampling clock. When downsampling, $ratio = f_{s-out}/f_{s-in}$; when upsampling, $ratio=1$.
2. **Input Storage:** Store input data, controlled by FIFO.
3. **Coefficient Memory:** Store filter coefficients.
4. **Lagrange Interpolator:** It calculates the position delay based on the sampling rate. By performing Lagrange interpolation on the filter coefficients, it finally obtains the required sampling filter coefficients

5. FIR Filter: Filter the data to realize sample conversion to obtain the sampling data.

4.2 Port Description

The /IO ports of Gowin ASRC IP are shown in Figure 4-2.

Figure 4-2 Gowin ASRC IP Port Diagram



For the details, refer to Table 4-1.

Table 4-1 Gowin ASRC IP I/O List

Signal	I/O	Data Width	Description
clk	Input	1	Clock signal
ce	Input	1	Enable signal
rstn	Input	1	Reset signal, active - low
in_clkin	Input	1	Input sample clock
in_clkout	Input	1	Output sample clock
in_data0,... in_data3	Input	32	Input sample data
in_data4,... in_data7	Input	32	Input sample data (valid only in 8-channel mode)
manual_ratio_en	Input	1	Manual ratio enable signal
manual_ratio	Input	26	Manual ratio

Signal	I/O	Data Width	Description
			(4 bits integer, 22 bits decimal)
fifo_overflow	Output	1	FIFO overflow signal
out_locked	Output	1	Ratio lock signal
out_ratio	Output	26	Output ratio signal (4 bits integer, 22 bits decimal)
out_valid	Output	1	Data output valid signal
out_data0,... out_data3	Output	32	Output data
out_data4, ... out_data7	Output	32	Output data (valid only in 8-channel mode)

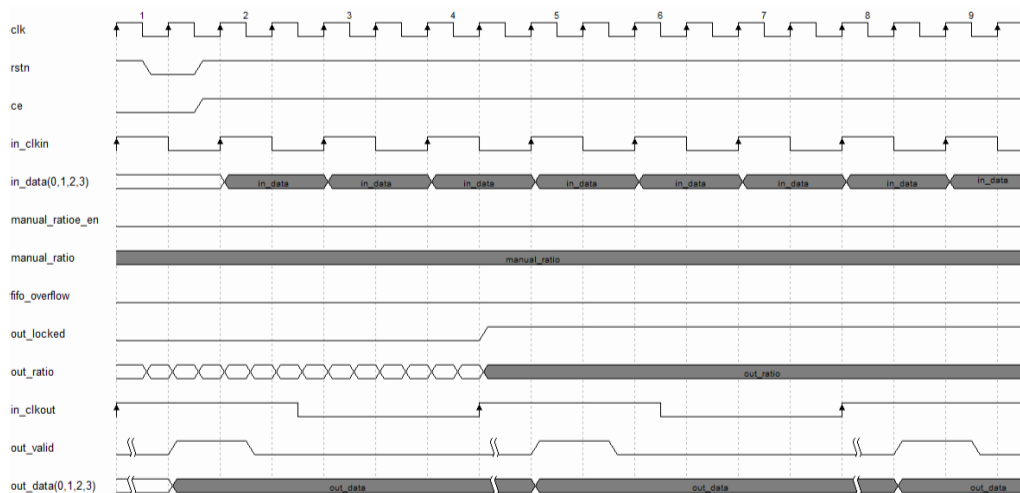
4.3 Timing Description

This section is to introduce the timing of ASRC.

4.3.1 ASRC Auto-detect Sampling Ratio Timing

The timing diagram of ASRC auto-detect sampling ratio is shown in Figure 4-3 .

Figure 4-3 Timing Diagram of ASRC Auto-detecting Sampling Ratio



The auto-detect sampling ratio (out_ratio) is performed by computing based on the input sampling clock (in_clkin) and the output sampling clock (in_clkout), and generating the output sampling ratio (out_ratio). When the lock signal (out_locked) is asserted high, the output sampling ratio is stable.

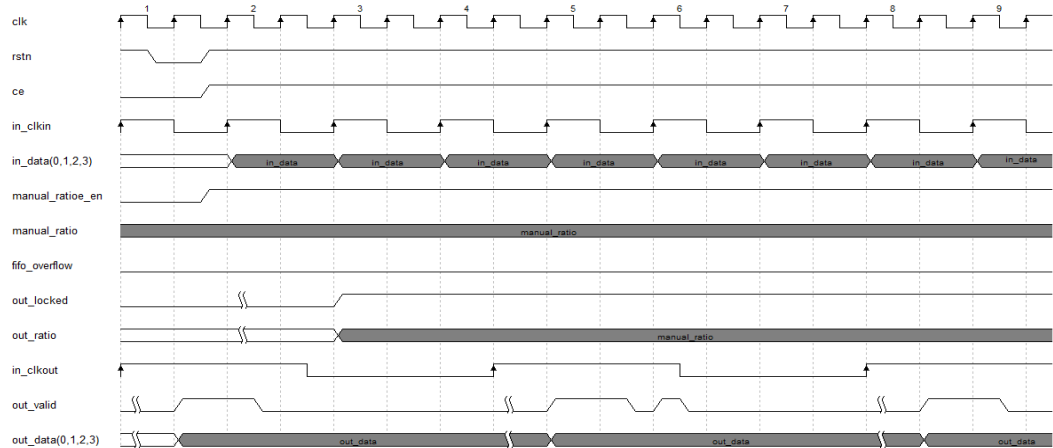
The sample input data (in_data) can be input through four channels or eight channels. After calculating, the sample output data (out_data) of each

channel is obtained.

4.3.2 ASRC Manual Sampling Ratio Timing

The timing diagram of ASRC manual sampling ratio is shown in Figure 4-4.

Figure 4-4 Timing Diagram of ASRC Manual Sampling Ratio



When `manual_ratio_en = 1`, the sampling ratio is manually configured. The conversion is performed using a fixed sampling ratio, and a fixed output sampling ratio is generated. In this mode, the lock signal (`out_locked`) is not meaningful.

The input sampled data (`in_data`) can be provided through four or eight channels. After a certain processing delay, the corresponding output sampled data (`out_data`) is generated for each channel.

4.3.3 Required Clock Frequencies for Different Conversions

Table 4-2 Required Clock Frequencies for Different Conversions (MHz) at a Maximum Sampling Frequency of 192 kHz

Input Clock Frequency	Output Clock Frequency			
	44.1 kHz	48 kHz	96 kHz	192 kHz
44.1 kHz	18	20	38	75
48 kHz	20	20	38	75
96 kHz	35	35	38	75
192 kHz	65	65	70	75

Table 4-3 Required Clock Frequencies for Different Conversions (MHz) at a Maximum Sampling Frequency of 384 kHz

Input Clock Frequency	Output Clock Frequency			
	48 kHz	96 kHz	192 kHz	384 kHz
48 kHz	11	22	43	85
96 kHz	14	22	43	85
192 kHz	20	27	43	85
384 kHz	31	39	54	85

When the maximum sampling frequency is set to 192 kHz:

- For upsampling, the minimum required system processing clock frequency is: $f_{clk} = f_{s_{out}} \times 390$
- For downsampling, the minimum required system processing clock frequency is: $f_{clk} = f_{s_{in}} \times 320 + f_{s_{out}} \times 70$

When the maximum sampling frequency is set to 384 kHz, the IP consumes more DSP resources to reduce the required system processing clock frequency:

- For upsampling, the minimum required system processing clock frequency is: $f_{clk} = f_{s_{out}} \times 220$
- For downsampling, the minimum required system processing clock frequency is: $f_{clk} = f_{s_{in}} \times 160 + f_{s_{out}} \times 60$

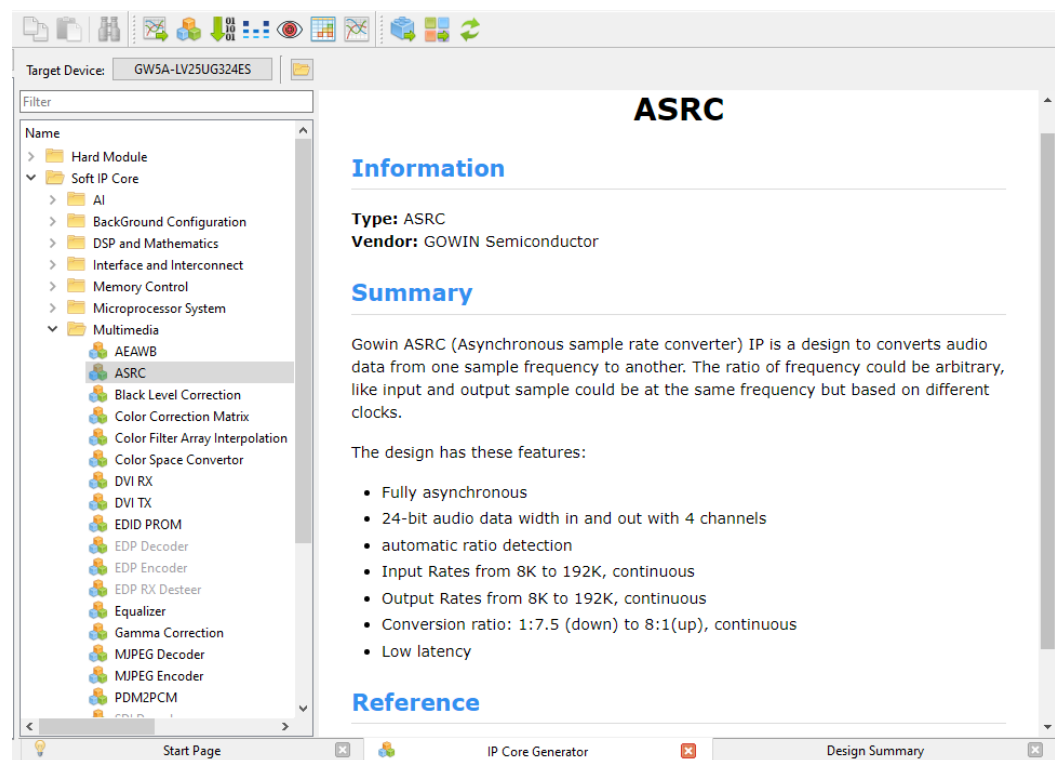
5 Interface Configuration

Select "Tools > IP Core Generator" in Gowin Software, and you can invoke and configure ASRC.

1. Open IP Core Generator

After creating a new project, you can click the "IP Core Generator", as shown in Figure 5-1.

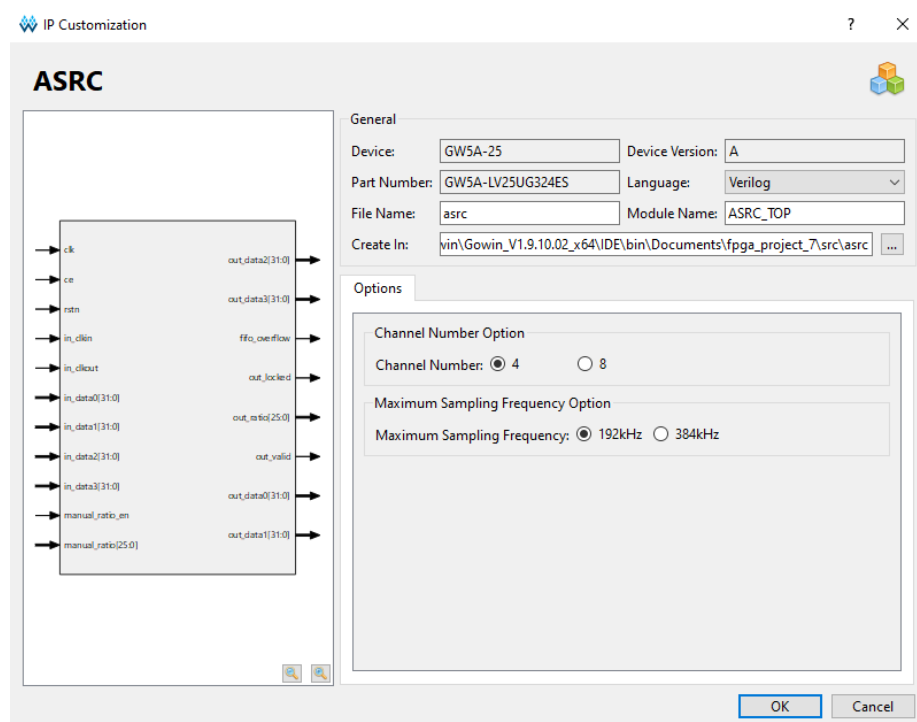
Figure 5-1 IP Core Generator Interface



2. Open ASRC IP Core

Click "Multimedia" and double click "ASRC" to open the interface, as shown in Figure 5-2.

Figure 5-2 Gowin ASRC IP Interface



This manual uses the GW5A-25 device and the GW5A-LV25UG324ES package as an example.

- The "Create In" option is used to specify the output directory for the generated IP core files. It can be modified by the user.
- The "File Name" option is used to specify the name of the generated IP configuration file. It can be modified by the user.
- The "Module Name" option is used to specify the name of the generated IP module. It can be modified by the user.

The IP configuration interface includes the "Channel Number" and "Maximum Sampling Frequency" configuration options, which can be set according to application requirements.

Table 5-1 Gowin ASRC IP Configuration Options

Option	Description
Channel Number	Number of channels
Maximum Sampling Frequency	Maximum supported sampling frequency

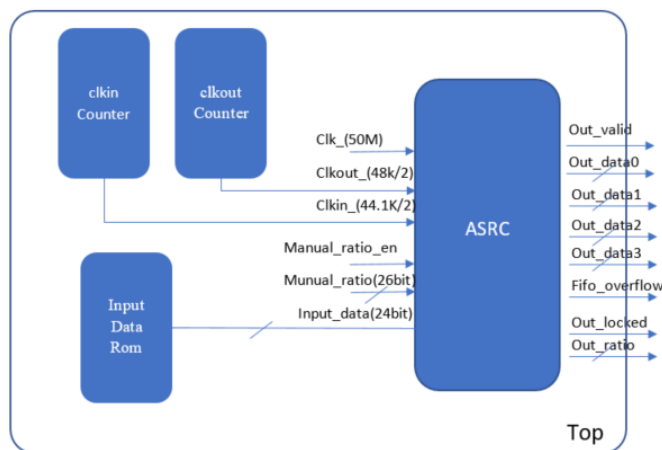
6 Reference Design

This chapter introduces the usage of ASRC reference design. The ASRC design instance has only one module. See the ASRC [reference design](#) for details.

The block diagram of reference design is as shown in Figure 6-1. In the design instance, the steps are as follows:

1. The input clock (48/2) KHz is generated through clk_in_counter.
2. The output clock (44.1/2) KHz is generated through clkout_counter.
3. The input data is stored in ROM and then transmitted to ASRC module.
4. After calculating by ASRC module, the output is obtained.

Figure 6-1 Block Diagram of Reference Design



ASRC functions can be verified using this design. When the reference design is applied to board level test, users need to provide appropriate incentive to the reference design and use an on-line logic analyzer or oscilloscope to observe the signal.

