DK_START_GW5A-LV25UG324_V2.0

User Guide

DBUG423-1.0E, 03/01/2024

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Revision History

Date	Version	Description
03/01/2024	1.0E	Initial version published.

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1 About This Guide

1.1 Purpose

The DK_START_GW5A-LV25UG324_V2.0 development board (hereinafter referred to as “the development board”) user guide consists of following three parts:

- A brief introduction to the features of the development board.
- An introduction to the development board system architecture and hardware resources
- An introduction to the hardware circuits, functions and pinout

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- DS1103, GW5A series of FPGA Products Data Sheet
- UG985, GW5A-25 Pinout
- UG1101, GW5A series of FPGA Products Package and Pinout User Guide
- UG290, Gowin FPGA Products Programming and Configuration Guide
- SUG100, Gowin Software User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
ADC	Analog-to-digital Converter
DDR	Double Data Rate
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable I/O
JTAG	Joint Test Action Group
LDO	Low Dropout Regulator
LVDS	Low-Voltage Differential Signaling
MIPI	Mobile Industry Processor Interface
PMIC	Power Management Integrated Circuit

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

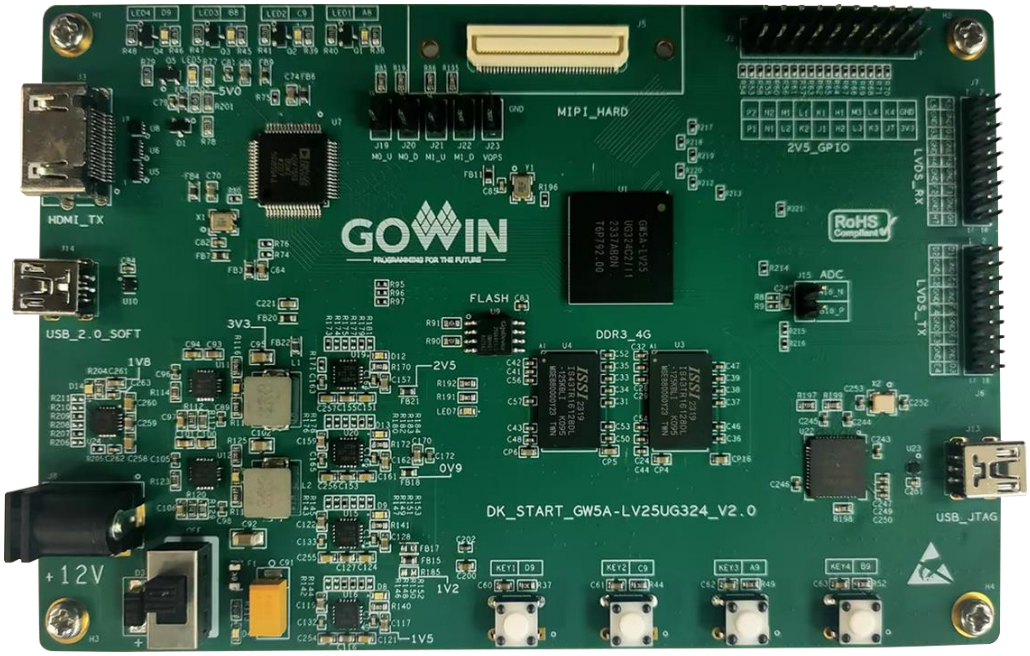
Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Development Board Introduction

2.1 Overview

Figure 2-1 DK_START_GW5A-LV25UG324_V2.0 Development Board



DK_START_GW5A-LV25UG324_V2.0 development board applies to DDR3 high-speed data storage, MIPI, LVDS high-speed communication, ADC, HDMI_TX communication, USB 2.0 communication, hardware verification, and software learning and debugging, etc.

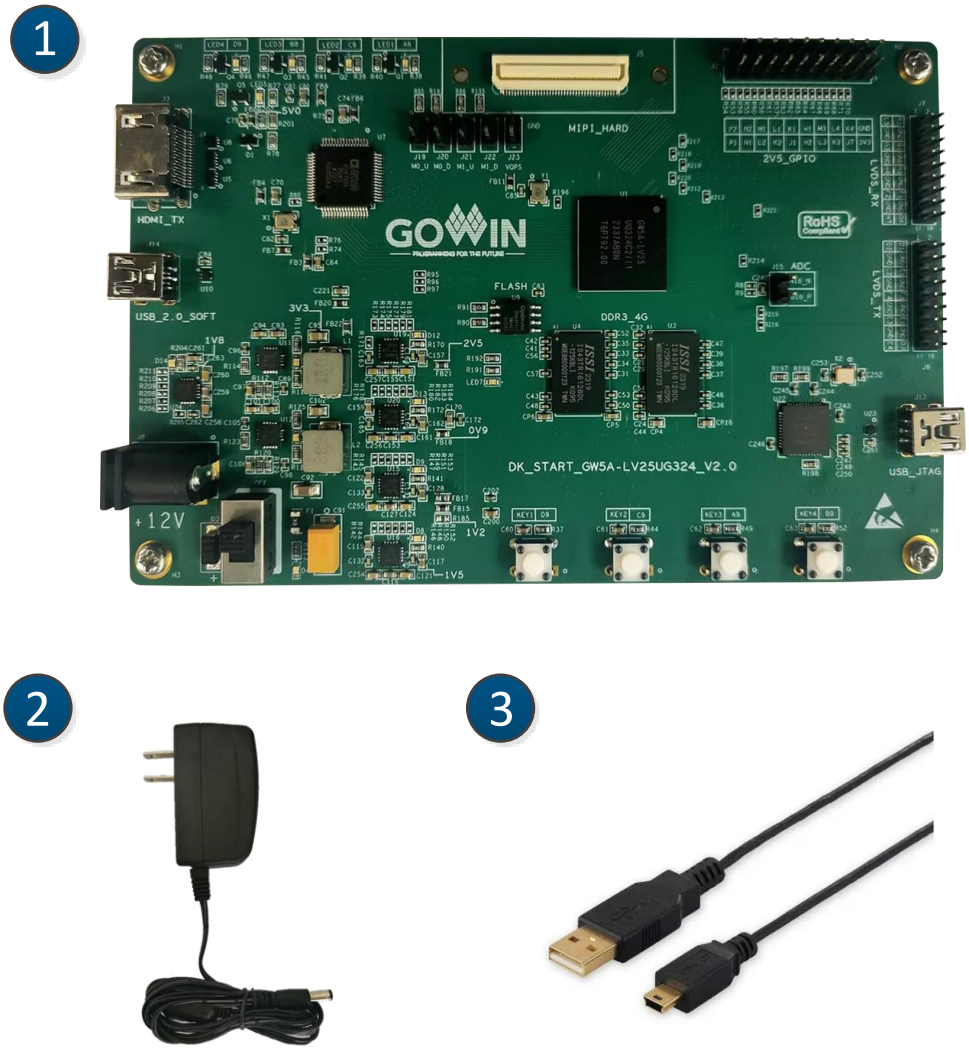
The development board adopts Gowin GW5A-LV25UG324 FPGA device. For the internal resources of the chip, see *DS1103, GW5A series of FPGA Products Data Sheet*.

2.2 A Development Board Kit

The development board kit includes the following items:

1. DK_START_GW5A-LV25UG324_V2.0 development board
2. 12V power (Input: AC 100-240V~50/60Hz 0.6A, output: DC12V 2A)
3. Mini USB-B Cable

Figure 2-2 A Development Board Kit



① DK_START_GW5A-LV25UG324_V2.0 development board

② 12V power supply adapter

③ Mini USB-B Cable

2.3 PCB Components

Figure 2-3 PCB Components

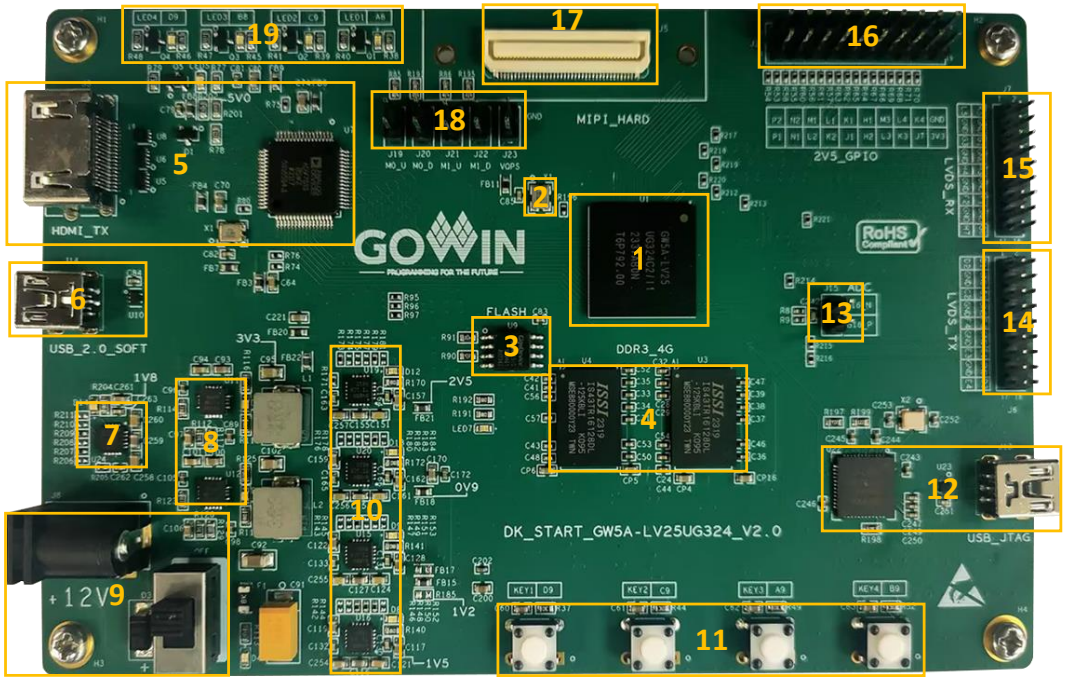


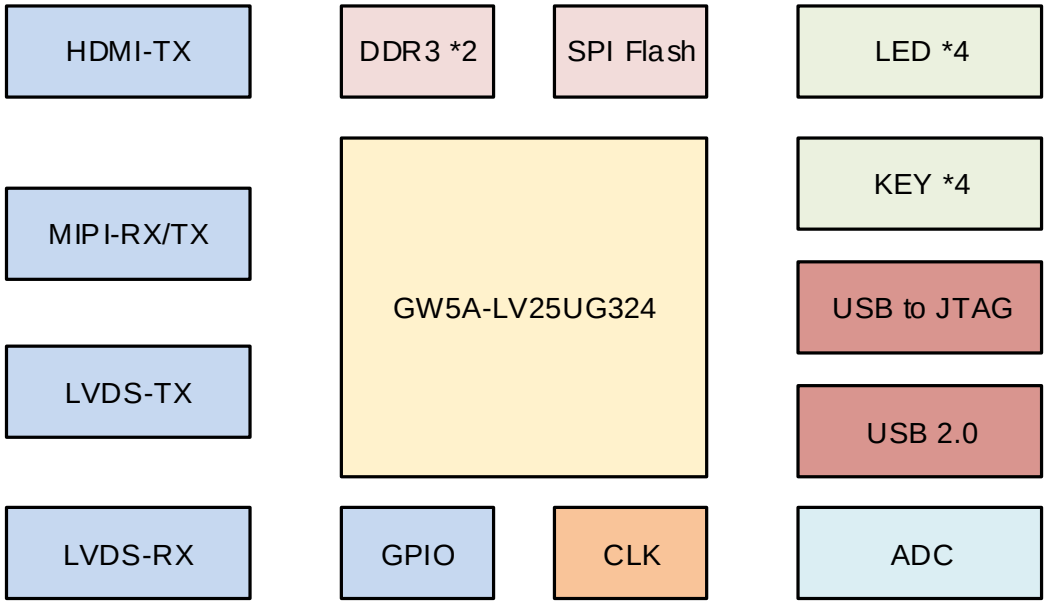
Table 2-1 PCB Components

Number	Description
1	GW5A-LV25UG324, FPGA
2	50M clock crystal oscillator
3	64Mbit SPI Flash
4	4Gbit DDR3 SDRAM
5	HDMI_TX interface
6	USB 2.0 Interface
7	LDO power conversion chip
8	DC-DC power conversion chip
9	+12V power supply
10	LDO power conversion chip
11	4*Switch
12	Mini USB download interface
13	ADC input interfaces
14	4 lane + 1 clk, LVDS_TX interface

Number	Description
15	4 lane + 1 clk, LVDS_RX interface
16	18*GPIO
17	MIPI_RX/TX hard core (4 lane + 1 clk) and 4 GPIOs
18	Mode Selection
19	4*LED

2.4 System Block Diagram

Figure 2-4 System Block Diagram



2.5 Features

The key features are as follows:

- FPGA Device
  - The development board adopts GW5A-LV25UG324 FPGA device, which is the fifth generation products of Gowin Arora family.
  - Max. user I/O: 239
- Download and Boot
  - Integrate USB download circuit on the board, download through Mini USB-B interface
  - External SPI Flash boot
  - The DONE light is on after loading
- Power Supply
  - External DC12V/2A Power
  - The POWER light is on after power on

  - The board generates 0.9V, 1.2V, 1.5V, 1.8V, 2.1V, 2.5V, 3.3V, 5V voltage.
- System Clock
  - 50MHz clock
- Memory device
  - 4Gbit DDR3 SDRAM
  - 64Mbit Quad SPI Flash Memory
- LVDS interface
  - LVDS_TX interface, single channel, includes 4 data + 1 clk
  - LVDS_RX interface, single channel, includes 4 data + 1 clk
- MIPI interface
  - MIPI_RX/TX hard core, single channel, includes 4 data + 1 clk
  - 4 GPIOs
  - 3.3V power supply
  - Use connector with 80 contacts and 0.5mm pitch
- ADC
  - 1 ADC interface
  - The interface uses 1x2p pins.
  - The ADC differential input is designed with an anti-aliasing filter.
- Key & LED
  - 4 keys
  - 4 LEDs
- HDMI interface
  - 1 HDMI-TX interface
- USB 2.0 Interface
  - Mini USB-B interface with electrostatic protection
- GPIO interface
  - 18 GPIOs with 2.5V

3 Development Board Circuit

3.1 FPGA

Overview

For the resources of GW5A series of FPGA Products, refer to *DS1103, GW5A series of FPGA products*.

I/O BANK Introduction

For the I/O BANK, package, and pinout information, see *UG1101, GW5A Series of FPGA Products Package and Pinout User Guide* for more details.

3.2 Power Supply

3.2.1 Introduction

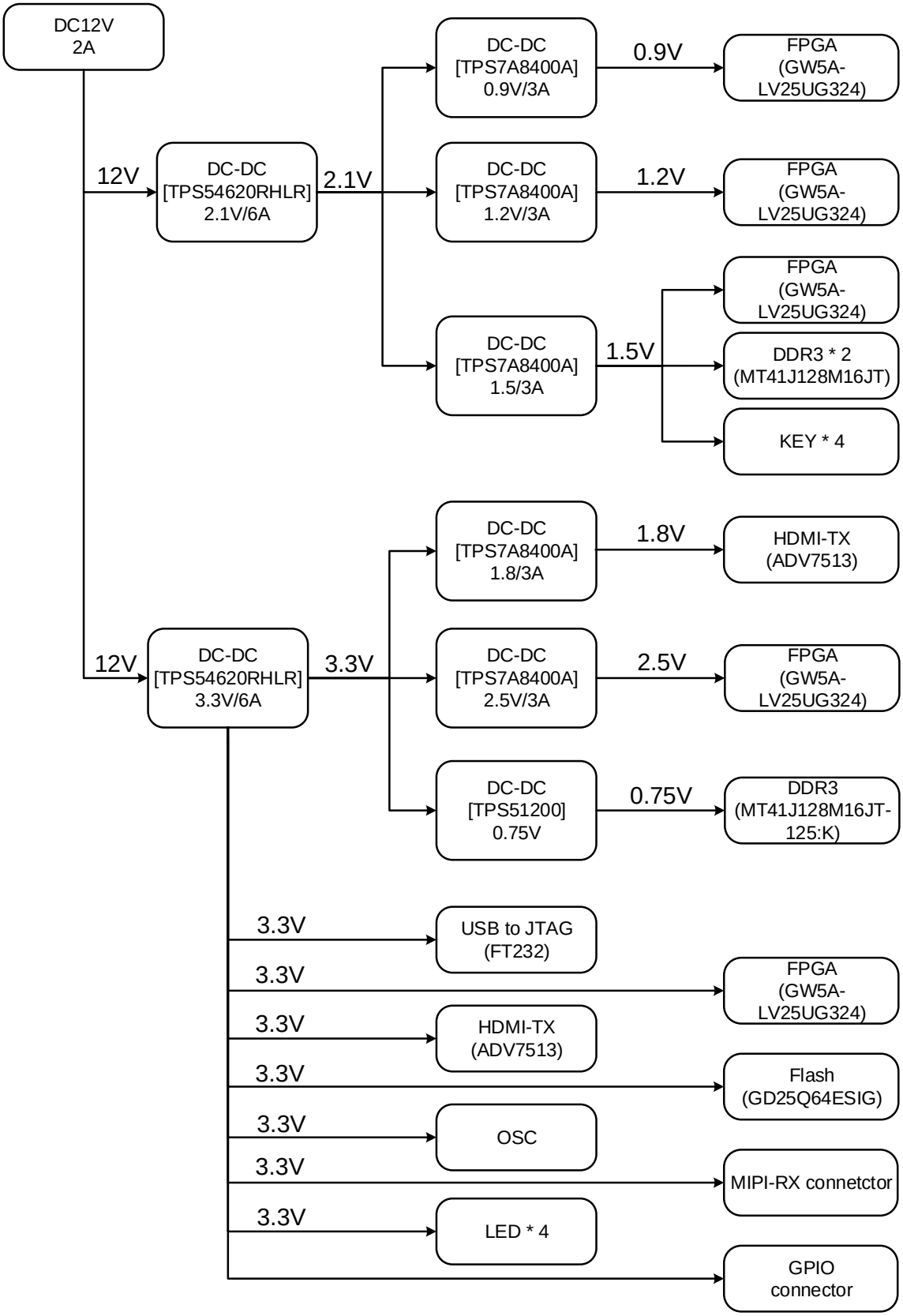
The development board needs to be powered by a 12V power adapter.

The input parameter of the adapter is AC 100-240V~50/60MHz 0.6A, and the output parameter is DC 12V 2A.

The input 12V power is regulated by the PMIC on the development board to generate 0.9V, 1.2V, 1.5V, 1.8V, 2.1V, 2.5V, and 3.3V power supplies.

3.2.2 Power Distribution

Figure 3-1 Power Distribution Diagram



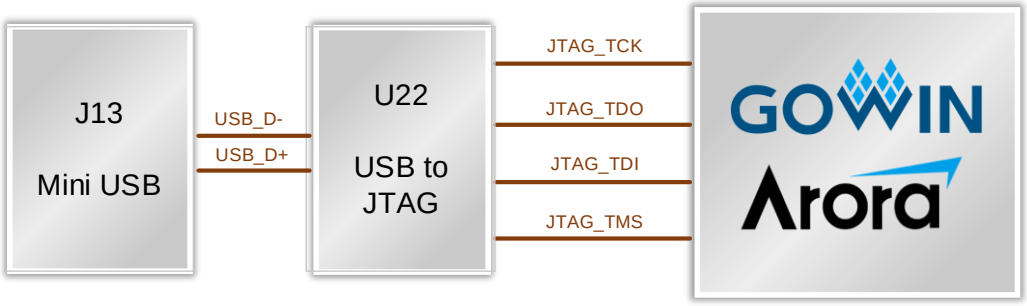
3.3 Download Module

3.3.1 Introduction

The DK_START_GW5A-LV25UG324_V2.0 development board has a Mini USB-B download interface (J13) designed to program the programs to external SPI FLASH or download them to SRAM.

The download connection diagram is show in Figure 3-2.

Figure 3-2 Connection Diagram of Download



3.3.2 Pin Distribution

Table 3-1 JTAG Pinout

Signal Name	FPGA (U1) Pin No.	BANK	I/O Level	Description
JTAG_TCK	A17	10	3.3V	JTAG signals
JTAG_TDO	D16	10	3.3V	
JTAG_TDI	D15	10	3.3V	
JTAG_TMS	B18	10	3.3V	

Table 3-2 J13 Pin Distribution for Mini USB Interface

J13 Pin No.	Signal Name	FPGA (U1) Pin No.	BANK	I/O Level	Description
1	VSLA_5P0	--	--	5V	Power
2	USB_D-	--	--	3.3V	USB- signal
3	USB_D+	--	--	3.3V	USB+ signal
4	NC	--	--	--	Floating
5	GND	--	--	--	GND
6	GND	--	--	--	GND

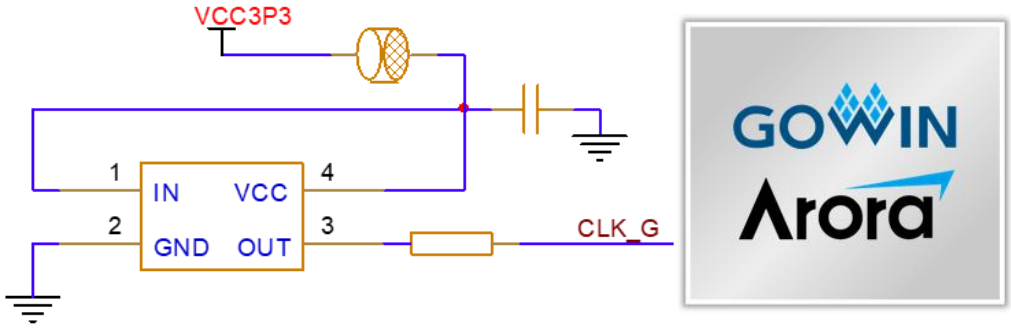
J13 Pin No.	Signal Name	FPGA (U1) Pin No.	BANK	I/O Level	Description
7	GND	--	--	--	GND
8	GND	--	--	--	GND
9	GND	--	--	--	GND

3.4 Clock

3.4.1 Introduction

50MHz single-ended clock signal is introduced to the FPGA clock source. The clock pinout is as shown in Table 3-3.

Figure 3-3 Clock Connection Diagram



3.4.2 Pin Distribution

Table 3-3 Clock Pinout

Signal Name	FPGA (U1) Pin No.	BANK	I/O Level	Description
CLK_G	T9	4	3.3V	Frequency 50MHz

3.5 DDR3

3.5.1 Introduction

DK_START_GW5A-LV25UG324_V2.0 development board includes two 2Gbit DDR3 chips. The signals of DDR3 chip is connected to the BANK1, BANK2, and BANK3 of FPGA. The specific configurations of DDR3 are as shown in Table 3-4.

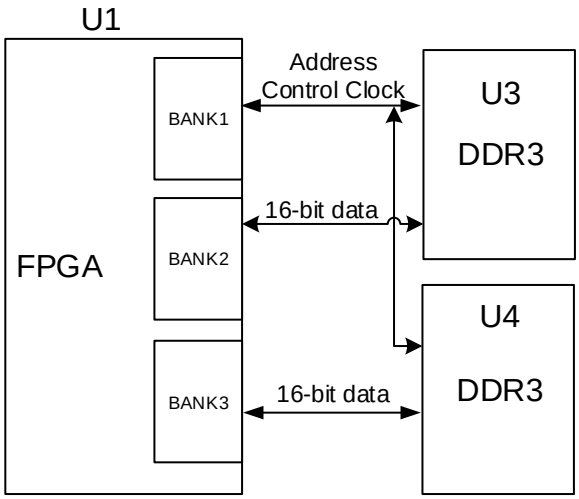
Table 3-4 DDR3 Configuration

Designator	Capacity
U3	128M x 16bit
U4	128M x 16bit

DDR3 hardware design requires strict consideration of signal integrity. In the design of circuit and PCB, matching resistor/termination resistor, impedance control and equal length control of traces have been fully considered to ensure DDR3 works stably at high speed.

The hardware connection diagram of DDR3 is as show in Figure 3-4.

Figure 3-4 Hardware Connection Diagram of DDR3



3.5.2 Pin Distribution

Table 3-5 DDR3 Pinout

Signal Name	FPGA (U1) Pin No.	BANK	I/O Level	Description
DDR3_A0	B11	1	1.5V	Address
DDR3_A1	A10	1	1.5V	Address
DDR3_A2	C11	1	1.5V	Address
DDR3_A3	F11	1	1.5V	Address
DDR3_A4	A14	1	1.5V	Address
DDR3_A5	G11	1	1.5V	Address
DDR3_A6	C12	1	1.5V	Address
DDR3_A7	F10	1	1.5V	Address

Signal Name	FPGA (U1) Pin No.	BANK	I/O Level	Description
DDR3_A8	A12	1	1.5V	Address
DDR3_A9	C10	1	1.5V	Address
DDR3_A10	F12	1	1.5V	Address
DDR3_A11	A11	1	1.5V	Address
DDR3_A12	D12	1	1.5V	Address
DDR3_A13	G9	1	1.5V	Address
DDR3_BA0	B14	1	1.5V	Bank address
DDR3_BA1	E12	1	1.5V	Bank address
DDR3_BA2	D11	1	1.5V	Bank address
DDR3_CSn	E13	1	1.5V	Chip select
DDR3_CASn	F13	1	1.5V	Column address strobe
DDR3_CK_EN	A13	1	1.5V	Clock Enable
DDR3_ODT	E11	1	1.5V	On-die Termination Enable
DDR3_RASn	C15	1	1.5V	Row address strobe
DDR3_RSTn	F9	1	1.5V	Reset
DDR3_WEn	C13	1	1.5V	Write enable
DDR3_CKn	C14	1	1.5V	Differential clock
DDR3_CKp	D14	1	1.5V	Differential clock
DDR3_DQ0	E18	2	1.5V	Data
DDR3_DQ1	F15	2	1.5V	Data
DDR3_DQ2	E16	2	1.5V	Data
DDR3_DQ3	F14	2	1.5V	Data
DDR3_DQ4	H13	2	1.5V	Data
DDR3_DQ5	C17	2	1.5V	Data
DDR3_DQ6	F16	2	1.5V	Data
DDR3_DQ7	C18	2	1.5V	Data
DDR3_DQ8	G16	2	1.5V	Data
DDR3_DQ9	K12	2	1.5V	Data

Signal Name	FPGA (U1) Pin No.	BANK	I/O Level	Description
DDR3_DQ10	F17	2	1.5V	Data
DDR3_DQ11	L12	2	1.5V	Data
DDR3_DQ12	G18	2	1.5V	Data
DDR3_DQ13	L13	2	1.5V	Data
DDR3_DQ14	F18	2	1.5V	Data
DDR3_DQ15	K13	2	1.5V	Data
DDR3_LDM	G14	2	1.5V	Data input mask
DDR3_UDM	H15	2	1.5V	Data input mask
DDR3_LDQSp	D17	2	1.5V	Data Clock
DDR3_LDQSn	D18	2	1.5V	Data Clock
DDR3_UDQSp	J13	2	1.5V	Data Clock
DDR3_UDQSn	K14	2	1.5V	Data Clock
DDR3_DQ16	L18	3	1.5V	Data
DDR3_DQ17	L15	3	1.5V	Data
DDR3_DQ18	M18	3	1.5V	Data
DDR3_DQ19	J16	3	1.5V	Data
DDR3_DQ20	L17	3	1.5V	Data
DDR3_DQ21	H18	3	1.5V	Data
DDR3_DQ22	M16	3	1.5V	Data
DDR3_DQ23	H17	3	1.5V	Data
DDR3_DQ24	P17	3	1.5V	Data
DDR3_DQ25	T17	3	1.5V	Data
DDR3_DQ26	N17	3	1.5V	Data
DDR3_DQ27	N14	3	1.5V	Data
DDR3_DQ28	P18	3	1.5V	Data
DDR3_DQ29	U17	3	1.5V	Data
DDR3_DQ30	N18	3	1.5V	Data
DDR3_DQ31	U18	3	1.5V	Data
DDR3_LDM_1	L16	3	1.5V	Data input mask

Signal Name	FPGA (U1) Pin No.	BANK	I/O Level	Description
DDR3_UDM_1	T18	3	1.5V	Data input mask
DDR3_LDQSp_1	K17	3	1.5V	Data Clock
DDR3_LDQSn_1	K18	3	1.5V	Data Clock
DDR3_UDQSp_1	N15	3	1.5V	Data Clock
DDR3_UDQSn_1	N16	3	1.5V	Data Clock

3.6 SPI Flash

3.6.1 Introduction

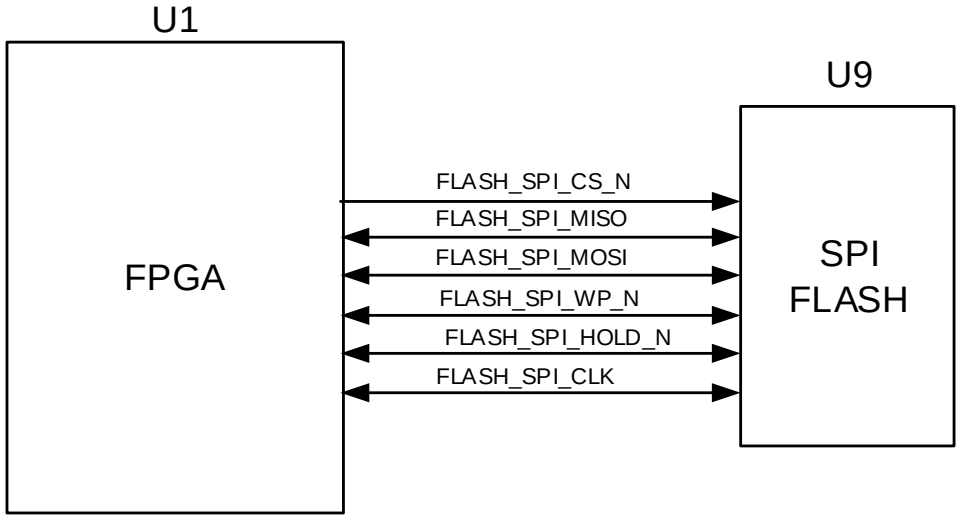
The DK_START_GW5A-LV25UG324_V2.0 development board includes an SPI Flash memory chip with the memory capacity of 64Mbit. The FPGA program is programmed into the SPI FLASH and the FPGA chip loads the program in the SPI Flash through the MSPI interface when powered up. The specific configurations of SPI FLASH are as shown in Table 3-6.

Table 3-6 Specific Configurations of SPI FLASH

Designator	Capacity
U9	64M Bit

The SPI Flash is connected to the dedicated pins in BANK4 on the FPGA chip. Figure 3-5 is the hardware connection diagram of SPI Flash.

Figure 3-5 Hardware Connection Diagram of SPI Flash



3.6.2 Pin Distribution

Table 3-7 Flash Pinout

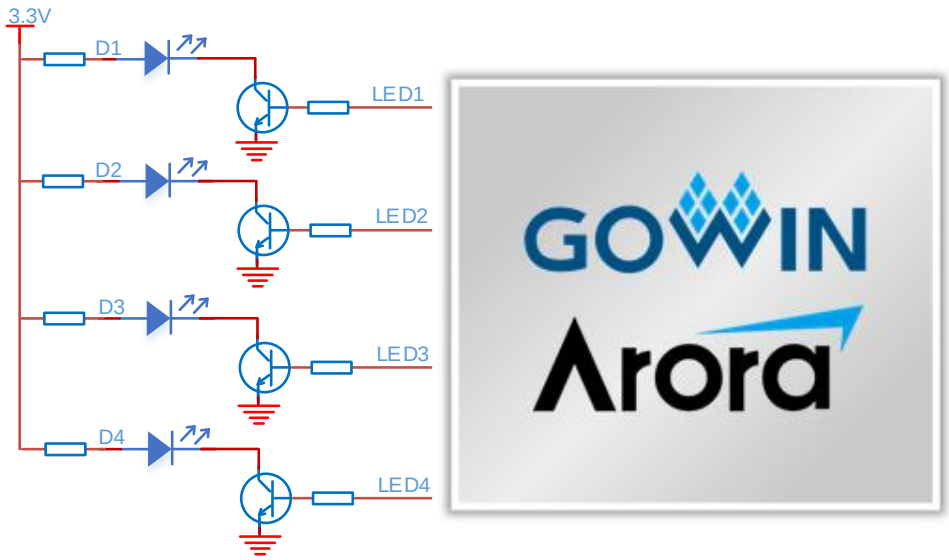
Signal Name	FPGA (U1) Pin No.	BANK	I/O Level	Description
FLASH_SPI_CLK	R15	4	3.3V	Clock signal
FLASH _SPI_CS_N	V3	4	3.3V	Chip select signal
FLASH_SPI_MISO	R13	4	3.3V	Serial data input
FLASH_SPI_MOSI	T13	4	3.3V	Serial data output
FLASH_SPI_WP_N	T14	4	3.3V	Write protection signal
FLASH_SPI_HOLD_N	V14	4	3.3V	Clock lock

3.7 LED & Key

3.7.1 Introduction

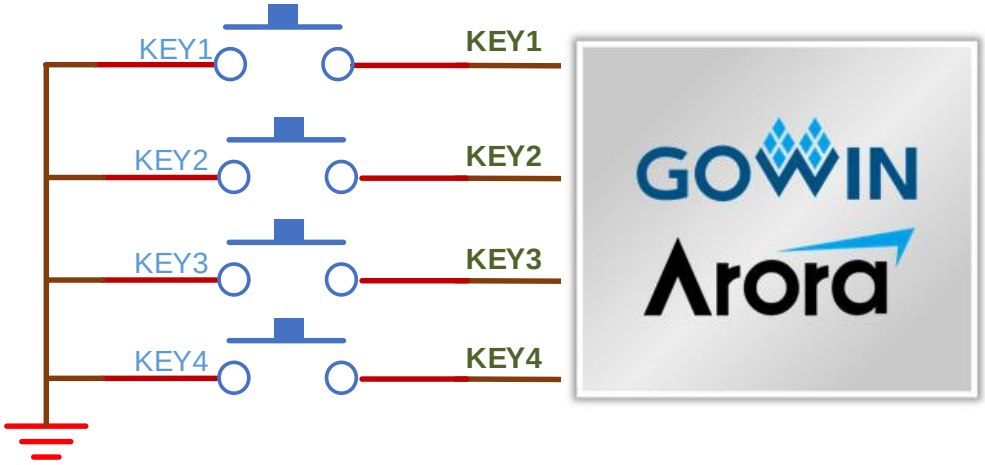
The DK_START_GW5A-LV25UG324_V2.0 development board includes four user LEDs. The user LEDs are connected to the IO of FPGA BANK0 and can be switched on and off via the program. The user LEDs will be on when the IO voltage is high. The user LEDs will be off when the IO voltage is low. The connection diagram is shown in Figure 3-6.

Figure 3-6 Connection Diagram of LED



There are four user keys on the development board. The user keys are respectively connected to the general IO of FPGA BANK0. The corresponding IO input voltage of the FPGA is low when the key is pressed while high when the key is not pressed. The key circuit has a hardware dithering function. The connection diagram is shown in Figure 3-7.

Figure 3-7 Key Connection Diagram



3.7.2 Pin Distribution

Table 3-8 LED Pinout

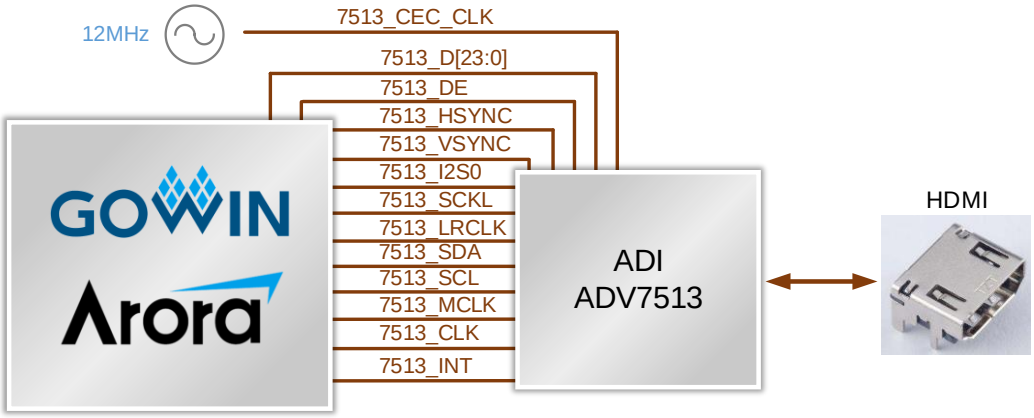
Signal Name	FPGA (U1) Pin No.	BANK	I/O Level	Description
LED1	A8	0	1.5V	LED
LED2	A7	0	1.5V	LED
LED3	B8	0	1.5V	LED
LED4	C8	0	1.5V	LED
KEY1	D9	0	1.5V	Key
KEY2	C9	0	1.5V	Key
KEY3	A9	0	1.5V	Key
KEY4	B9	0	1.5V	Key

3.8 HDMI_TX Interface

3.8.1 Introduction

The DK_START_GW5A-LV25UG324_V2.0 development board includes HDMI_TX interface. The HDMI_TX interface uses ADI encoding chip of ADV7513BSWZ. The connection diagram is as shown in Figure 3-8.

Figure 3-8 Connection Diagram of FPGA and HDMI Interface



3.8.2 Pin Distribution

Table 3-9 HDMI_TX Module Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
7513_CLK	V8	5	3.3V	The RGB data row-locked output clock
7513_D0	P6	5	3.3V	RGB data signal
7513_D1	P7	5	3.3V	RGB data signal
7513_D2	M8	5	3.3V	RGB data signal
7513_D3	U5	5	3.3V	RGB data signal
7513_D4	V5	5	3.3V	RGB data signal
7513_D5	V6	5	3.3V	RGB data signal
7513_D6	U7	5	3.3V	RGB data signal
7513_D7	V7	5	3.3V	RGB data signal
7513_D8	U8	5	3.3V	RGB data signal
7513_D9	T6	5	3.3V	RGB data signal

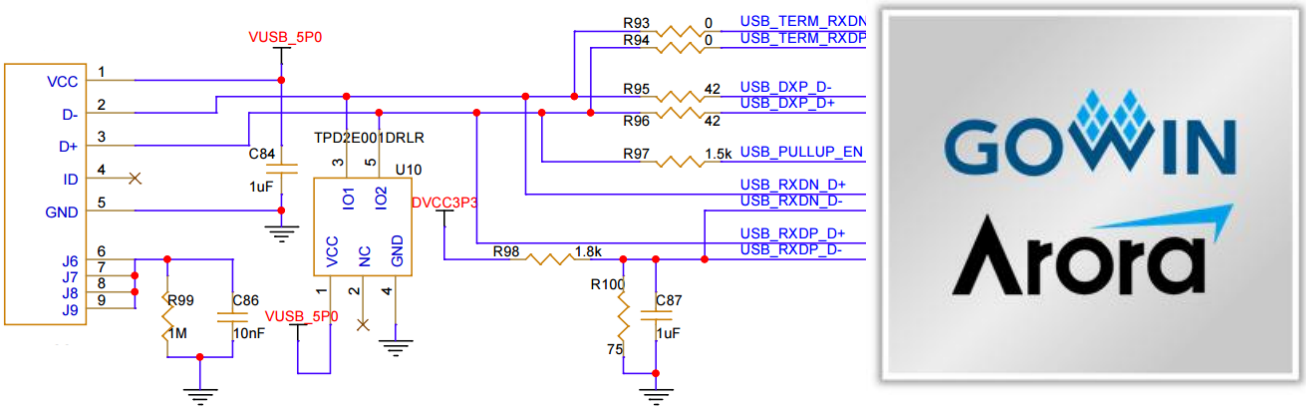
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
7513_D10	R7	5	3.3V	RGB data signal
7513_D11	T7	5	3.3V	RGB data signal
7513_D12	P8	5	3.3V	RGB data signal
7513_D13	N8	5	3.3V	RGB data signal
7513_D14	N9	5	3.3V	RGB data signal
7513_D15	M10	5	3.3V	RGB data signal
7513_D16	M11	4	3.3V	RGB data signal
7513_D17	V12	4	3.3V	RGB data signal
7513_D18	V13	4	3.3V	RGB data signal
7513_D19	U13	4	3.3V	RGB data signal
7513_D20	V15	4	3.3V	RGB data signal
7513_D21	U15	4	3.3V	RGB data signal
7513_D22	V16	4	3.3V	RGB data signal
7513_D23	U16	4	3.3V	RGB data signal
7513_VSYNC	T5	5	3.3V	Vertical Sync output signal
7513_HSYNC	N5	5	3.3V	Horizontal Sync output signal
7513_DE	N6	5	3.3V	RGB data enable
7513_SCLK	T3	5	3.3V	Audio Serial Clock
7513_LRCLK	R3	5	3.3V	Audio left/right clock
7513_MCLK	R5	5	3.3V	Audio master clock
7513_IIS0	T4	5	3.3V	Audio output pin
7513_SCL	R11	4	3.3V	I2C serial interface clock
7513_SDA	N11	4	3.3V	I2C serial interface data
7513_INT	T11	4	3.3V	Interrupt signal

3.9 USB 2.0 Interface

3.9.1 Introduction

The DK_START_GW5A-LV25UG324_V2.0 development board implements the USB 2.0 interface through the Mini USB-B connector, featuring ESD protection circuit designed for communication between the FPGA and external devices.

Figure 3-9 USB 2.0 Schematic Connection Diagram



3.9.2 Pin Distribution

Table 3-10 USB 2.0 Interface Pin Distribution

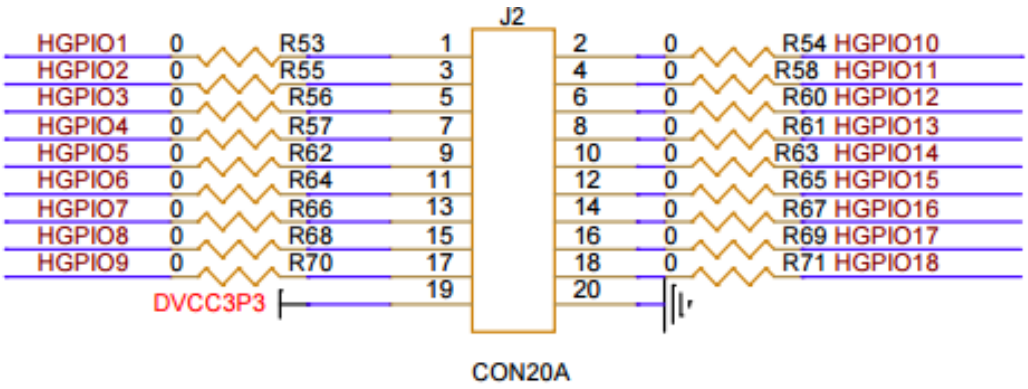
Signal Name	FPGA (U1) Pin No.	BANK	IO Level	Description
USB_TERM_RXDN	P11	4	3.3V	Terminal resistance control at high speed, USB data pin at full speed and low speed
USB_TERM_RXDP	N10	4	3.3V	Terminal resistance control at high speed, USB data pin at full speed and low speed
USB_DXP_D-	V10	4	3.3V	USB data pin at high speed
USB_DXP_D+	U10	4	3.3V	USB data pin at high speed
USB_PULLUP_EN	T12	4	3.3V	Pull-up
USB_RXDN_D+	R10	4	3.3V	USB- signal
USB_RXDN_D-	T10	4	3.3V	USB+ Reference signal
USB_RXDP_D+	U11	4	3.3V	USB+ signal
USB_RXDP_D-	V11	4	3.3V	USB- Reference signal

3.10 GPIO

3.10.1 Introduction

The DK_START_GW5A-LV25UG324_V2.0 development board routes out 18 2.5V GPIOs through the double-row pin header with 2.54mm pitch.

Figure 3-10 Schematic Connection Diagram of GPIO



3.10.2 Pin Distribution

Table 3-11 GPIO Pinout

Signal Name	FPGA (U1) Pin No.	BANK	IO Level
HGPIO1	P1	6	2.5V
HGPIO2	N1	6	2.5V
HGPIO3	L2	6	2.5V
HGPIO4	K2	6	2.5V
HGPIO5	J1	6	2.5V
HGPIO6	H2	6	2.5V
HGPIO7	L3	6	2.5V
HGPIO8	K3	6	2.5V
HGPIO9	J7	7	2.5V
HGPIO10	P2	6	2.5V
HGPIO11	N2	6	2.5V
HGPIO12	M1	6	2.5V
HGPIO13	L1	6	2.5V
HGPIO14	K1	6	2.5V

Signal Name	FPGA (U1) Pin No.	BANK	IO Level
HGPIO15	H1	6	2.5V
HGPIO16	M3	6	2.5V
HGPIO17	L4	6	2.5V
HGPIO18	K4	6	2.5V

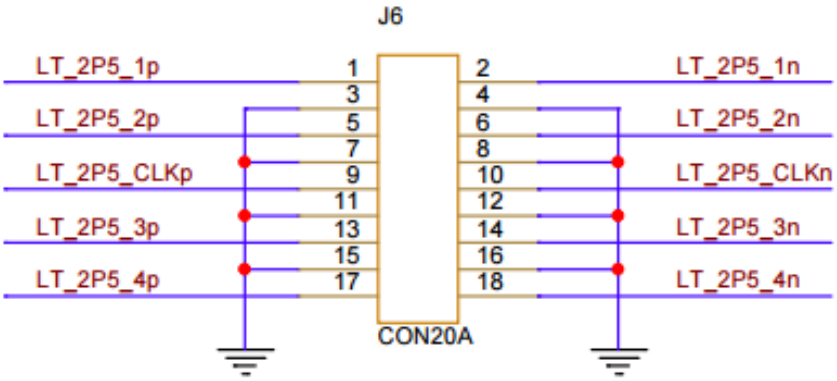
3.11 LVDS Interface

3.11.1 Introduction

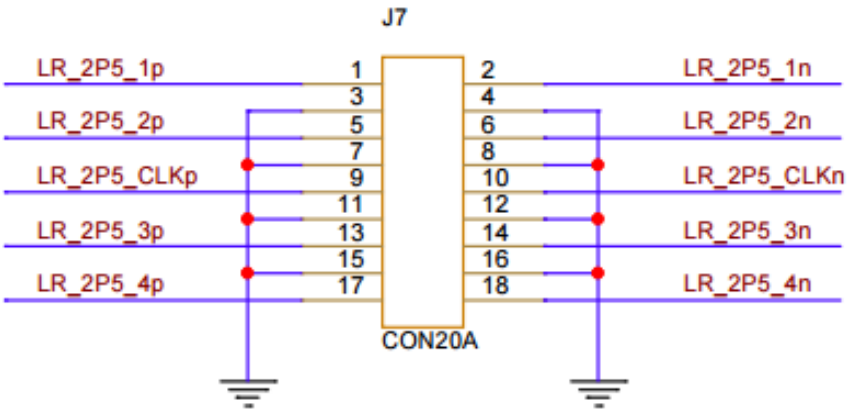
The DK_START_GW5A-LV25UG324_V2.0 development board includes an LVDS transceiver connector, both in the form of 2x9P pin headers with 2.0mm pitch. LVDS_TX contains: 4 data + 1 clk; LVDS_RX contains: 4 data + 1 clk.

Figure 3-11 Connection Diagram of LVDS Interface Schematic

LVDS_TX:



LVDS_RX:



3.11.2 Pin Distribution

Table 3-12 LVD_TX Interface Pin Distribution

Signal Name	FPGA (U1) Pin No.	BANK	I/O Level	Description
LT_2P5_1p	D2	7	2.5V	LVDS data
LT_2P5_1n	D1	7	2.5V	LVDS data
LT_2P5_2p	C2	7	2.5V	LVDS data
LT_2P5_2n	C1	7	2.5V	LVDS data
LT_2P5_CLKp	F4	7	2.5V	LVDS Clock
LT_2P5_CLKn	F3	7	2.5V	LVDS Clock
LT_2P5_3p	E3	7	2.5V	LVDS data
LT_2P5_3n	E1	7	2.5V	LVDS data
LT_2P5_4p	E4	7	2.5V	LVDS data
LT_2P5_4n	D3	7	2.5V	LVDS data

Table 3-13 LVD_RX Interface Pin Distribution

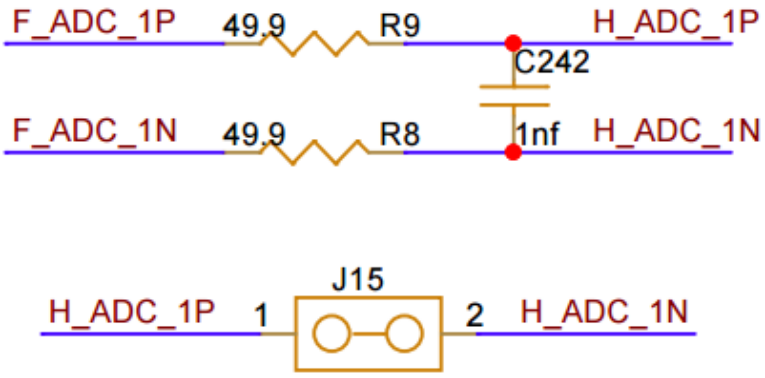
Signal Name	FPGA (U1) Pin No.	BANK	I/O Level	Description
LR_2P5_1p	L5	7	2.5V	LVDS data
LR_2P5_1n	K5	7	2.5V	LVDS data
LR_2P5_2p	G3	7	2.5V	LVDS data
LR_2P5_2n	G1	7	2.5V	LVDS data
LR_2P5_CLKp	H4	7	2.5V	LVDS Clock
LR_2P5_CLKn	H3	7	2.5V	LVDS Clock
LR_2P5_3p	F2	7	2.5V	LVDS data
LR_2P5_3n	F1	7	2.5V	LVDS data
LR_2P5_4p	H7	7	2.5V	LVDS data
LR_2P5_4n	G6	7	2.5V	LVDS data

3.12 ADC interface

3.12.1 Introduction

The DK_START_GW5A-LV25UG324_V2.0 development board includes input interfaces for ADC signal. The connector uses a 1x2P pin header with 2.54mm pitch. Figure 3-12 is the ADC schematic connection diagram and the anti-aliasing filter circuit.

Figure 3-12 ADC Schematic



3.12.2 Pin Distribution

Table 3-14 ADC Signal Input Pin Distribution

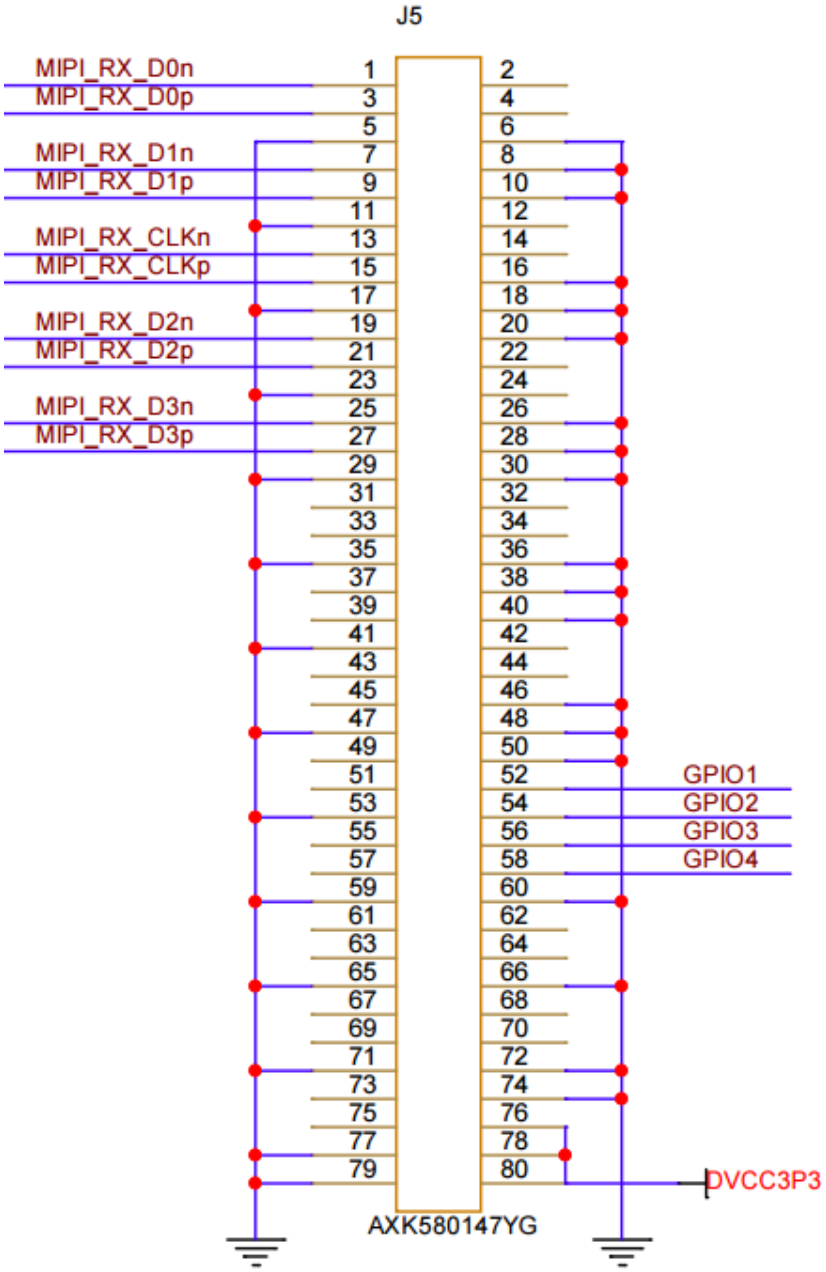
Signal Name	FPGA (U1) Pin No.	BANK	IO Level	Description
H_ADC_1P	B16	1	1.5V	Analog signal input
H_ADC_1N	A16	1	1.5V	Analog signal input

3.13 MIPI

3.13.1 Introduction

The MIPI interface on the development board uses the 80pin AXK580147YG connector with 0.5mm pitch. Lead out MIPI_RX/TX hard core signals (4 data + 1 clk) and 4 GPIOs from FPGA. In addition, the connector provides 3.3V power. The schematic circuit is as shown in Figure 3-13.

Figure 3-13 Schematic Circuit of MIPI Interface



3.13.2 Pin Distribution

Table 3-15 MIPI Interface Pinout

Signal Name	FPGA (U1) Pin No.	BANK	I/O Level	Description
MIPI_RX_D0n	T1	MIPI	-	MIPI data signal
MIPI_RX_D0p	T2	MIPI	-	MIPI data signal
MIPI_RX_D1n	U1	MIPI	-	MIPI data signal
MIPI_RX_D1p	U2	MIPI	-	MIPI data signal
MIPI_RX_CLKn	M5	MIPI	-	MIPI clock signal
MIPI_RX_CLKp	L6	MIPI	-	MIPI clock signal
MIPI_RX_D2n	N3	MIPI	-	MIPI data signal
MIPI_RX_D2p	N4	MIPI	-	MIPI data signal
MIPI_RX_D3n	P3	MIPI	-	MIPI data signal
MIPI_RX_D3p	P4	MIPI	-	MIPI data signal
GPIO1	F6	7	2.5V	GPIO
GPIO2	J6	7	2.5V	GPIO
GPIO3	K6	7	2.5V	GPIO
GPIO4	L7	7	2.5V	GPIO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