Mitigating Single-Event Upsets (SEUs) in FPGAs-A Comparative Analysis

White Paper

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1 Introduction

Field-Programmable Gate Arrays (FPGAs) are integral to today's electronics, offering unmatched flexibility and configurability. However, their reliance on SRAM cells for configuration introduces vulnerabilities to SEUs. This paper explores SEUs in FPGAs, highlighting why they must be prevented and how rapid correction is crucial.

2 Understanding Single-Event Upsets

SRAM Cells: The Heart of FPGAs

SRAM cells are the control centers of FPGAs, storing the Bitstream that governs their operation. Any change in the SRAM cell state can lead to catastrophic functional failures, making SEUs a grave concern.

Shrinking Transistors and SEUs

While SRAM cells often start from older technology, their susceptibility to SEUs increases as transistor sizes shrink to save die area. This downsizing reduces their ability to retain data, making them vulnerable to various external factors, especially in aerospace applications.

Cosmic Rays and Earth's Surface

Ordinarily, cosmic rays dissipate harmlessly in Earth's atmosphere, posing little threat to surface dwellers. However, SRAM cells' shrinking transistor sizes have led to concerns about even reduced cosmic rays causing SEUs, potentially leading to FPGA malfunctions.

Particles of Interest

Two primary particles causing SEUs are neutrons (mimicking cosmic rays) and Alpha particles, typically emitted by solder balls in packages. While changing materials is an option, it's often more economical to handle SEUs effectively.

3 Advantages of GOWIN FPGA Solutions

Strengthening SRAM Cells

Preventing SEUs begins with strengthening SRAM cells. GOWIN's innovative approach involves designing custom SRAM cells and enhancing their resilience. This measure significantly improves SEU resistance, even in smaller die sizes like the 22nm Arora V.

The 22nm BSRAM is till using TSMC foundry cells, there is a notable difference in the SER report. We do have hard ECC circuits for users to correct BSRAM SEU errors when reading out BSRM content.

Comparative Performance

Comparing GOWIN's 22nm FPGA with competitors like Company X's 28nm 6 and 7 serials reveals GOWIN's superior SEU resistance. Comprehensive test data highlights this performance edge.

Controlled Testing

To quantify SEU resilience, controlled testing with neutron and Alpha particle bombardment is essential. GOWIN's failure rate data shows robust protection against SEUs, surpassing competitors and prior FPGA generations. Below is the comparison to Gowin's GW2A 55nm Configuration SRAM cell which comes from TSMC 55nm GP process. (Ref TN713, GOWIN 22nm FPGA SER Test Report)

Table 1 55nm TSMC SRAM Configuration Cell VS 22nm Gowin SRAM Configuration Cell

	55nm FIT/Mb	22nm FIT/Mb
CSNS Neutron	165	59
Thermal Neutron	58	12
Alpha	55	7

4 Rapid Error Correction

The Importance of Error Correction

For mission-critical applications, error correction is paramount. GOWIN employs a Hamming code-based error correction system, capable of detecting and correcting data errors.

Comparative Error Correction

GOWIN's error correction algorithm excels compared to Company X. Company X can only correct single-bit errors or adjacent two-bit errors (in advanced mode) per frame, while GOWIN's GW5A can correct a greater variety of two-bit errors per frame or multi-bit errors spanning multiple positions in the frame. Additionally, GOWIN's GW5A devices can report unrecoverable multi-bit errors, thereby enhancing the system's reliability.

Efficient Frame Size

GOWIN's FPGA frames are designed for efficiency, with significantly fewer bits per frame compared to Company X's. Smaller frame sizes reduce the risk of multiple-bit errors.

Some more information about the Frame size:

138K: Frame length: 1,513 bits

25k: Frame length: 469 bits

60k: Frame length: 918 bits

Compared to Company X serial 7 Frame is 3,232 bits.

Dedicated Parabit

GOWIN integrates dedicated Parabits within the SRAM frame, simplifying error correction, no fabric function is involved for detection and correction operation. Gowin provides a simple wrapper IP – "SEU Handler" to make users easily access the SEU report and correction function. This approach enhances reliability and efficiency.

Customizable Scanning Frequency

GOWIN's FPGA solutions offer customizable scanning frequencies, enabling faster error detection and correction, crucial for uninterrupted operation, particularly in critical server environments. In advanced mode, the scan frequency can be up to 200MHz.

5 Efficiency and Integration

GOWIN's FPGA solutions integrate SEU mitigation features into the hardware, simplifying deployment for customers. This approach ensures efficient, reliable operations.

6 GOWIN 22nm FPGA SER Test Report

Test Background

- GOWIN’s FPGA devices are SRAM-based, which means the user logic is programmed and controlled by internal configuration SRAM cells. A Single event upset of an SRAM cell, introduced by Alpha particles or Neutron particles, is well understood by the industry and needs to be considered in system failure rate calculations for mission-critical, functional safety, and high-reliability applications.

SRAM Tested

The number of SRAM cells can be derived from the bitstream file. The bitstream file contains all the data needed to be programmed into the FPGA SRAM cell array. Therefore, from the array size, we should be able to obtain the SRAM cell number. Such an array includes 2 types of SRAM cells: one is the configuration SRAM; the other is the block SRAM that users utilize for memory storage in their designs which does not involve the logic control. Table 2 and Table 3 show the soft error rates caused by single event upsets (SEUs) affecting memory cells used as configuration SRAM and block SRAM.

Test Methods

Neutron cross-sections are determined from CSNS beam testing according to the JESD89/6 Accelerated High-energy Neutron Test Procedure, and the thermal neutron cross-section according to the JESD89/7 Accelerated Thermal Neutron Test Procedure. The neutron soft error rate (in FIT/Mb) is corrected for New York City. Alpha particle cross-section is determined by Americium-241 source as alpha radiation source according to JESD89/5 Accelerated Alpha Particles Test Procedure, and the alpha soft error rate (in FIT/Mb) is corrected based on alpha emissivity 0.001 counts/cm2/hr.

Soft Error Rates for Configuration SRAM

Table 2 below shows the soft error rates caused by single event upsets (SEUs) affecting memory cells used as configuration SRAM.

Table 2 SER for Configuration SRAM

Tech Node	Product Family	CSNS Neutron[3]			Thermal Neutrons			Alpha Particle (Actual)[4]		
22nm	Arora V	Cross-section(cm^2/bit)	FIT/Mb[5]	std dev	Cross-section (cm^2/bit)	FIT/Mb[5]	std dev	Cross-section (cm^2/bit)	FIT/Mb	std dev
		$4.30*10^{-15}$	58.6	2	$1.80*10^{-15}$	12.3	7	$6.21*10^{-12}$	6.7	1

Note!

- [1] Experiments are performed on GW5A-25 product, with the numbers of 650 KBytes SRAM.
- [2] Experiments are performed at ambient temperature with typical power supply voltages.
- [3] Data from China Spallation Neutron Source (CSNS)
- [4] Typical alpha data is based on alpha emissivity of 0.001counts/cm2/hr.
- [5] Neutron soft error rates (in FIT/Mb) are corrected for New York City, according to JESD89A.
- [6] During the test with ECC function on, all SEUs detected during the test were corrected, the SER is 0.

Soft Error Rates for Block SRAM

Table 3 below shows the soft error rates caused by SEUs affecting memory cells used as block SRAM.

Table 3 SER for Block SRAM

Tech Node	Product Family	CSNS Neutron[3]			Thermal Neutrons			Alpha Particle (Typical) [4]		
22nm	Arora V	Cross-section(cm^2/bit)	FIT/Mb[5]	std dev	Cross-section (cm^2/bit)	FIT/Mb[5]	std dev	Cross-section (cm^2/bit)	FIT/Mb	std dev
		$1.34*10^{-14}$	165.0	22	$1.16*10^{-14}$	79.3	30	$3.54*10^{-11}$	37	2

Note!

- [1] Experiments are performed on GW5A-25 product, with the numbers of 126 KBytes SRAM.
- [2] Experiments are performed at ambient temperature with typical power supply voltages.
- [3] Data from China Spallation Neutron Source (CSNS)
- [4] Typical alpha data is based on alpha emissivity of 0.001counts/cm2/hr, actual
- [5] Neutron soft error rates (in FIT/Mb) are corrected for New York City, according to JESD89A.

ECC for Configuration SRAM

Gowin 22nm FPGAs provide ECC function, an experimental group was set up for ECC function capability verification. Under the same FLUX experimental conditions, with the SRAM readback frequency of 15MHz and the readback and comparison period of 44610us, SEUs can be observed during the readback process, in which SBUs are observed while no MBU is found. All observed SBUs are corrected by ECC circuitry, and the whole bitstream is maintained to allow the device to work normally.

7 Conclusion

GOWIN's GW5AT and GW5A family of FPGAs excel in preventing and correcting SEUs, outperforming competitors like Company X. With enhanced SRAM cells, efficient error correction, and dedicated Parabits, GOWIN offers a more reliable and efficient solution for mission-critical applications. Our FPGA solutions empower customers to deploy robust systems, even in the most challenging environments, with confidence.

Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

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