



Gowin Scaler IP

User Guide

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Revision History

Date	Version	Description
09/17/2019	1.0E	Initial version published.
01/16/2020	1.1E	Reference design and its file updated.
06/18/2020	2.0E	● Support for device updated. ● Port description updated. ● Parameter description updated.
03/07/2022	3.0E	● Removed output buffer to reduce BSRAM resource. ● Extended input line buffer depth, up to 4096. ● Removed Bicubic 6 tap algorithm.

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1 About This Guide

1.1 Purpose

The purpose of Gowin Scaler IP User Guide is to help you learn the features and usage of Gowin Scaler IP by providing the descriptions of functions, ports, timing, configuration and call, reference design.

1.2 Related Documents

The user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. [DS100, GW1N series of FPGA Products Data Sheet](#)
2. [DS117, GW1NR series of FPGA Products Data Sheet](#)
3. [DS102, GW2A series of FPGA Products Data Sheet](#)
4. [DS226, GW2AR series of FPGA Products Data Sheet](#)
5. [DS961, GW2ANR series of FPGA Products Data Sheet](#)
6. [DS971, GW2AN-18X & 9X Data Sheet](#)
7. [DS976, GW2AN-55 Data Sheet](#)
8. [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Abbreviations and Terminology

Abbreviations and Terminology	Meaning
FPGA	Field Programmable Gate Array
SRAM	Static Random Access Memory
VESA	Video Electronics Standards Association
VS	Vertical Sync
HS	Horizontal Sync
DE	Data Enable

Abbreviations and Terminology	Meaning
IP	Intellectual Property
RGB	R(Red) G(Green) B(Blue)

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Overview

Gowin Scaler IP is used to convert the input video images from one resolution $X_{in} * Y_{in}$ to another output resolution $X_{out} * Y_{out}$. Resolution parameters can be preset in the IP configuration interface or dynamically configured in real time. In addition, interpolation algorithms supported by Scaler IP include nearest neighbor, bilinear and bicubic.

Gowin Scaler IP supports real-time video signal input and memory interface video signal input, and both input and output data interfaces are parallel video signals.

Table 2-1 Gowin Scaler IP

Gowin Scaler IP	
Logic Resource	Please refer to Table 2-2.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.8.05 and above)

2.2 Key Features

- Supports single, YCbCr422, YCbCr444 and RGB video format
- Supports parallel input
- Supports dynamic configuration of scale parameters
- Supports nearest neighbor, bilinear and bicubic algorithms
- The vertical and horizontal support 4 taps (for Bicubic only)
- The vertical and horizontal coefficients support 8, 16 and 32 phases (for Bicubic only)
- Image data supports 8,10, 12 bits width

- Filter coefficient supports 9~16 bits width
- Supports input and output resolution range from 32 x 32 to 4096 x 4096

2.3 Resource Utilization

Gowin Scaler IP employs Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking GW1N-9 and GW2A-18 series of FPGA devices as an instance, Table 2-2 presents an overview of the resource utilization. GW1N only supports nearest neighbor and bilinear algorithms. For the applications in other Gowin FPGA devices, please see the later release information.

Table 2-2 Resource Utilization

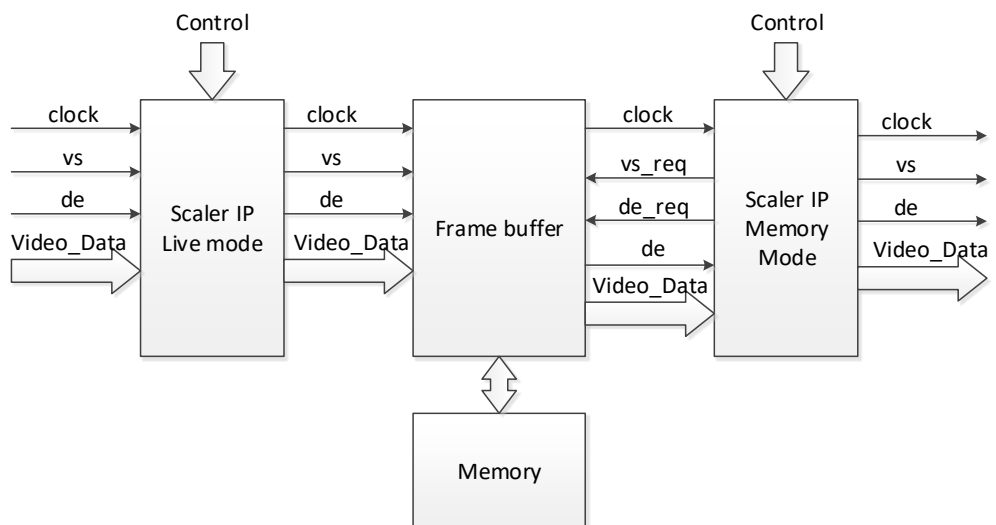
Device	GW1N-9	GW1N-9	GW2A-18	GW2A-18
Algorithm	Nearest Neighbor	Bilinear	Bilinear	Bicubic
Resolution	800x600 to 1280x720	800x600 to 1280x720	800x600 to 1280x720	800x600 to 1280x720
Video Format	YC444	YC444	YC444	YC444
Tapsize	2x2	2x2	2x2	4x4
Data Bit Width	8	8	8	8
Coefficient Bit Width	16	16	16	16
Resisters	933(17%)	933(17%)	926(5%)	1774(11%)
LUTs	738(10%)	738(10%)	735(3%)	1478(7%)
BSRAMs	12(46%)	12(46%)	12(26%)	24(52%)
MULT18x18	0/0/20	12/12/20	12/12/48	24/24/48

3 Functional Description

3.1 System Diagram

Gowin Scaler IP is used to receive video signals for scale in Live mode or video data in Memory mode. The input and output data interfaces are all video standard parallel signals, and the control interface is scale parameter signal.

Figure 3-1 System Block Diagram



3.2 Block Diagram

Figure 3-2 Block Diagram (Live mode)

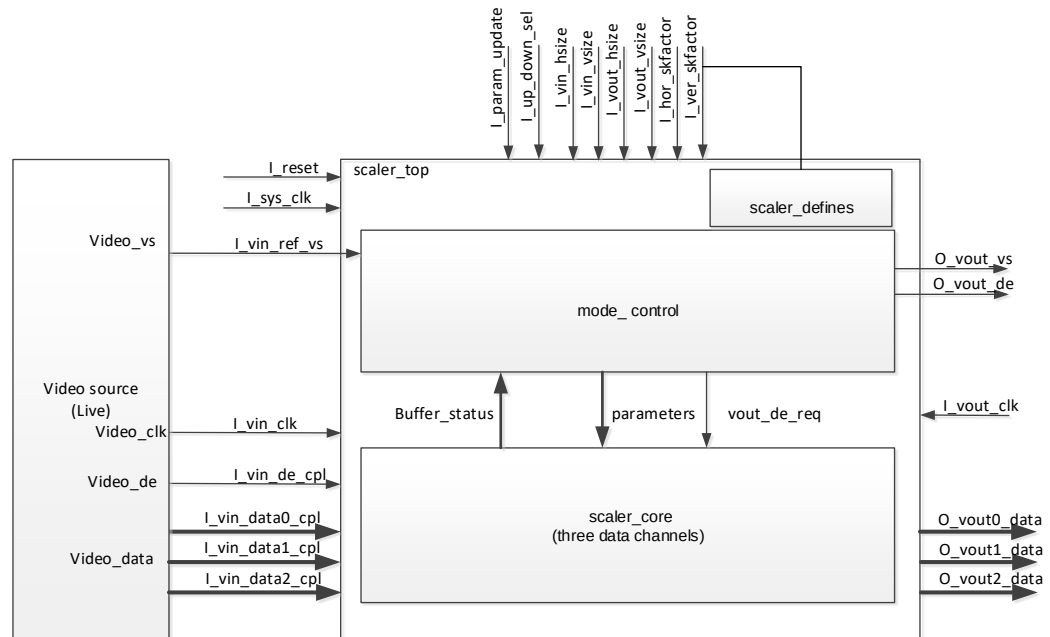
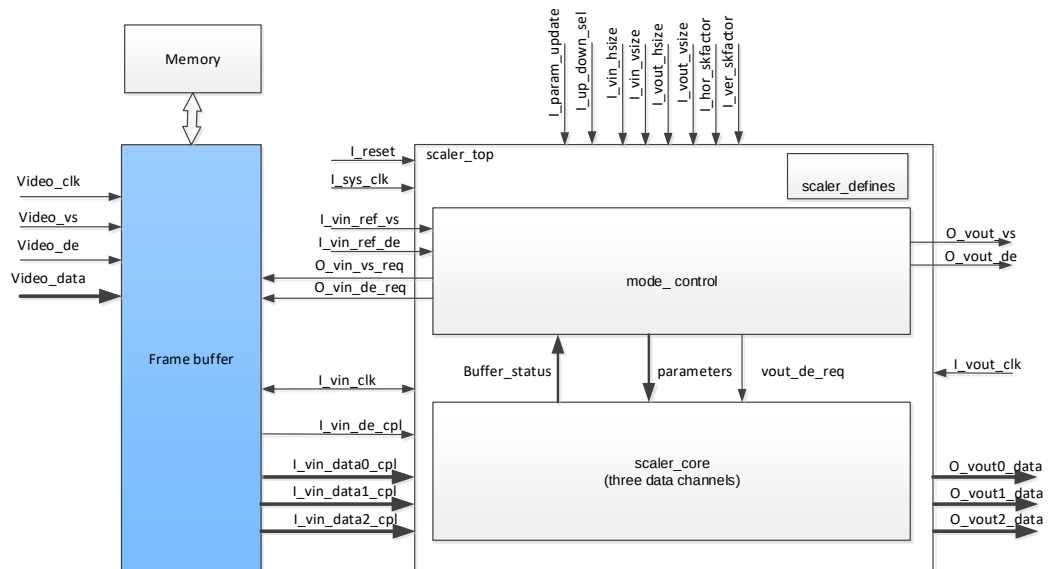


Figure 3-3 Block Diagram (Memory mode)



Scaler IP includes parameter definition module, mode control module and scale core module, among which the scale core module includes vertical calculation sub-module, horizontal calculation sub-module, row calculation control state machine sub-module and output row buffer sub-module, realizing video image scale function via mutual cooperations among these modules.

1. Parameter Definition Module

The Scaler parameters include video format, data source, data bit width, video resolution of input and output, and dynamic configuration.

2. Mode Control Module

Frame synchronization and data enable signals for input and output are configured based on the input video source type, defined parameters, and input and output data buffer status.

3. Scale Core Module

According to the input and output video resolution parameters, the live image scale operation is completed and output, and the empty and full state of the data buffer is output also. This module includes four sub-modules: vertical calculation sub-module, horizontal calculation sub-module, row calculation control state machine sub-module, and output row buffer sub-module.

- a). The functions completed by vertical calculation sub-module include vertical coordinate conversion, vertical calculation coefficient generation, vertical calculation data generation, vertical multiplication and addition processing, etc.
- b). The functions completed by horizontal calculation sub-module include horizontal coordinate conversion, horizontal calculation coefficient generation, horizontal calculation data generation, horizontal multiplication and addition processing, etc.
- c). According to the state of each module, the row calculation control state machine sub-module generates row calculation enable signal, controlling the vertical calculation sub-module and the horizontal calculation sub-module for calculation.
- d). The output row buffer sub-module will buffer the final calculated data into this sub-module and output the scaled data according to the data output request.

3.3 Working Principle

The working principle of Scaler IP is relatively simple. Based on VESA video standard, parallel video data with VS, DE and DATA is input into the input row buffer of Scaler IP. According to the input and output image resolution and scale factor parameters, the mapping position of each pixel of the target image in the original image is calculated respectively. Where (x,y) is the pixel coordinate of the target image, (x',y') is the pixel coordinate of the original image, ver_skfactor and hor_skfactor are the vertical and horizontal scale factors respectively, and the calculation formula is as follows.

$$x' = x * \text{hor_skfactor}$$

$$y' = y * \text{ver_skfactor}$$

Note!

- Scale factor, sk = input resolution/output resolution.
- Scale multiplier, sr = output resolution/input resolution.

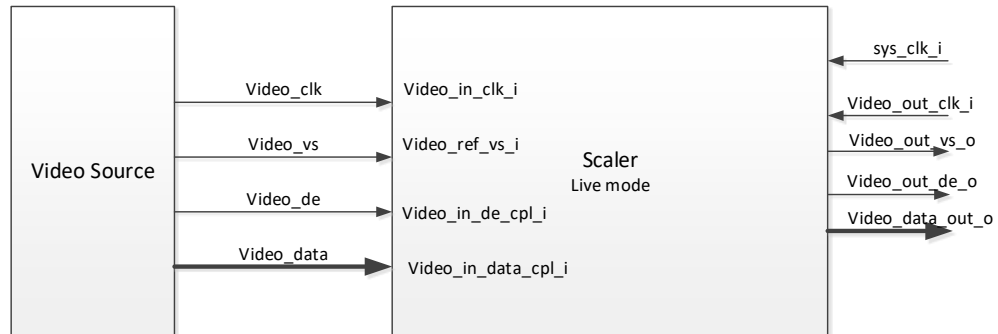
Finally, the calculated pixel of the target image is output to the output row buffer, then is output according to the parallel video data format with VS, DE and DATA.

Depending on the input video format, set the number of scale core and signal type.

Depending on the type of input signal source, Scaler IP can be set to two modes, Live mode and Memory mode.

3.3.1 Live Mode

Figure 3-4 Live Mode Block Diagram



The estimation formula of minimum output pixel clock and system working clock frequency in Live mode is as follows.

$$\text{Minf}_{\text{out}} = (\text{OutWidth} * \text{OutHeight}) / (\text{InHeight} / f_{\text{hs}}) * 1.1$$

Note!

- f_{hs} represents the input video line frequency
- "1.1" represents 10% margin increase

$$\text{Minf}_{\text{sys}} = 1.05 * f_{\text{in}} * (\text{MaxWidthTotal} * \text{SR}_{\text{ver}}) / (\text{InWidthTotal} + \text{InHblank})$$

Notes!

- SR_{ver} means that vertical scaling multiple is rounded.
- MaxWidthTotal means a larger total of input or output.

Example 1: Zoom in 640x480@60hz to 1920x1080@60hz

$$f_{\text{hs}} = 31.5\text{KHz}, f_{\text{in}} = 27\text{MHz}, \text{SR}_{\text{ver}} = \text{round_up}(1080/480) = 3$$

$$\text{InWidthTotal} + \text{InHblank} = 857 + 217 = 1074$$

$$\text{MaxWidthTotal} = 2200$$

$$\text{Minf}_{\text{out}} = (1920 * 1080) / (480 / 31500) * 1.1 = 149.69\text{MHz}$$

$$\text{Minf}_{\text{sys}} = 1.05 * 27\text{MHz} * (2200 * 3) / 1074 = 174.22\text{MHz}$$

Example 2: Zoom out 1920x1080@60hz to 1280x720@60hz

$$f_{\text{hs}} = 67.5\text{KHz}, f_{\text{in}} = 148.5\text{MHz}, \text{SR}_{\text{ver}} = \text{round_up}(720/1080) = 1$$

$$\text{InWidthTotal} + \text{InHblank} = 2200 + 280 = 2480$$

$$\text{MaxWidthTotal} = 2200$$

$$\text{Minf}_{\text{out}} = (1280 * 720) / (1080 / 67500) * 1.1 = 63.36\text{MHz}$$

$$\text{Minf}_{\text{sys}} = 1.05 \times 148.5\text{MHz} \times (2200 \times 1) / 2480 = 138.32\text{MHz}$$

In addition, the estimation formule of system clock frequency and input video clock frequency is as follows:

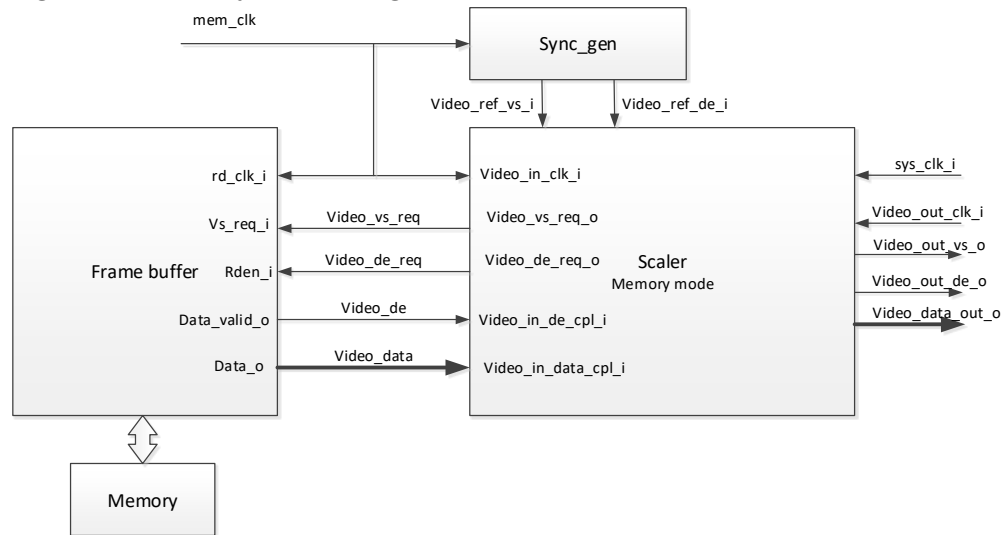
$$\frac{\text{sys_clk}}{\text{vin_clk}} > \text{sr}(\text{ZoomLevel})$$

When zooming out , $\text{sr} < 1$, the sys_clk and out_clk frequency only need to be slightly higher than the input clock when zooming out in live mode, or even using the input clock.

However, when zooming in in Live mode, especially when the magnification times is large, sys_clk is highly required, and this mode is not recommended.

3.3.2 Memory Mode

Figure 3-5 Memory Mode Diagram



The estimation formula of minimum input and output pixel clock in memory mode is as follows, and the system clock takes the larger of the two.

$$f_{\text{in}} \geq H_{\text{intotal}} * V_{\text{intotal}} * f_{\text{invs}}$$

$$f_{\text{out}} \geq H_{\text{outtotal}} * V_{\text{outtotal}} * f_{\text{outvs}}$$

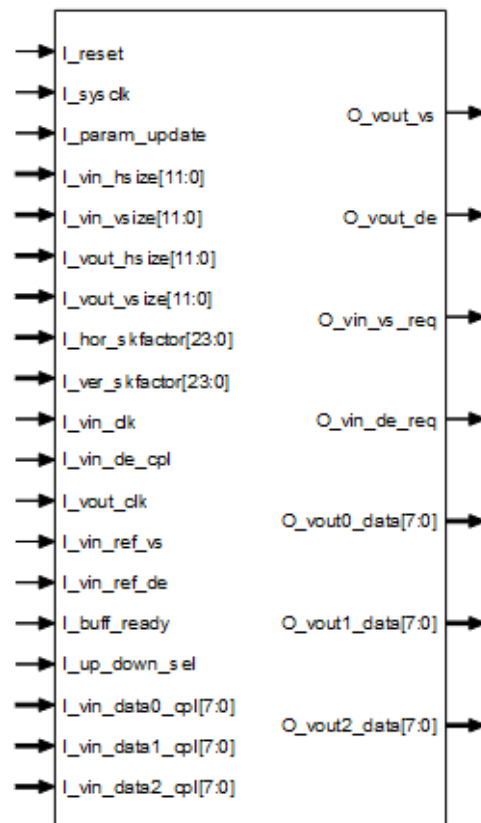
This clock frequency is the pixel clock frequency of each resolution in VESA standard, and the user can refer to VESA.

Since the system clock only needs to take the input/output pixel frequency higher than this frequency in Memory mode, the system clock will not be required highly. So Memory mode is suitable for zooming in.

4 Port List

The IO port of Gowin Scaler IP is shown in Figure 4-1.

Figure 4-1 Scaler IO Port Diagram



Ports may vary slightly depending on the configuration parameters.

The IO port of Gowin Scaler IP is shown in Table 4-1.

Table 4-1 Gowin CSC IP Ports List

No.	Signal Name	I/O	Description	Notes
1	I_reset	I	Reset signal, active-high	The I/O of all the signals takes CSC IP as reference.
2	I_sysclk	I	System working clock	
3	I_param_update	I	This signal is valid when dynamic control is enabled. Parameter updated enable signal, active-high, which requires at least 200ns.	
4	I_vin_hsize	I	This signal is valid when dynamic control is enabled. Input horizontal resolution of the image.	
5	I_vin_vsize	I	This signal is valid when dynamic control is enabled. Input vertical resolution of the image.	
6	I_vout_hsize	I	This signal is valid when dynamic control is enabled. Output horizontal resolution of the image.	
7	I_vout_vsize	I	This signal is valid when dynamic control is enabled. Output vertical resolution of the image.	
8	I_hor_skfactor	I	This signal is valid when dynamic control is enabled. Horizontal scale factor, unsigned fixed-point number. Above 8 bits represents integer, and below 16 bits represents decimal. The formula = (input horizontal resolution/output horizontal resolution)*(2 ¹⁶).	
9	I_ver_skfactor	I	This signal is valid when dynamic control is enabled. Vertical scale factor, unsigned fixed-point number. Above 8 bits represents integer, and below 16 bits represents decimal. The formula = (input vertical resolution/output vertical resolution)*(2 ¹⁶).	
10	I_vin_clk	I	Video input pixel clock	
11	I_vin_ref_vs	I	Input the reference field synchronization vs signal. When selecting Live mode, this signal is invalid. When selecting Memory mode, connect to vs signal of synchronous timing generation module.	
12	I_vin_ref_de	I	Input reference data enable de signal. When selecting Live mode, this signal is invalid. When selecting Memory mode, connect to de signal of synchronous timing generation module.	
13	O_vin_vs_req	O	Output field synchronization vs request	

No.	Signal Name	I/O	Description	Notes
			signal. When selecting Live mode, this signal is invalid. When selecting Memory mode, connect to vs request signal of frame buffer module.	
14	O_vin_de_req	O	Output data enable de request signal. When selecting Live mode, this signal is invalid. When selecting Memory mode, connect to de request signal of frame buffer module.	
15	I_buff_ready	I	Front-end input buff valid signal. When selecting Live mode, this signal is invalid. When selecting Memory mode, connect to frame buffer fifo status signal.	
16	I_up_down_sel	I	This signal is valid when dynamic control is enabled and when Memory mode is selected. Zoom in or out the selection signal: 0 represents zooming in; 1 represents zooming out;	
17	I_vin_vs_cpl	I	Input field synchronization vs signal. When selecting Live mode, connect to the input video vs signal. When selecting Memory mode, this signal is invalid.	
18	I_vin_de_cpl	I	Actual input data enable de signal. When selecting Live mode, connect to the input video de signal. When selecting Memory mode, connect to frame buffer module output de signal.	
19	I_vin_data0_cpl	I	Channel 0 input video data signal. When selecting Live mode, connect to the input video data signal. When selecting Memory mode, connect to the output data signal of frame buffer module. When the video format is YC422, it is the Y component.	
20	I_vin_data1_cpl	I	Channel 1 input video data signal. When selecting Live mode, connect to the input video data signal. When selecting Memory mode, connect to the output data signal of frame buffer module. When the video format is YC422, it is the C component.	
21	I_vin_data2_cpl	I	Channel 2 input video data signal. When selecting Live mode, connect to the	

No.	Signal Name	I/O	Description	Notes
			input video data signal. When selecting Memory mode, connect to the output data signal of frame buffer module.	
22	I_vout_clk	I	Video output pixel clock	
23	O_vout_vs	O	Output video field synchronization vs signal	
24	O_vout_de	O	Output video data enable de signal	
25	O_vout0_data	O	Channel 0 output video data signal. When the video format is YC422, it is the Y component.	
26	O_vout1_data	O	Channel 1 output video data signal. When the video format is YC422, it is the C component.	
27	O_vout2_data	O	Channel 2 output video data signal.	
28	O_vval_de	O	Debug option, vertical calculation output de signal.	
29	O_vval_data0	O	Debug option, vertical calculation output data signal.	
30	O_vval_data1	O	Debug option, vertical calculation output data signal.	
31	O_vval_data2	O	Debug option, vertical calculation output data signal.	

5 Parameter Configuration

Table 5-1 Scaler Parameter

No.	Name	Range	Default Value	Description
1	Data_Width	8, 10, 12	8	Single component data bus width of input/output image pixel
2	Coefficient Width	9~16	16	Interpolation calculation coefficient bus width; The highest 1bit for sign, 1bit for integer and the remainder for decimal place
3	Parameter Dynamic Control	Yes, No	Yes	Parameter dynamic configuration enable
3	Input Frame Width	32~4096	1024	Static input image horizontal resolution is valid when PARAM_DYNAMIC_CTRL is No.
4	Input Frame Height	32~4096	768	Static input image vertical resolution is valid when PARAM_DYNAMIC_CTRL is No.
5	Output Frame Width	32~4096	1024	Static output image horizontal resolution is valid when PARAM_DYNAMIC_CTRL is No.
6	Output Frame Height	32~4096	768	Static output image vertical resolution is valid when ; When PARAM_DYNAMIC_CTRL is No.
7	Video Format	Single, YC422, RGB or YC444	RGB or YC444	Video format selecting; Single: Single color component; YC422: The format of YCbCr 4:2:2 and inputs Y component and Cb/Cr component.

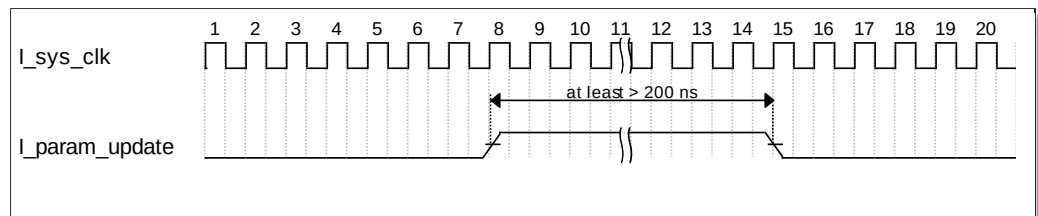
No.	Name	Range	Default Value	Description
				RGB or YCbCr 4:4:4: The format of YCbCr 4:4:4 and inputs Y component, Cb component and Cr component or RGB.
8	Data Source	Live, Memory	Live	Video source type selecting; LIVE: Represents parallel video data input. MEMORY: Represents read video data input from MEMORY.
9	Core Algorithm	Nearest neighbor, Bilinear, Bicubic	Bilinear	Scale core algorithm selection (GW1N and GW1NR can only select Nearest neighbor, Bilinear)
10	Filter Taps	2, 4	2	Filter coefficient tap (Bicubic can select 4, 6; Nearest neighbor and Bilinear can select 2)
11	Filter Phases	8, 16, 32	16	Filter coefficient phase (for Bicubic only)
12	Line Buffer Depth	1024, 2048, 4096	1024	Input line buffer depth must be greater than or equal to input frame width.
13	Vertical Data Enable	Yes, No	No	Debug option; display the vertical data if enabled.

6 Timing Description

This chapter describes the timing of Gowin Scaler IP.

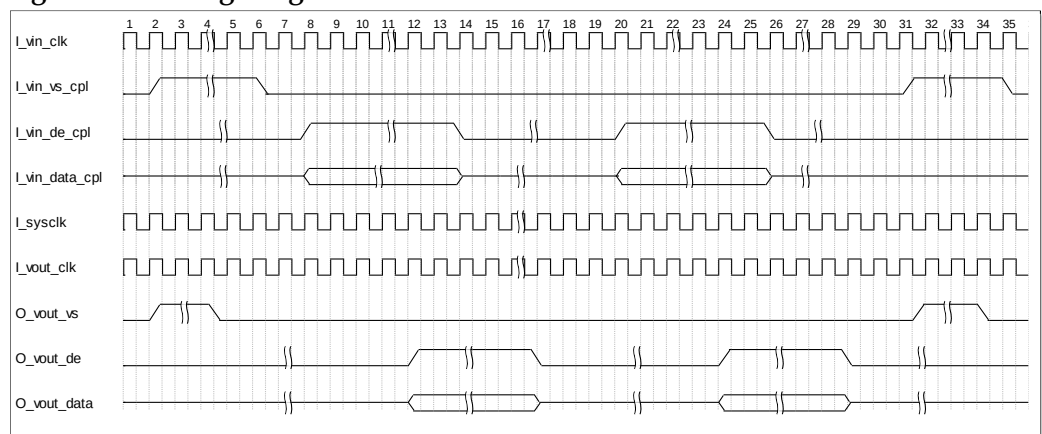
The timing requirement of I_param_update is as shown in Figure 6-1.

Figure 6-1 Timing Diagram of I_param_update



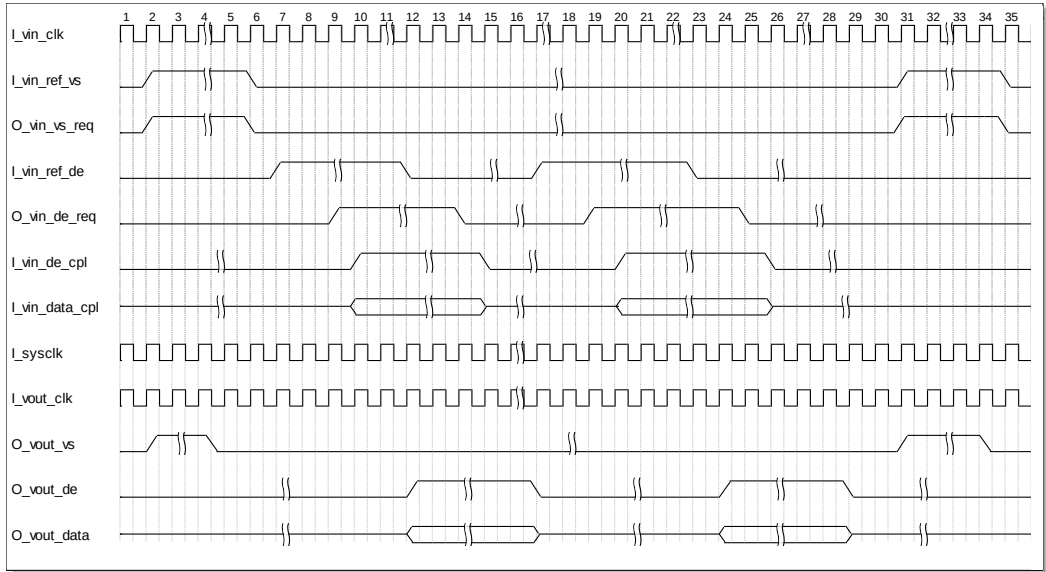
The timing diagram of Live mode is as shown in Figure 6-2.

Figure 6-2 Timing Diagram of Live Mode



The timing diagram of Memory mode is as shown in Figure 6-3.

Figure 6-3 Timing Diagram of Memory Mode



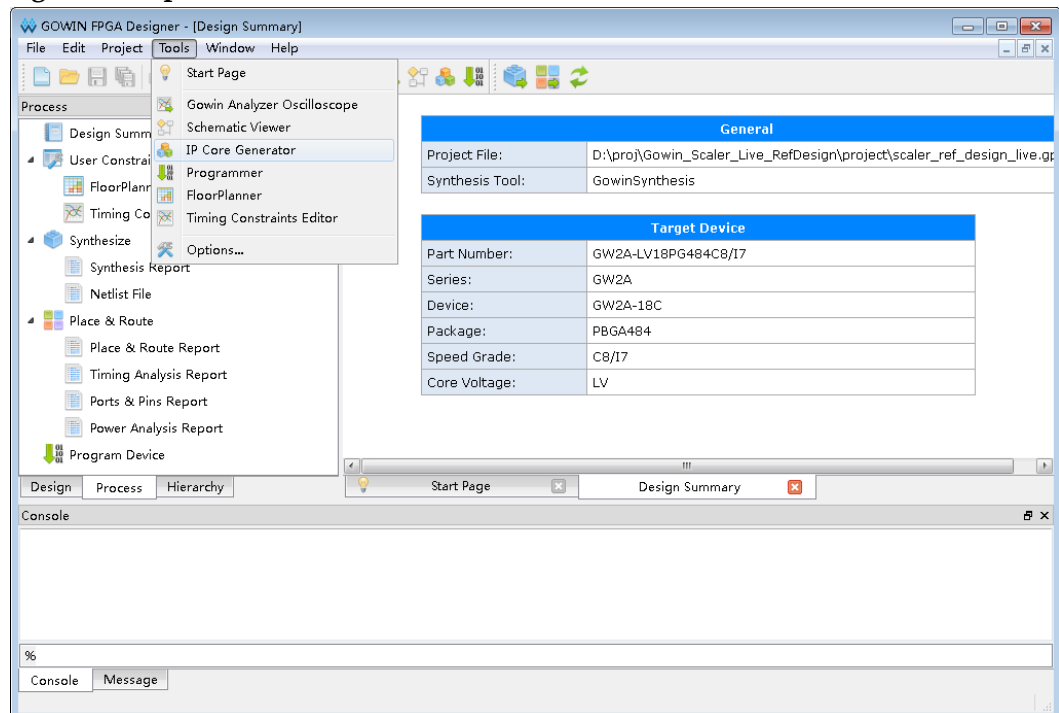
7 Interface Configuration

Users can use IP core generator tool in the IDE to call and configure Gowin Scaler IP.

1. Open IP Core Generator

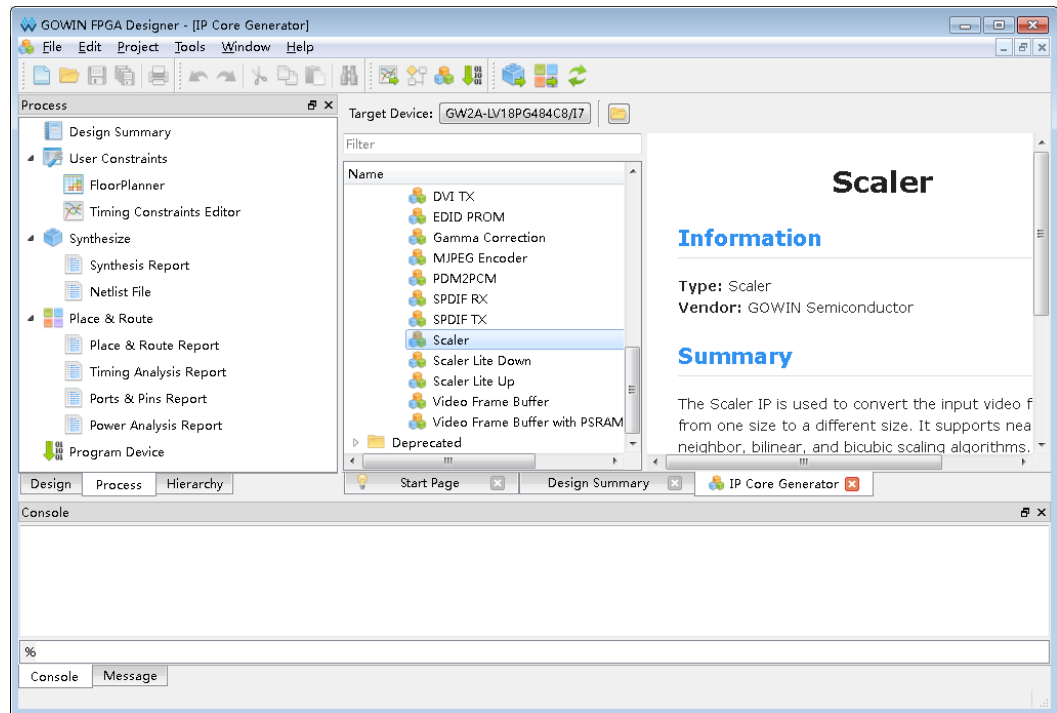
After creating the project, click the "Tools" tab in the upper left, select and open the IP Core Generator from the drop-down list, as shown in Figure 7-1.

Figure 7-1 Open IP Core Generator



2. Open Scaler IP Core

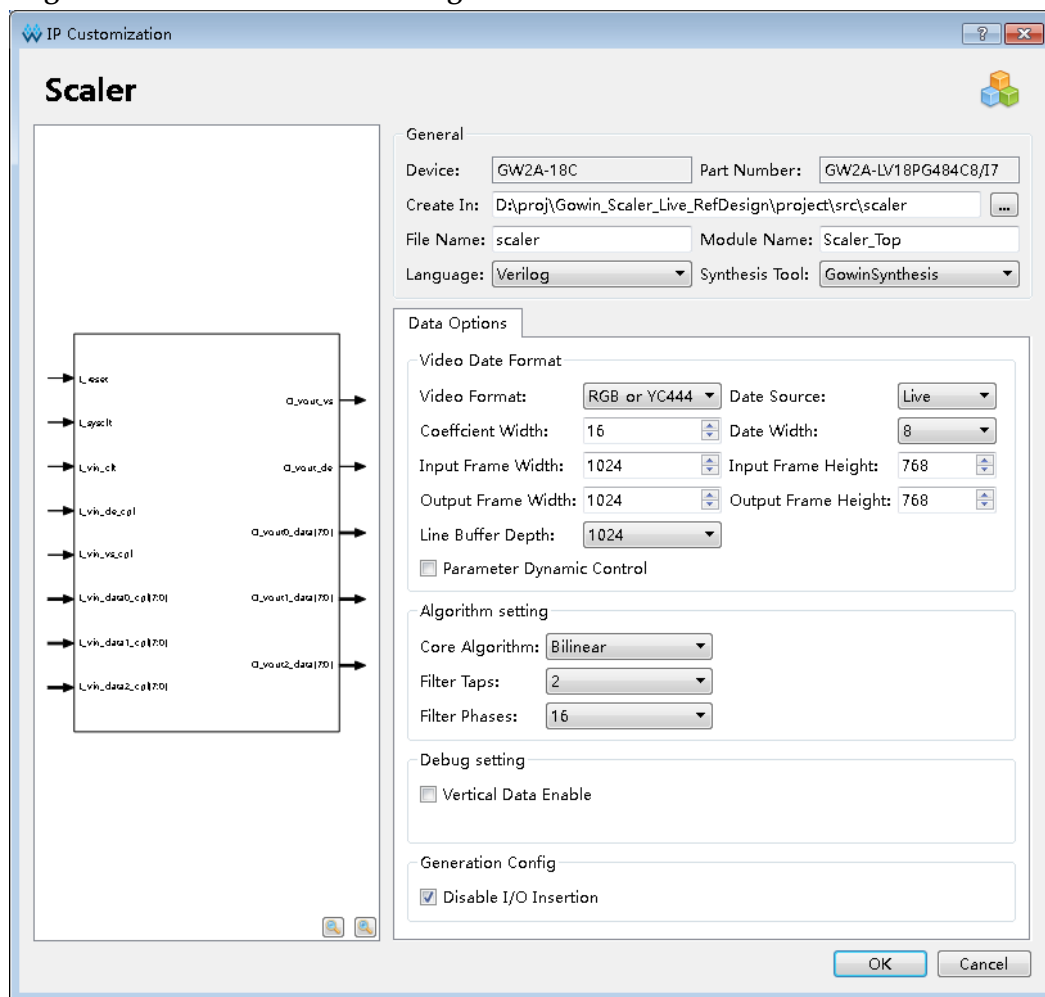
Click "Multimedia" option and double-click on "Scaler" to open the configuration interface, as shown in Figure 7-2.

Figure 7-2 Open Scaler IP Core

3. Open Scaler IP Core

On the left of the configuration interface is the port diagram of Scaler IP core, as shown in Figure 7-3.

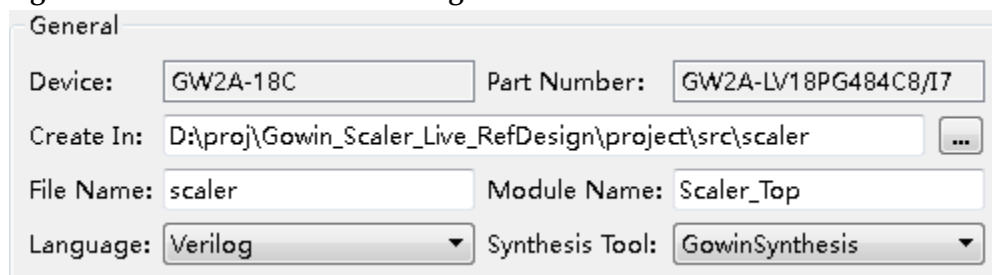
Figure 7-3 Scaler IP Core Port Diagram



4. Configuration Information

See the project basic information on the configuration interface. Take GW2A-18-PBGA484 as an example, the top-level file name of the generated project is shown in the "Module Name", and the default is "Scaler_Top", which can be modified by users. The file generated by the IP core is shown in "File Name", and the default is "scaler". It can be modified by users. The "Creat IN" option shows the IP core files path, and the default is \project path\src\scaler. It can be modified by users.

Figure 7-4 Basic Information Configuration Interface



5. Data Options

In the Data Options tab, users need to configure the algorithm, data bit width, resolution and other parameter information used by Scaler operations.

Figure 7-5 Options

The screenshot shows a configuration window titled "Data Options". It contains several sections with adjustable parameters:

- Video Date Format**
 - Video Format: **RGB or YC444** (dropdown)
 - Date Source: **Live** (dropdown)
 - Coefficient Width: **16** (spin box)
 - Date Width: **8** (spin box)
 - Input Frame Width: **1024** (spin box)
 - Input Frame Height: **768** (spin box)
 - Output Frame Width: **1024** (spin box)
 - Output Frame Height: **768** (spin box)
 - Line Buffer Depth: **1024** (spin box)
 - ☐ Parameter Dynamic Control
- Algorithm setting**
 - Core Algorithm: **Bilinear** (dropdown)
 - Filter Taps: **2** (spin box)
 - Filter Phases: **16** (spin box)
- Debug setting**
 - ☐ Vertical Data Enable
- Generation Config**
 - ☒ Disable I/O Insertion

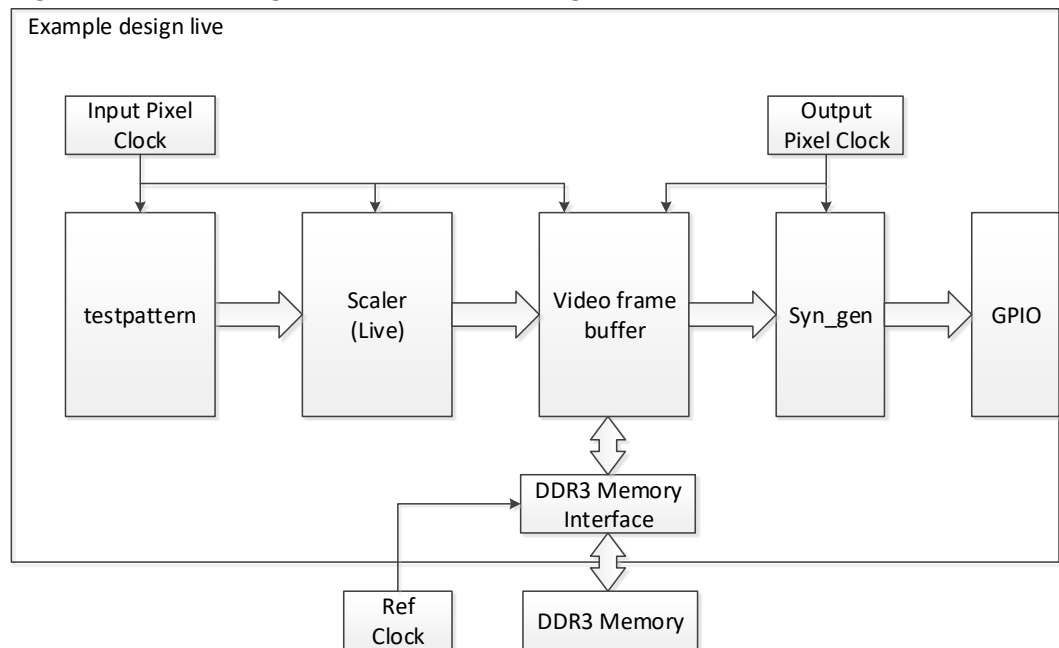
8 Reference Design

This chapter focuses on the usage and constructure of the reference design of Scaler IP. Please see the Scaler Reference Design for details at Gowinsemi website.

8.1 Design Instance Application

Taking DK-VIDEO-GW2A18-PG484 as an example, the block diagram is as shown in Figure 8-1. For the details of DK-VIDEO-GW2A18-PG484, you can click [here](#).

Figure 8-1 Blcok Diagram of Reference Design



In the above reference design example, Scaler IP selects the Live mode, and its steps are as follows:

1. The test pattern module is used to generate the test pattern with 1024x768 resolution and RGB888 data format.
2. Call Scaler IP core generator to generate Scaler module and zoom out the image from 1024x768 to 800x600.

3. The shrunk image data is written to the DDR3 buffer.
4. Then read from DDR3 with 1280x720 resolution.
5. Finally, the display is output to the monitor through the HDMI2 TX interface of the development board.

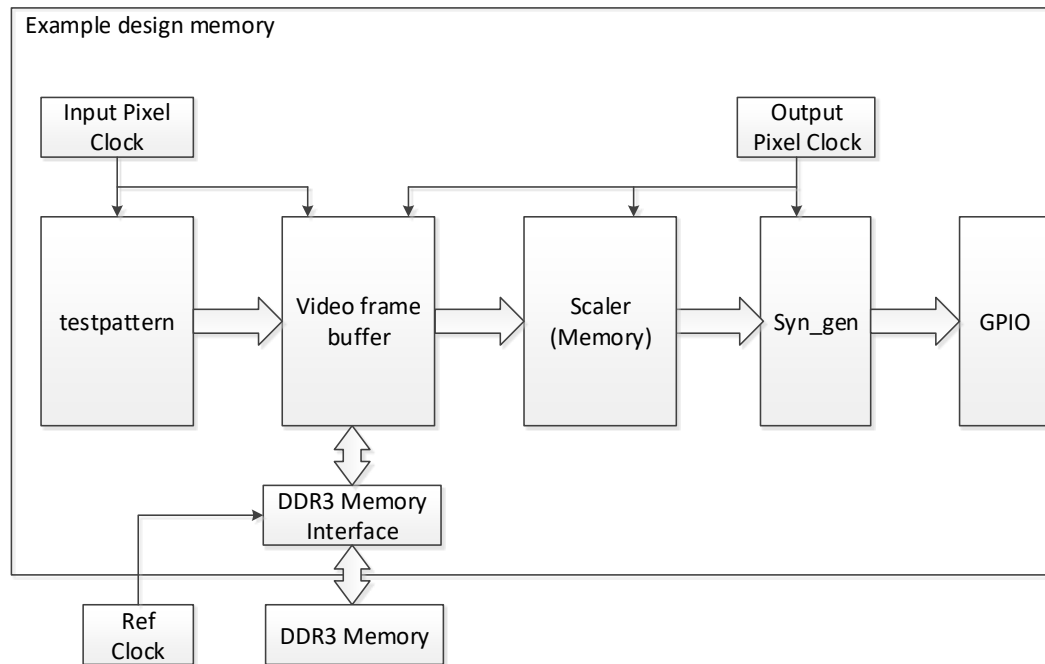
When the reference design is applied to the board level test, users can convert the output data via the video encoding chip and output it to the display or observe the data with the online logic analyzer or oscilloscope.

In the simulation project provided by the reference design, BMP is used as the test excitation source. tb_top is the top-level module of the simulation project. The simulation results can be compared with the output figures

8.2 Design Instance Application

Taking DK-VIDEO-GW2A18-PG484 as an example, the block diagram is as shown in Figure 8-2.

Figure 8-2 Block Diagram of Reference Design



In the above design example, Scaler IP selects Memory mde, and the steps are as follows:

1. The test pattern module is used to generate the test pattern with 800x600 resolution and RGB888 data format.
2. The generated image data is written to the DD R3 buffer.
3. Call Scaler IP core generator to generate Scaler module and zoom in the image from 1280x720 to1920x1080。
4. Because scale is generated by standard timing in Memory mode, the scaled data can be output and displayed. Finally, the display is output

to the monitor through the HDMI2 TX interface of the development board.

When the reference design is applied to the board level test, users can convert the output data via the video encoding chip and output it to the display or observe the data with the online logic analyzer or oscilloscope.

In the simulation project provided by the reference design, BMP is used as the test excitation source. tb_top is the top-level module of the simulation project. The simulation results can be compared with the output figures.

9 File Delivery

The delivery file of Gowin Scaler IP includes document, design source code and reference design.

9.1 Document

The document mainly includes the user guide.

Table 9-1 Documents List

Name	Description
IPUG903, Gowin Scaler IP User Guide	Gowin Scaler IP User Guide

9.2 Design Source Code (Encryption)

The encrypted code file includes the Gowin Scaler IP RTL encrypted code which is used for GUI in order to cooperate with Gowin software to generate the IP core required by users.

Table 9-2 Design Source Code List

Name	Description
scaler.v	The top-level file of the IP core, which provides users with interface information, encrypted.

9.3 Reference Design

Gowin_Scaler_Live_RefDesign folder includes the netlist file of Gowin Scaler IP, user reference design, constraints file, top-level file and the project file, etc.

Table 9-3 Gowin_Scaler_Live_RefDesign src File List

Name	Description
scaler_test_top.v	The top module of reference design
testpattern.v	Test pattern generation module
scaler_test_top.cst	Project Physical Constraints File
scaler_ref_design_live.sdc	Project Timing Constraints File
scaler	Scaler IP project folder
scaler.v	Scaler IP top-level file generated (encrypted)
scaler.vo	Scaler IP netlist file generated for simulation usage

Name	Description
ddr3_memory_interface	DDR3 Memory Interface IP project folder
video_frame_buffer	Frame buffer module project folder
line_buffer	Line buffer module project folder
gowin_rpll	PLL IP project folder
syn_code	Synchronous timing module project folder
i2c_master	I2C Master IP project folder
adv7513_iic_init.v	ADV7513 chip initialization module

Gowin_Scaler_Memory_RefDesign folder mainly contains netlist files, user reference designs, constraint files, top-level files and project folders for the Gowin Scaler IP.

Table 9-4 Gowin_Scaler_Memory_RefDesign src File List

Name	Description
scaler_test_top.v	The top module of reference design
testpattern.v	Test pattern generation module
scaler_test_top.cst	Project Physical Constraints File
scaler_ref_design_live.sdc	Project Timing Constraints File
scaler	Scaler IP project folder
scaler.v	Scaler IP top-level file generated (encrypted)
scaler.vo	Scaler IP netlist file generated for simulation usage
ddr3_memory_interface	DDR3 Memory Interface IP project folder
video_frame_buffer	Frame buffer module project folder
gowin_rpll	PLL IP project folder
syn_code	Synchronous timing module project folder
i2c_master	I2C Master IP project folder
adv7513_iic_init.v	ADV7513 chip initialization module

