



Gowin Gamma Correction IP

User Guide

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Revision History

Date	Version	Description
02/26/2021	1.0E	Initial version published.
09/26/2025	1.0.1E	Descriptions of Table 2-2 Resource Utilization (GW2A-18 C8/I7) updated.
10/17	1.0.2E	● 16-bit data width option removed. ● A note added below Table 2-2 Resource Utilization (GW2A-18 C8/I7).

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1 About This Guide

1.1 Purpose

The purpose of Gowin Gamma Correction IP User Guide is to help you learn the features and usage of this product by providing the descriptions of functions, ports, timing, GUI and reference design.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS961, GW2ANR series of FPGA Products Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)
- [DS971, GW2AN-18X & 9X Data Sheet](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1239, GW5AST series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)
- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1118, GW5ART series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
BSRAM	Block Static Random Access Memory
DSP	Digital Signal Processing
IP	Intellectual Property
ISP	Image Signal Processing
RGB	R(Red) G(Green) B(Blue)
SRAM	Static Random Access Memory

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2Overview

2.1 Introduction to Gamma Correction IP

Gowin Gamma Correction IP is a configurable, resource-saving IP that can correct image data to make the brightness of the display devices better suited to the light intensity of the human eyes.

Table 2-1 Gowin Gamma Correction IP Overview

Gowin Gamma Correction IP	
Logic Resource	Please refer to Table 2-2.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software

Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Features

- Supports input images with 8x8~4320x7680 pixels.
- Supports input images with 8/10/12-bit data width.
- Supports output images with 8/10/12-bit data width.
- Supports shared correction or independent correction of each color channel.

2.3 Max. Frequency

The maximum frequency of Gowin Gamma Correction IP is mainly determined by the speed grade of the devices and configuration parameters. Taking GW2A-18 series of FPGA devices as an example, it can reach up to 200MHz.

2.4 Resource Utilization

Gowin Gamma Correction IP resource utilization mainly depends on the size of image, etc. The resource utilization may be different with different devices.

Taking GW2A-18 series of FPGA as an example, the resource utilization of Gowin Gamma Correction IP under different lookup table configurations is shown in Table 2-2.

Table 2-2 Resource Utilization (GW2A-18 C8/I7)

Configuration	Data Width	LOGICS	REGS	BSRAMS
Frame Size (640*480) LUT Number (1)	8	24	80	1
Frame Size (640*480) LUT Number (3)	8	13	44	3

Note!

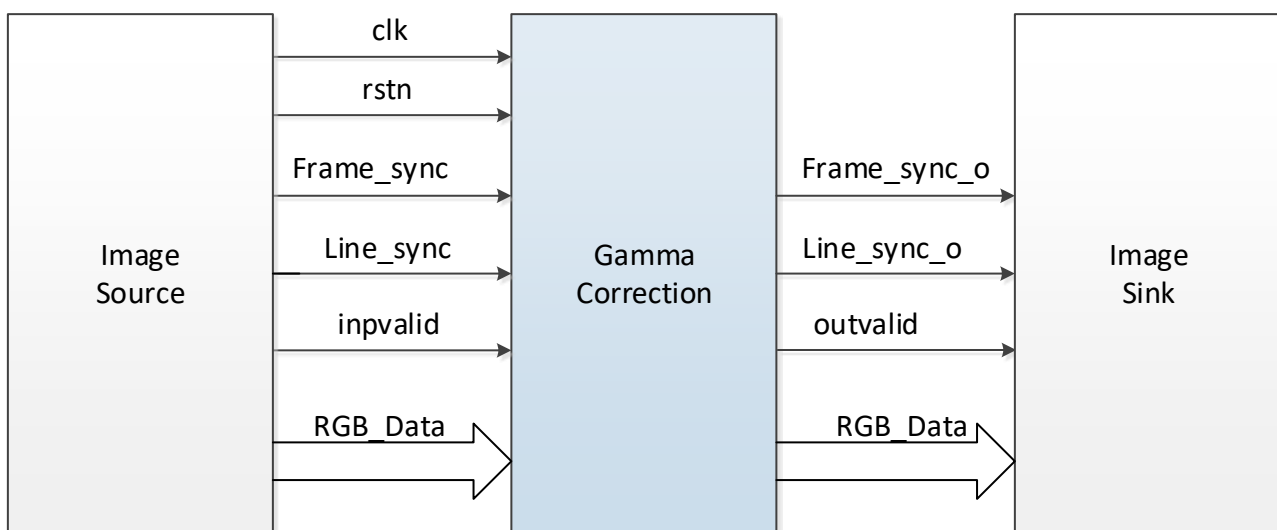
In RGB mode, gamma correction is applied to all three components, with a total of three LUTs. In YUV mode, gamma correction is applied only to the Y component, with a single LUT.

3 Functional Description

3.1 System Block Diagram

In Gowin Gamma Correction IP, the data comes from the RGB image data of the image source and is output after exponent operation according to the set gamma value, and the block diagram is shown in Figure 3-1.

Figure 3-1 Gowin Gamma Correction IP Block Diagram

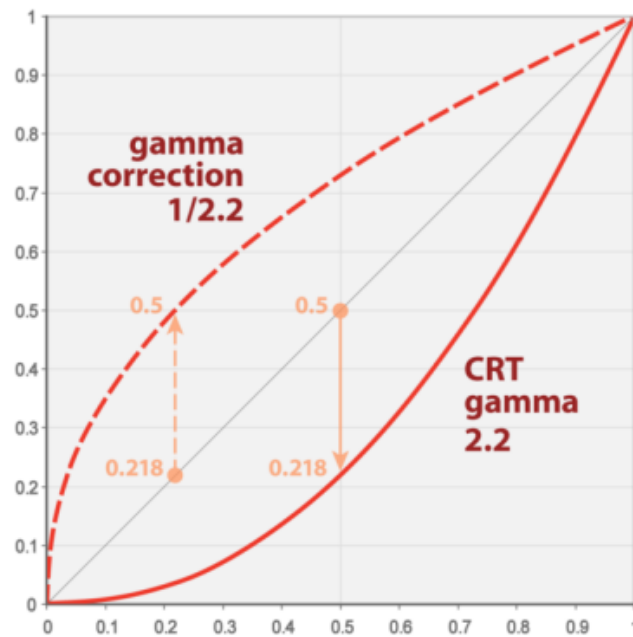


3.2 Algorithm Introduction

Gamma Correction is an algorithm that exponentially change the input image grayscale values to correct brightness deviations.

There is an exponential relationship between the light intensity of external light sources and the input light intensity. That is, at low illumination, human eyes are easier to distinguish changes in brightness. With the increasing illumination, it is not easy to distinguish changes in brightness with human eyes. There is a linear relationship between the camera photosensitivity and input light intensity. In order to facilitate the human eyes to recognize the image, the images captured by the camera need gamma correction.

Figure 3-2 Gamma Correction Calculation



The straight line in the figure represents the linear color/brightness value, and the curve represents the non-linear display curve of the monitor configuration.

In general, when the value of gamma correction is greater than 1, the highlight of the image is compressed while the dark is expanded, which is called "gamma expansion"; when the value of gamma correction is less than 1, the highlight of the image is expanded while the dark is compressed, which is called "gamma compression". In the simplest case, gamma correction is defined by the following power law expression,

$$data_out = data_in^\gamma$$

where data_in is the input data, γ is the gamma value, and data_out is the output data.

3.3 Gamma Correction Register

The registers of the Gowin Gamma Correction IP are affected by the LUT Number configuration and are used to re-write the gamma look-up tables. The host controller transfers the data to the Gowin Gamma Correction IP through the SRAM interface.

Table 3-1 Gowin Gamma Correction Registers

LUT Number	Name	Address	Width	Type	Description
1	Single_LUT	0x10	32	W	The upper 16 bits of the register represent the look-up tables address and the lower 16 bits represent the look-up tables storage data.

LUT Number	Name	Address	Width	Type	Description
3	Triple_LUT_R	0x10	32	W	The upper 16 bits of the register represent the R channel look-up tables address and the lower 16 bits represent the R channel look-up tables storage data.
	Triple_LUT_G	0x14	32	W	The upper 16 bits of the register represent the G channel look-up tables address and the lower 16 bits represent G channel look-up tables storage data.
	Triple_LUT_B	0x18	32	W	The upper 16 bits of the register represent the B channel look-up tables address and the lower 16 bits represent B channel look-up tables storage data.

4 Port Description

The IO ports of Gowin Gamma Correction IP are shown in Figure 4-1. For the details, you can see Table 4-1.

Figure 4-1 Ports Diagram of Gowin Gamma Correction IP

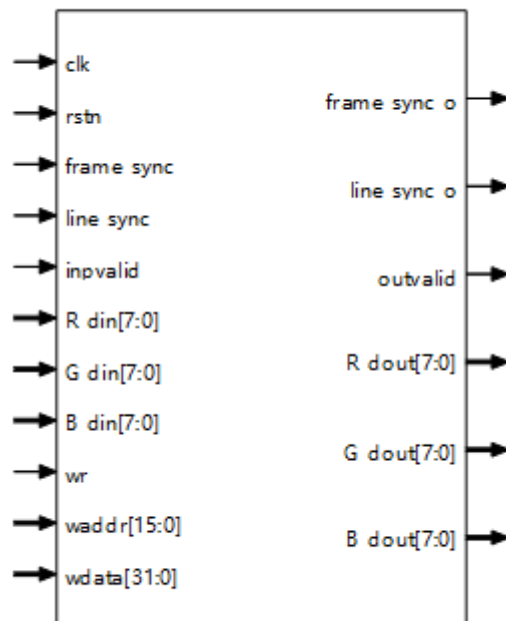


Table 4-1 I/O List of Gowin Gamma Correction IP

Signal	I/O	Data Width	Description
clk	I	1	Input clock signal
rstn	I	1	Reset signal, active-low
frame_sync	I	1	Input frame synchronization signal
line_sync	I	1	Input line synchronization signal
inpvalid	I	1	Input data valid signal
R_din	I	Changeable	Input image data signal
G_din	I	Changeable	Input image data signal
B_din	I	Changeable	Input image data signal

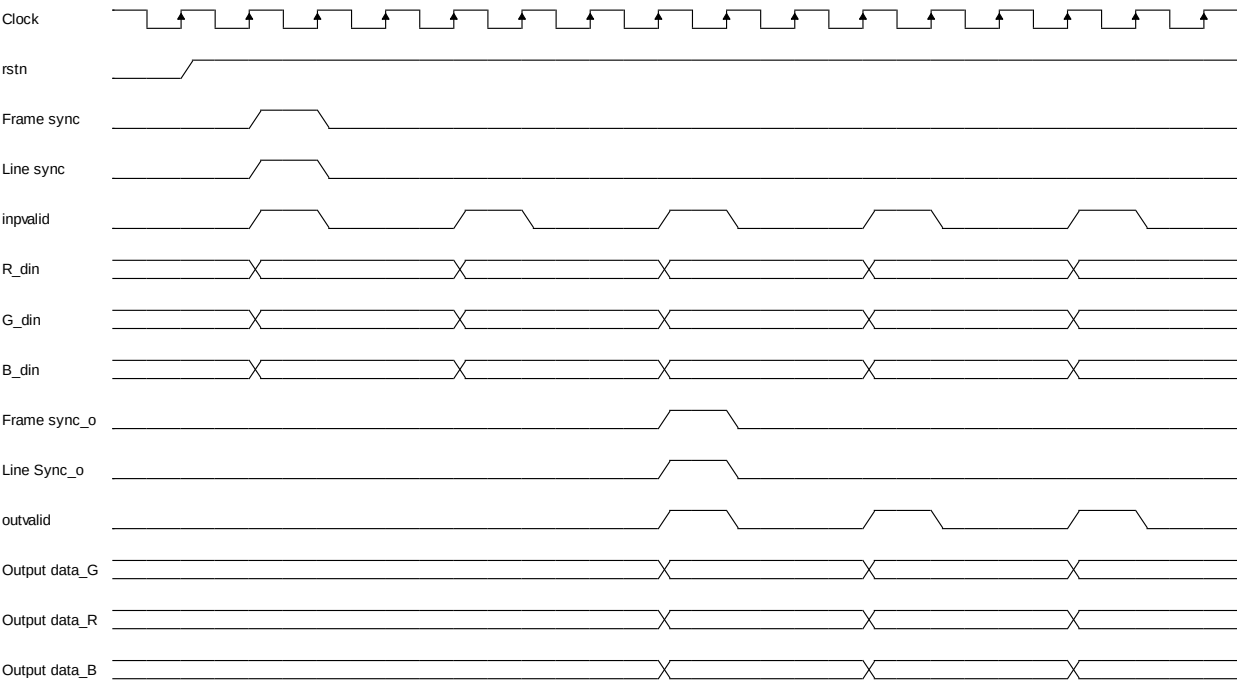
Signal	I/O	Data Width	Description
wr	I	1	Write signal
waddr	I	16	Write address signal
wdata	I	32	Write data signal
frame_sync_o	O	1	Output frame synchronization signal
line_sync_o	O	1	Output line synchronization signal
outvalid	O	1	Output valid signal; when high, the output signal is valid.
R_dout	O	Changeable	Output image data signal
G_dout	O	Changeable	Output image data signal
B_dout	O	Changeable	Output image data signal

5Timing Description

This chapter mainly introduces the timing of Gowin Gamma Correction IP.

After operating, IP will output the data with a latency. The input data requires at least three cycles to be stable and the timing is as shown in Figure 5-1.

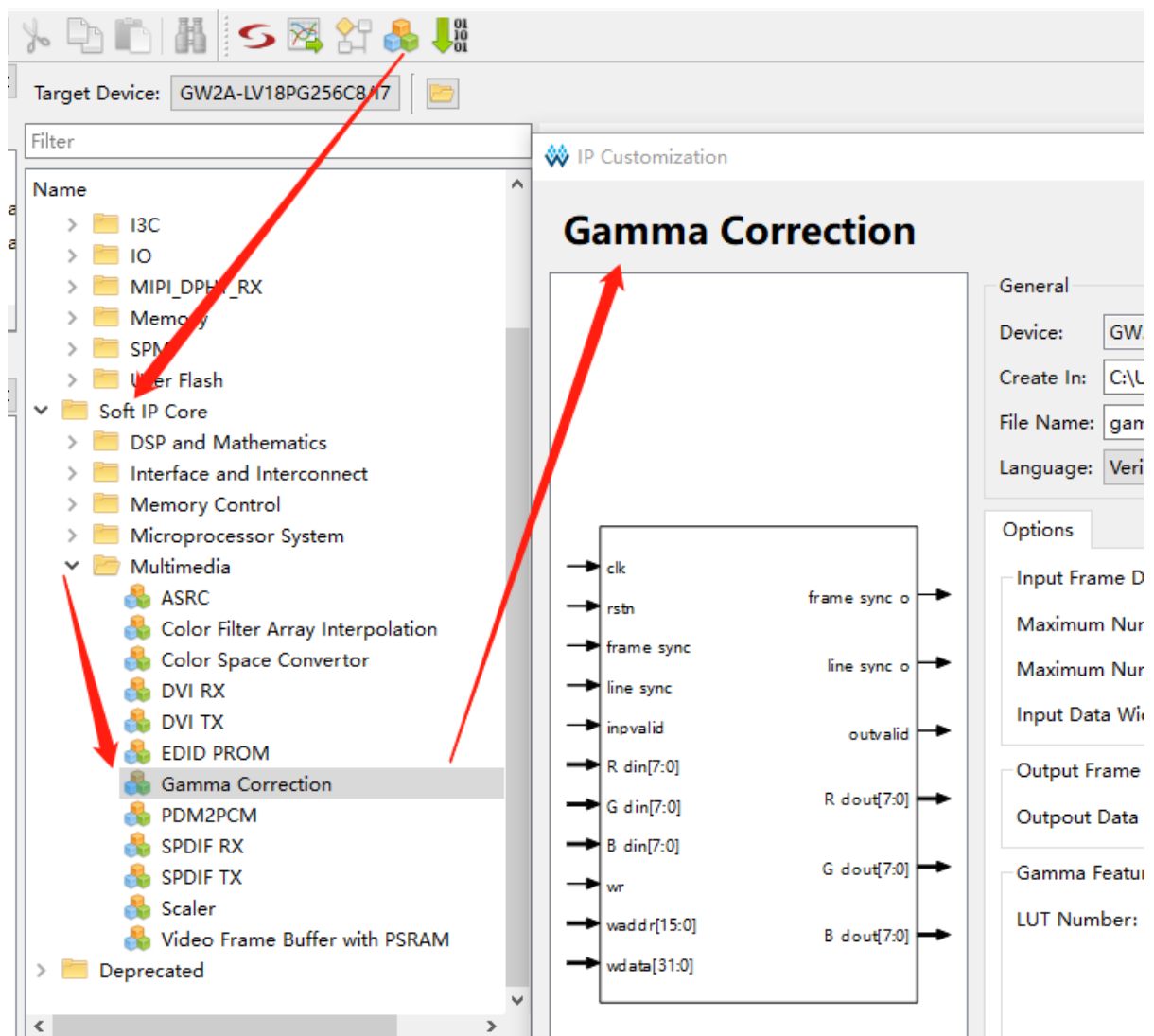
Figure 5-1 Gamma Correction IP Timing



6_{GUI}

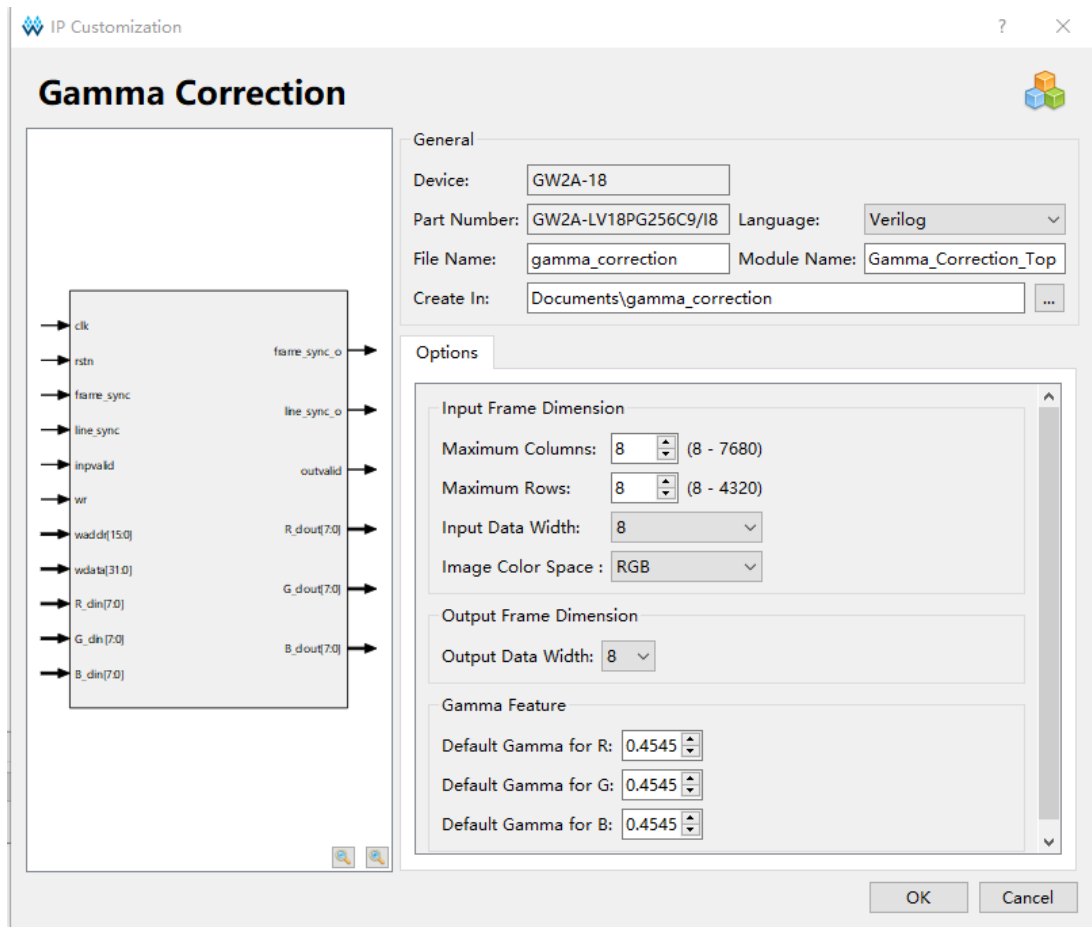
Click "Tools > IP Core Generator > Multimedia > Gamma Correction" to call and configure Gowin Gamma Correction IP. Toolbar icon is also available as shown in Figure 6-1.

Figure 6-1 Open GUI Via Icon



Gowin Gamma Correction IP configuration interface is shown in Figure 6-2.

Figure 6-2 Gowin Gamma Correction IP Configuration



- You can configure the generated file name by modifying the "File Name" text box.
- You can configure the module name by modifying the "Module Name" text box.
- You can configure IP working mode and other options using "Options".
The configuration options are shown in Table 6-1.

Table 6-1 Option Description

Options	Description
Maximum Number of Columns	Number of input image columns
Maximum Number of Rows	Number of input image rows
Input Data Width	Input data bit width, 8/10/12 bits.
Output Data Width	Output data bit width, 8/10/12 bits.
LUT Number	Number of LUT • 1 supports shared configuration. • 3 supports independent configuration.
Default Gamma	Default Gamma value; it can be configured independently or shared, and the range is 0~8.

7 Reference Design

Please refer to the related test cases in [RefDesign](#).

8 File Delivery

The delivery files for Gowin Gamma Correction IP include documents and reference design.

8.1 Documents

The folder contains the user guide in PDF version.

Table 8-1 Documents List

Name	Description
IPUG765, Gowin Gamma Correction IP User Guide	Gowin IP User Guide, namely this one.

8.2 Reference Design

The Ref. Design folder contains the netlist file, the user reference design, the constraint file, the top file, the project folder, etc.

Table 8-2 Ref. Design Folder

Name	Description
exp.v	Top module and excitation generation module of reference design
gamma_correction.vo	Gowin Gamma Correction IP netlist file
demo.cst	Project physical constraints file
fpga_project.gao	Capture the output data of Gamma Correction
gamma_correction	Gamma Correction IP project folder

