



Gowin Customized PHY IP

Release Note

RN1024-1.0E, 07/21/2023

Copyright © 2023 Guangdong Gowin Semiconductor Corporation. All Rights Reserved.

GOWIN is a trademark of Guangdong Gowin Semiconductor Corporation and is registered in China, the U.S. Patent and Trademark Office, and other countries. All other words and logos identified as trademarks or service marks are the property of their respective holders. No part of this document may be reproduced or transmitted in any form or by any means, electronic, mechanical, photocopying, recording or otherwise, without the prior written consent of GOWINSEMI.

Disclaimer

GOWINSEMI assumes no liability and provides no warranty (either expressed or implied) and is not responsible for any damage incurred to your hardware, software, data, or property resulting from usage of the materials or intellectual property except as outlined in the GOWINSEMI Terms and Conditions of Sale. GOWINSEMI may make changes to this document at any time without prior notice. Anyone relying on this documentation should contact GOWINSEMI for the current documentation and errata.

Revision History

Date	Version	Description
07/21/2023	1.0E	Initial version published.

Contents

Contents i

1 About This Guide 1

2 Overview 2

3 Documentation..... 3

4 IP Support..... 4

1 About This Guide

This release includes Gowin Customized PHY IP user guide and reference design.

Gowin Customized PHY IP user guide and reference design can be downloaded from the Gowin website, and the reference design has been configured with specific parameters that can be used for simulation, synthesis, placement and routing after adding user design.

2 Overview

Gowin Customized PHY IP supports flexible configuration of Gowin SerDes functions such as Line Rate, Reference Clock, Data Width, 8B10B Encoding/Decoding, Channel Bonding and RX Clock Correction, etc.

Function	Description
Front-end synthesis tool: GowinSynthesis	
Customized PHY supported	● Supports line rate configuration with the range 1Gbps~12.5Gbps ● Supports reference clock frequency configuration with the range 50MHz~800MHz ● Supports PLL with options of CPLL or QPLL ● Supports user data widths of 8/10/16/20/32/40/64/80 ● Supports 8B10B encoding and decoding ● Supports Word Alignment ● Supports Channel Bonding ● Supports RX Clock Correction
Back-end placement and routing tool: Gowin Software (V1.9.9.Beta-1 and above)	
Enhancements	—

3 Documentation

The software release file contains Gowin Customized PHY IP user guides, which are listed below:

Documents	Description
IPUG1024, Gowin Customized PHY IP User Guide	PDF
RN1024, Gowin Customized PHY IP Release Note	PDF

4 IP Support

Since the requirements of user design and the maximum frequency are different, the reference design does not include FPGA specific location (.cst) and timing constraints (.sdc) documents, and you can determine the location and timing constraints on your own.

For the customized IP design and support, please contact Gowin sales and support.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

