



Gowin PID Controller 3p3z IP

User Guide

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Revision History

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1 About This Guide

1.1 Purpose

Gowin PID Controller 3p3z IP User Guide includes the descriptions of the functions, features, ports, timing, call and configuration, and reference design, etc. It helps users quickly learn the features and usage of Gowin Controller 3p3z IP.

1.2 Related Documents

You can find the related documents at GOWINSEMI website:

www.gowinsemi.com

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS961, GW2ANR series of FPGA Products Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)
- [DS971, GW2AN-18X& 9X Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
DSP	Digital Signal Processing
IP	Intellectual Property
RAM	Random Access Memory
LUT	Look-up Table

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Introduction to Gowin PID Controller 3p3z IP

Gowin PID Controller 3p3z IP can realize the feedback system control of three poles and three zeros, using the time division multiplexing to process the multi-channel data.

Table 2-1 Gowin PID Controller 3p3z IP

Gowin PID Controller 3p3z IP	
IP Core Application	
Logic Resource	Please refer to Table 2-2.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.8.07 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Features and Performance

2.2.1 Feature

Supports multi-channel processing

2.2.2 Max. Frequency

The max. frequency of Gowin PID Controller 3p3z IP is mainly determined by speed grade of the selected devices, and it can reach up to 100MHz.

2.2.3 Latency

The latency of Gowin PID Controller 3p3z IP is about twelve clock cycles.

2.2.4 Resource Utilization

Gowin PID Controller 3p3z IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speed grades or the different modes of IP configuration.

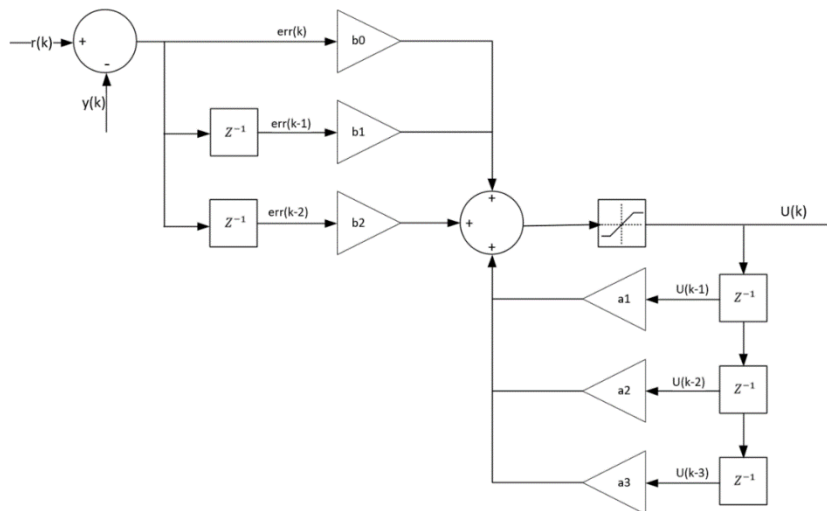
Take GW2A-55 series of FPGA as an example. See Table 2-2 for the resource utilization. For the applications on the other GOWINSEMI devices, see the later release.

Table 2-2 Gowin PID Controller 3p3z IP Resource Utilization

Device	Speed Grade	Name	Resource Utilization	Note
GW2A-55	-7	Registers	1183	Data Width=16 Parameter Fractional width= 8 Input Channel = 3
		LUT	723	
		ALU	70	
		DSP	1	
		BSRAM	0	

3 Introduction to PID Controller 3p3z Algorithm

Figure 3-1 Algorithm Control Schematic



Gowin PID Controller 3p3z IP can realize the feedback system control of three poles and three zeros. As shown in Figure 3-1, the actual value $r(k)$ and reference value $y(k)$ produce an error $err(k)$, and the controller performs the error control through the proportion parameters b_0 , b_1 , b_2 and a_1 , a_2 , a_3 .

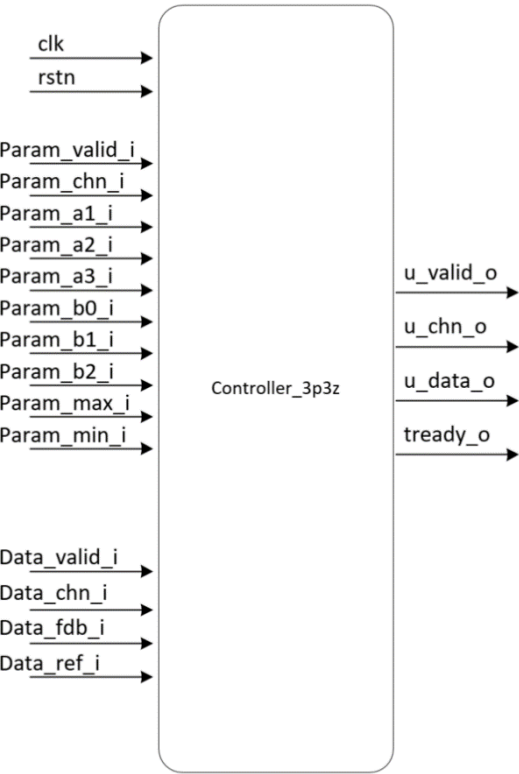
The formula is:

$$U(k) = b_0 \times err(k) + b_1 \times err(k-1) + b_2 \times err(k-2) + a_1 \times U(k-1) + a_2 \times U(k-2) + a_3 \times U(k-3)$$

4 Port Description

The I/O port of Gowin PID Controller 3p3z IP is shown in Figure 4-1.

Figure 4-1 Gowin PID Controller 3p3z IP Port Diagram



For the details of I/O port , see Table 4-1.

Table 4-1 I/O Port List of Gowin PID Controller 3p3z IP

Signal	I/O	Data Width	Description
clk	Input	1	Working clock
rstn	Input	1	Reset signal, asynchronous, active-low. Synchronous reset and asynchronous release is

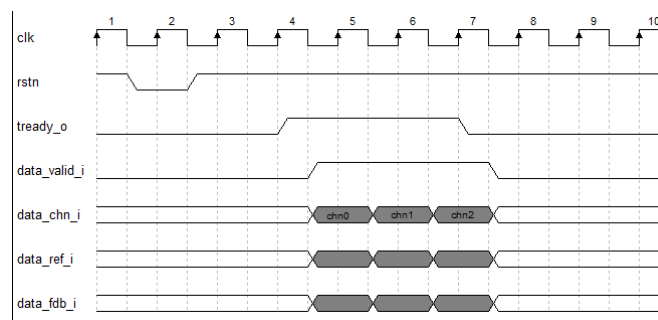
Signal	I/O	Data Width	Description
			recommended.
Parameter setting input signal			
Param_valid_i	Input	1	Input valid signal
Param_chn_i	Input	2	Input channel
Param_a1_i	Input	16	a1 input data
Param_a2_i	Input	16	a2 input data
Param_a3_i	Input	16	a3 input data
Param_b0_i	Input	16	b0 input data
Param_b1_i	Input	16	b1 input data
Param_b2_i	Input	16	b2 input data
Param_max_i	Input	16	Output maximum
Param_min_i	Input	16	Output minimum
Data input signal			
Tready_o	output	1	Input ready signal
Data_valid_i	input	1	Data input valid signal
Data_chn_i	input	2	Data input channel
Data_ref_i	input	16	Reference input value
Data_fdb_i	input	16	Feedback input value
Data output signal			
U_valid_o	Output	1	Output valid signal
U_chn_o	Output	2	Output channel
U_data_o	Output	16	Output data

5 Timing Description

This section describes the timing of Gowin PID Controller 3p3z IP.

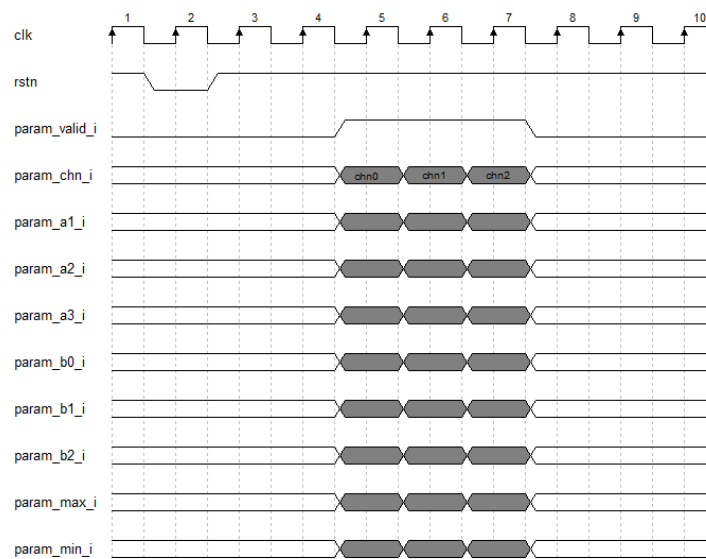
Figure 5-1 shows the timing diagram of three-channel data input of Gowin PID Controller 3p3z.

Figure 5-1 Timing Diagram of Three-channel Data Input



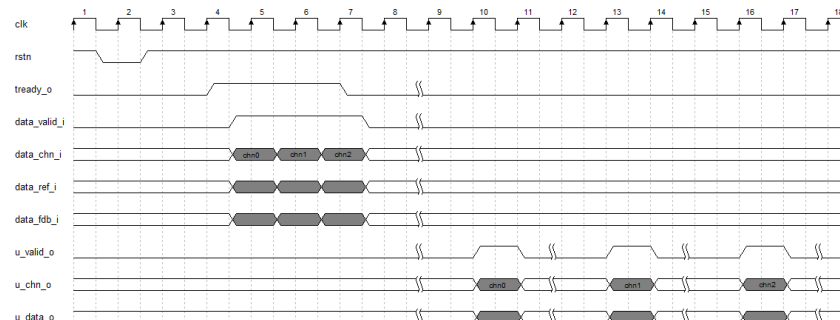
1. After the signal tready_o is high, the data can be input.
2. When the signal data_valid_i is high, the data input is valid.
3. The data need to be input in sequence corresponding to its channel.

Figure 5-2 shows the timing diagram of parameter configuration.

Figure 5-2 Timing Diagram of Parameter Configuration

1. The parameter needs to be input before data processing, not during data processing.
2. When the signal **param_valid_i** is high, the input data is valid and the data must correspond to its channel input.
3. If the parameter is reset, the signal **rstn** should be pulled down to reset once.

Figure 5-3 shows the timing diagram of the output of Gowin PID Controller 3p3z.

Figure 5-3 Timing Diagram of the Output of Gowin PID Controller 3p3z IP

1. When the output valid signal is high, the output data is valid.
2. Each channel data will be output sequentially in order of channel.
3. There will be at least 3 cycle intervals for the inter-channel data outputs.

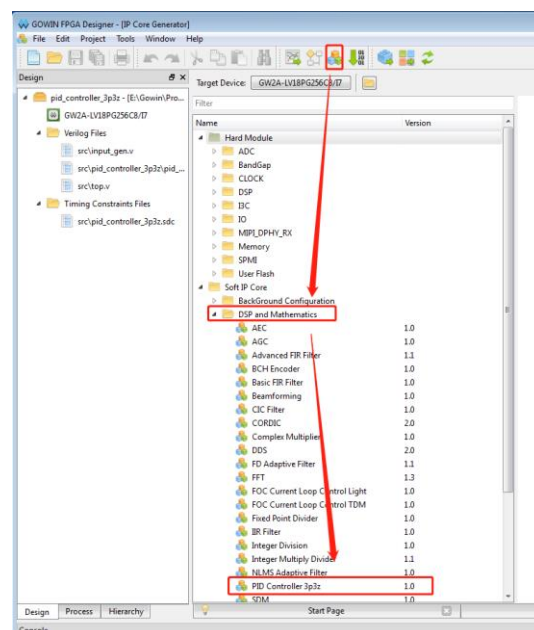
6 Invoke and Configure IP

In “Tools” menu bar of Gowin Software interface, you can start the “IP Core Generator” tool to invoke and configure PID Controller 3p3z.

1. Open IP Core Generator

After creating a new project, click the IP Core Generator button to open the IP Core Generator, as shown in Figure 6-1.

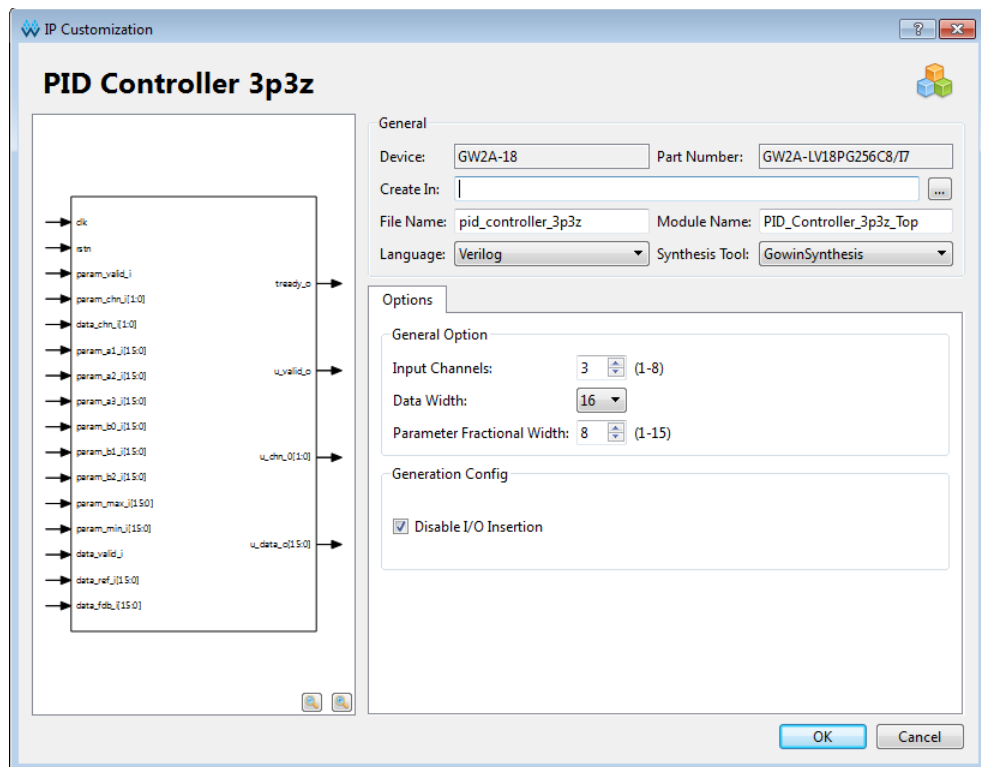
Figure 6-1 IP Core Generator Interface



2. Open PID Controller 3p3z IP core

Click “DSP and Mathematics”, double-click “PID Controller 3p3z” to open PID Controller 3p3z IP, as shown in Figure 6-2.

Figure 6-2 PID Controller 3p3z Interface



3. PID Controller 3p3z IP core configuration

- Input channel configuration
- Input data width configuration
- Parameter fractional width configuration

7 Reference Design

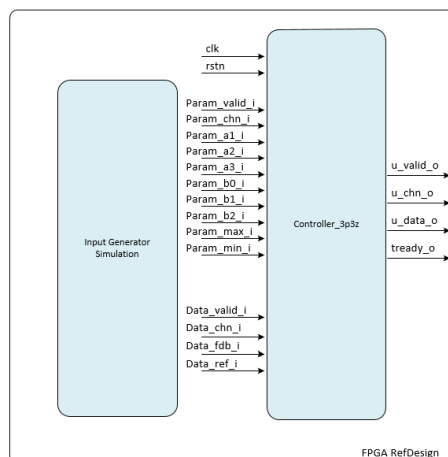
This chapter is intended to introduce the example and usage of Gowin PID Controller 3p3z reference design. Gowin PID Controller 3p3z design example has only one module; for the details, see the [reference design](#).

Application

The block diagram of reference design is as shown in Figure 7-1. In the design instance, the steps are as follows:

1. The timing of parameter setting is simulated via the Input Generator Simulation module and input to the PID Controller_3p3z module.
2. The timing of data generation is simulated via the Input Generator Simulation module and is input to the PID Controller_3p3z module.
3. After the operation by IP, the output data is obtained.

Figure 7-1 Block Diagram of Reference Design



PID Controller_3p3z functions can be verified using this design. When the reference design is applied to board level testing, you need to provide appropriate stimulus to the reference design, and you can use an on-line logic analyzer or oscilloscope to observe the signals.

