DK_START_GW2AN-UV9XUG400C7I6_V1.0

User Guide

DBUG411-1.0.2E, 12/07/2023

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Revision History

Date	Version	Description
02/02/2023	1.0E	Initial version published.
03/17/2023	1.0.1E	Chapter 4 “Quick Start” removed.
12/07/2023	1.0.2E	“Figure 3-2 Clock and Reset Connection Diagram” in “3.4 Clock and Reset” updated.

Contents

List of Figures

List of Tables

1 About This Guide

1.1 Purpose

The DK_START_GW2AN-UV9XUG400C7I6_V1.0 development board (hereinafter referred to development board) user guide consists of following three parts:

- A brief introduction to the features of the development board;
- An introduction to the development board system architecture and hardware resources;
- An introduction to the hardware circuits, functions and pinout.

1.2 Supported Products

The information presented in this guide applies to GW2AN-UV9XUG400 device.

1.3 Related Documents

You can find the related documents at www.gowinsemi.com:

- DS971, GW2AN-18X and GW2AN-9X Data Sheet
- UG978, GW2AN-9X Pinout
- UG973, GW2AN-18X and GW2AN-9X Package & Pinout User Guide
- UG290, Gowin FPGA Products Programming and Configuration Guide
- SUG100, Gowin Software User Guide

1.4 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
BSRAM	Block Static Random Access Memory
DDR	Double Data Rate
DSP	Digital Signal Processing
FLASH	Flash Memory
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable Input/Output
LDO	Low Dropout Regulator
LUT4	Four-input Look-up Table
LVDS	Low-Voltage Differential Signaling
SSRAM	Shadow Static Random Access Memory

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

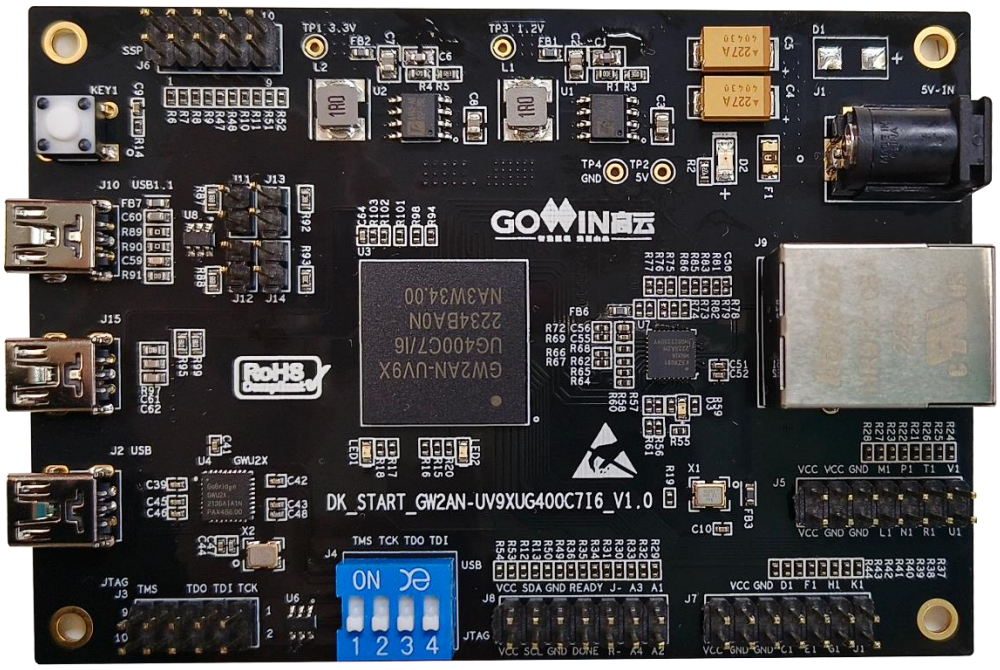
Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Development Board Introduction

2.1 Overview

Figure 2-1 DK_START_GW2AN-UV9XUG400C7I6_V1.0 Development Board



DK_START_GW2AN-UV9XUG400C7I6_V1.0 development board is embedded with GW2AN-UV9XUG400 chip. It can apply to USB 1.1 communication, USB 2.0 communication, industrial Ethernet communication, 9X series FPGA function evaluation, hardware reliability verification, and software learning and debugging.

The GW2AN series of FPGA products are the first generation non-volatile products of the Arora® family. They offer a range of comprehensive features and rich internal resources like high-speed LVDS interfaces, abundant BSRAM memory, and NOR Flash. These embedded resources combine a streamlined FPGA architecture with a 55nm process

to make the GW2AN series of FPGA products suitable for high-speed, low-cost applications.

The development board has the following features:

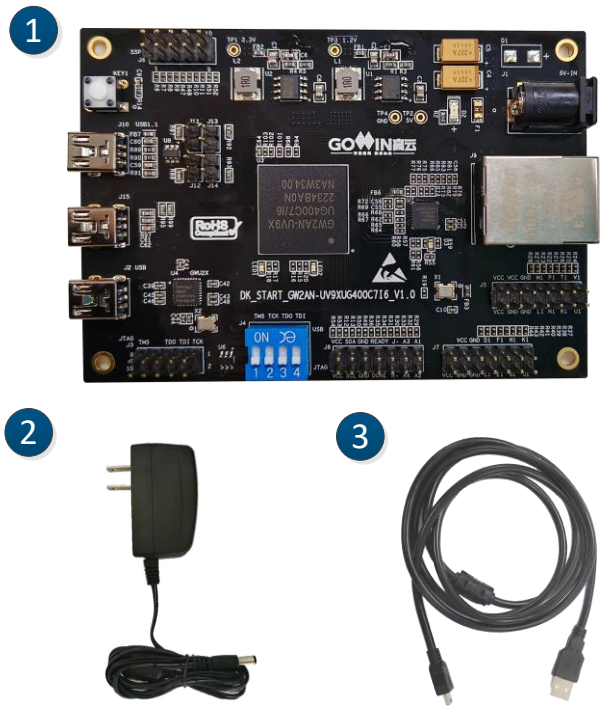
- An industrial Ethernet PHY chip supporting 10M/100M industrial Ethernet communication
- Include one USB 1.1 interface and one USB 2.0 interface, supporting USB-to-Ethernet Communication
- Support JTAG download
- Reserve GPIO interfaces, LEDs and keys to facilitate user test

2.2 A Development Board Kit

The development board suite includes the following items:

1. DK_START_GW2AN-UV9XUG400C7I6_V1.0 Development Board
2. 5V power (Input: 100-240V~50/60Hz 0.5A, output: DC 5V 2A)
3. USB Mini B Cable

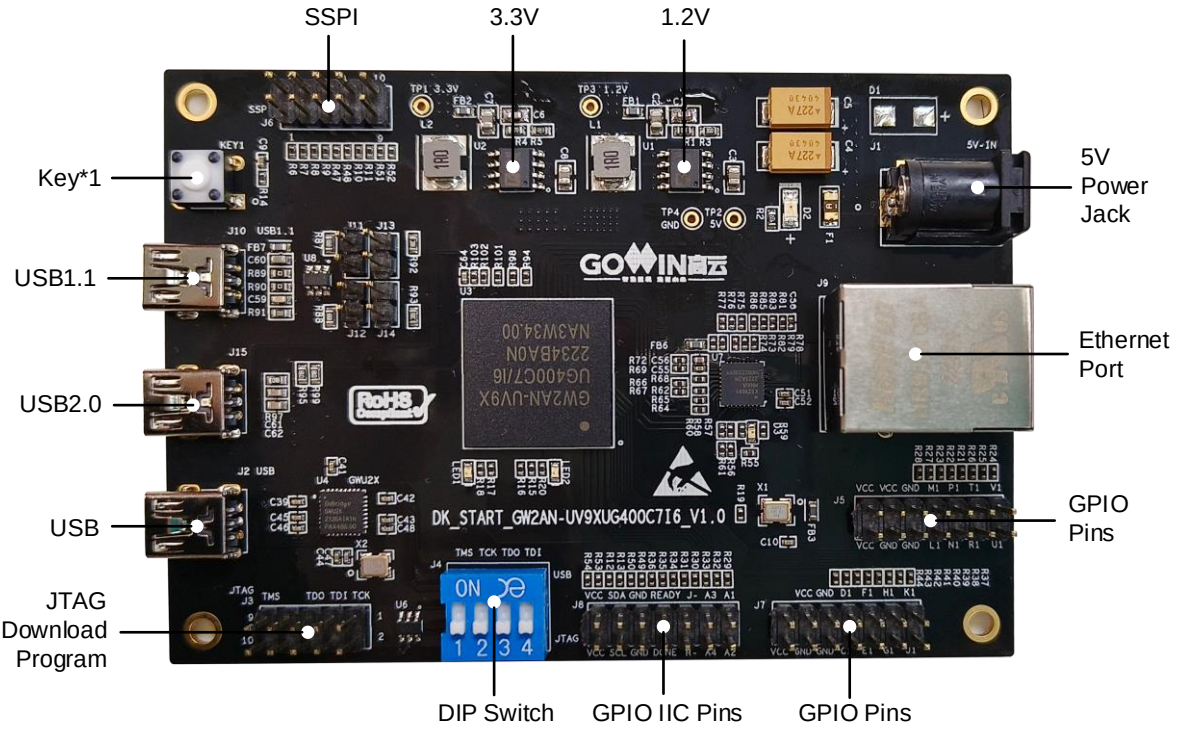
Figure 2-2 A Development Board Kit



① DK_START_GW2AN-UV9XUG400C7I6_V1.0 Development Board
② 5V Power Supply
③ USB Mini B Data Cable

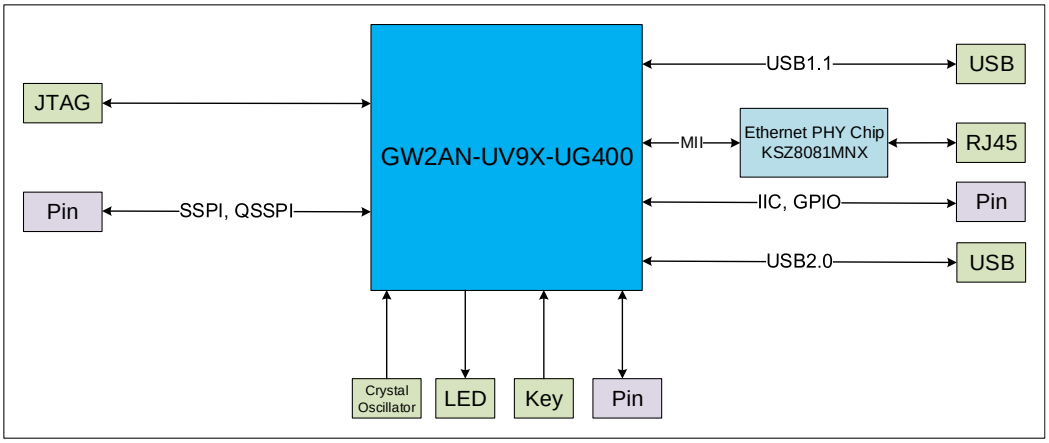
2.3 PCB Components

Figure 2-3 PCB Components



2.4 System Block Diagram

Figure 2-4 System Block Diagram



2.5 Features

The key features are as follows:

1. The FPGA device
   - Gowin GW2AN-UV9XUG400 FPGA
   - Max. user I/O: 335
2. Download and Boot
   - The board includes a download module. You can use JTAG downloader to download the program.
   - Blue DONE light (LED1) will be on when programming or configuration is complete.
3. Power
   - External DC 5V 2A
   - The LED is on after power on
   - The development board provides 5.0V, 3.3V, and 1.2V power.
4. Clock system
   12MHz crystal oscillator provides clock input for GW2AN-UV9XUG400
5. Ethernet interface
   - One Ethernet interface
   - Adopt KSZ8081MNX Ethernet chip (10/100MHz)
   - RJ45 interface
6. GPIO Interface

   Reserve four sets of GPIOs, including one set of GPIOs with SSPI interface, three sets of common GPIOs. There are 32 pins in total.
7. Debug module
   - 1 key
   - 1 LED (LED2)
8. USB 1.1 communication

   Support communication with FPGA through USB 1.1 interface
9. USB 2.0 communication

   Support communication with FPGA through USB 2.0 interface

3 Development Board Circuit

3.1 FPGA Module

Overview

For the resources of GW2AN-UV9XUG400 FPGA products, please refer to *DS971, GW2AN-18X and GW2AN-9X Data Sheet*.

I/O BANK Introduction

For the I/O BANK, package, and pinout information, see *UG973, GW2AN-18X and GW2AN-9X Package & Pinout User Guide* for more details.

3.2 Download Module

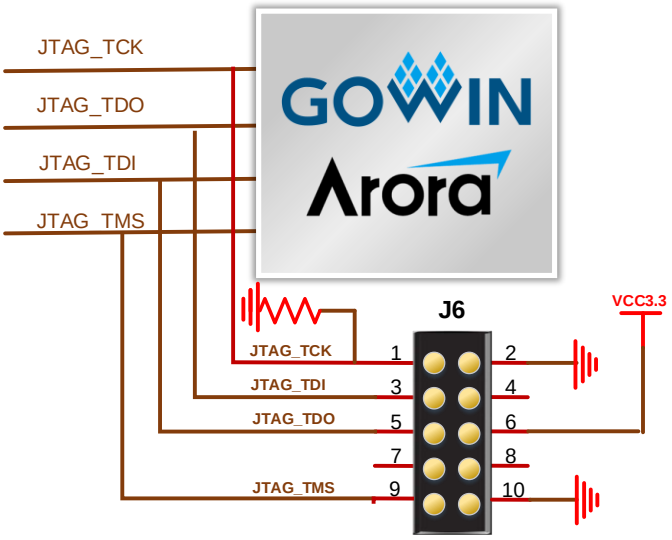
3.2.1 Introduction

The development board provides a JTAG download interface. The MODE value of the GW2AN-9X is fixed.

Download the program to the on-chip SRAM or Flash. If downloaded to SRAM, the data stream file will be lost when the device is powered down. While downloaded to Flash, the data stream file will not be lost after power down.

LED1 connected with DONE will be on after the program download is complete.

Figure 3-1 JTAG Download Connection Diagram



3.2.2 Pinout

Table 3-1 FPGA Download and Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
JTAG_TCK	C9	0	3.3V	JTAG Signal
JTAG_TDO	E8	0	3.3V	JTAG Signal
JTAG_TDI	C7	0	3.3V	JTAG Signal
JTAG_TMS	D9	0	3.3V	JTAG Signal

3.3 Power Supply

3.3.1 Introduction

The development board is powered via a power adapter. The input parameter is 100-240V~50/60MHz 0.5A, and the output is DC +5V 2A.

The input 5V power can generate 3.3V and 1.2V via the power transfer chip on the development board.

Convert DC+5V to DC+3.3V via FP6165ADXR-G1 chip and its peripheral circuit with maximum output current of 3A.

Convert DC+3.3V to DC+1.2V via FP6165ADXR-G1 chip and its peripheral circuit with maximum output current of 3A.

3.4 Clock and Reset

3.4.1 Introduction

The development board offers a 12MHz active crystal oscillator connected to the global clock pins.

You can reset with the reset key (automatic reset when power on).

Figure 3-2 Clock and Reset Connection Diagram

3.4.2 Pinout

Table 3-2 Clock and Reset Pins Distribution

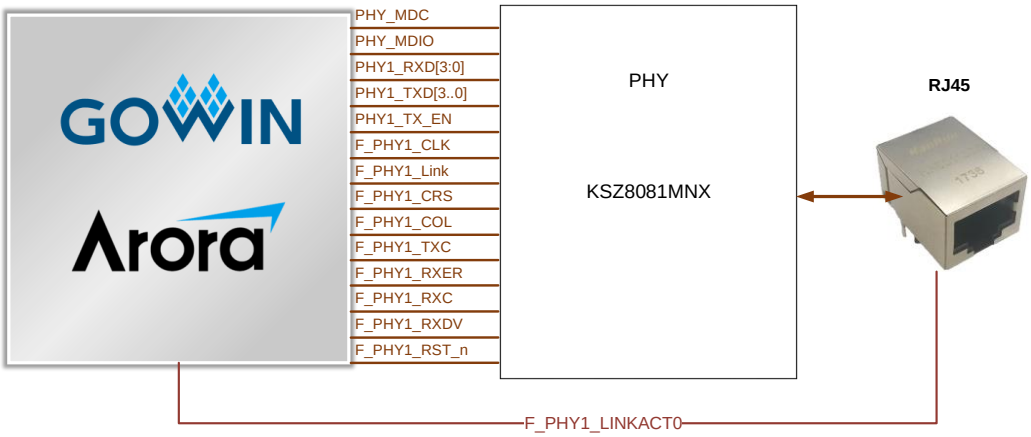
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_CLK	E2	8	3.3V	12MHz active crystal oscillator input
F_RST_N	P20	8	2.5V	Reset Signal, active Low

3.5 Ethernet

3.5.1 Introduction

The development board includes one KSZ8081MNXCA-TR chip, supporting MII interface.

Figure 3-3 Connection Diagram of FPGA and Ethernet



3.5.2 Pinout

Table 3-3 Ethernet Pins Distribution

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_PHY1_Link	V10	5	3.3V	Programmable LED1
F_PHY1_CLK	W9	5	3.3V	Clock input (25M)
F_PHY_MDIO	V6	5	3.3V	Management data
F_PHY_MDC	U6	5	3.3V	Management clock
F_PHY1_RXD3	Y11	5	3.3V	Receive data 3
F_PHY1_RXD2	Y10	5	3.3V	Receive data 2
F_PHY1_RXD1	Y9	5	3.3V	Receive data 1
F_PHY1_RXD0	Y8	5	3.3V	Receive data 0
F_PHY1_RXDV	Y7	5	3.3V	Receive data valid output
F_PHY1_RXC	Y5	5	3.3V	Receive clock output
F_PHY1_RXER	Y4	5	3.3V	Receive error output
F_PHY1_TXC	Y3	5	3.3V	Transmit clock output
F_PHY1_TXEN	Y2	5	3.3V	Send enable
F_PHY1_TXD0	Y1	5	3.3V	Transmit data 0
F_PHY1_TXD1	W1	5	3.3V	Transmit data 1
F_PHY1_TXD2	W2	5	3.3V	Transmit data 2

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_PHY1_TXD3	W3	5	3.3V	Transmit data 3
F_PHY1_COL	W4	5	3.3V	Collision test
F_PHY1_CRS	W5	5	3.3V	Carrier sense
F_PHY1_RST_n	W10	5	3.3V	Chip reset
F_PHY1_LINKACT0	W11	5	3.3V	Connection network interface

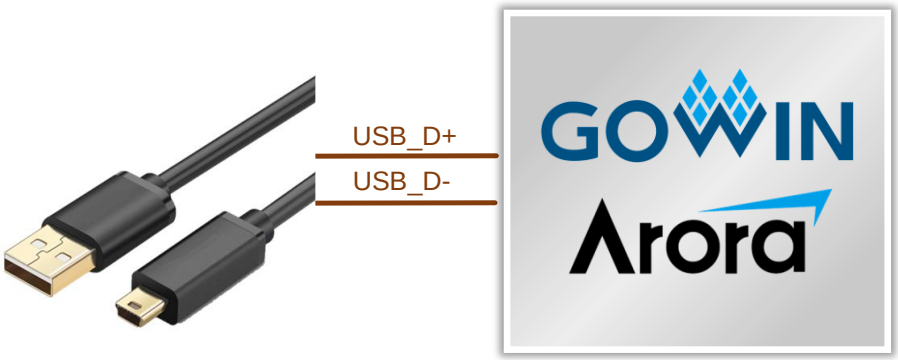
3.6 USB 1.1

3.6.1 Introduction

There is one USB 1.1 interface on the development board, which can be used for communication between FPGA and USB 1.1 interface.

USB 1.1 has two communication modes, low speed mode (1.5Mbps) and high speed mode (12Mbps). You can select the communication mode of USB1.1 by jumper cap.

Figure 3-4 USB Interface Connection Diagram



3.6.2 Pinout

Table 3-4 USB 1.1 Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
USB_D-	K20	3	3.3V	USB signal line-
USB_D+	K19	3	3.3V	USB signal line+

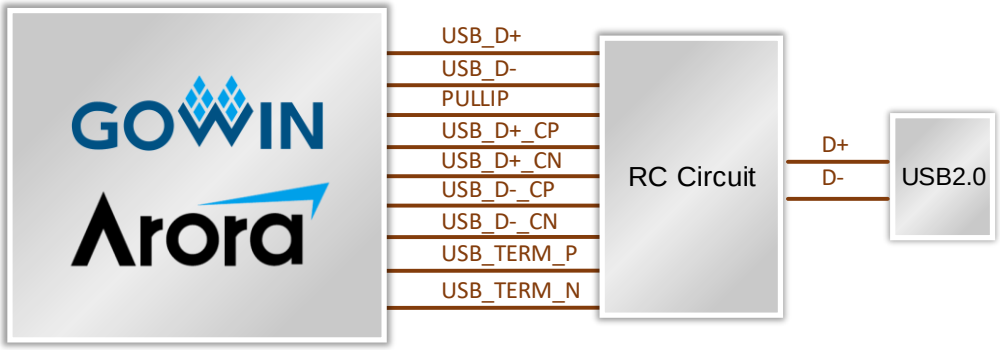
3.7 USB 2.0

3.7.1 Introduction

There is one USB 2.0 interface on the development board, which can be used for communication between FPGA and USB 1.1 interface.

The USB 2.0 interface is directly connected to the FPGA through a configuration resistor.

Figure 3-5 USB Interface Connection Diagram



3.7.2 Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
USB_Pullip	Y14	4	3.3V	VBUS detection to reset USB
USB_D+_CP	Y16	4	3.3V	USB+ signal
USB_D+/-_CN	W16	4	3.3V	USB+ reference signal
USB_D-_CP	Y17	4	3.3V	USB- signal
USB_D+/-_CN	W17	4	3.3V	USB- reference signal
USB_Term_p	V14	4	3.3V	Termination resistor control at high speed; USB data pin at full speed and low speed
USB_Term_n	U14	4	3.3V	Termination resistor control at high speed; USB data pin at full speed and low speed
USB_D+	V12	4	3.3V	USB data pin at high speed
USB_D-	V13	4	3.3V	USB data pin at high speed

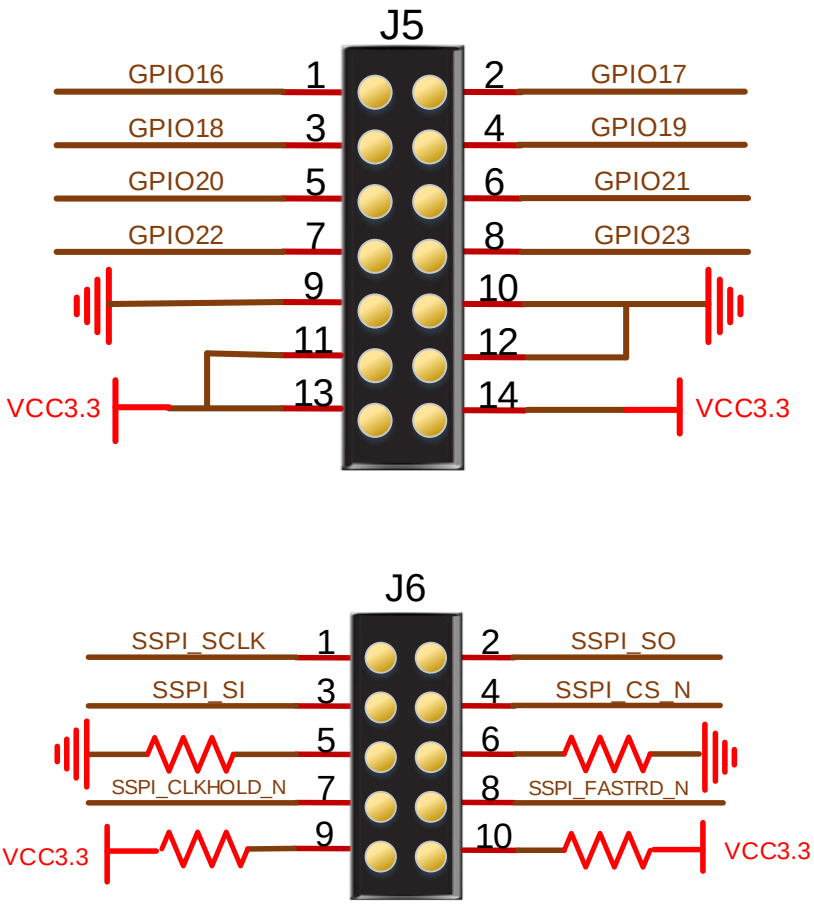
3.8 GPIO

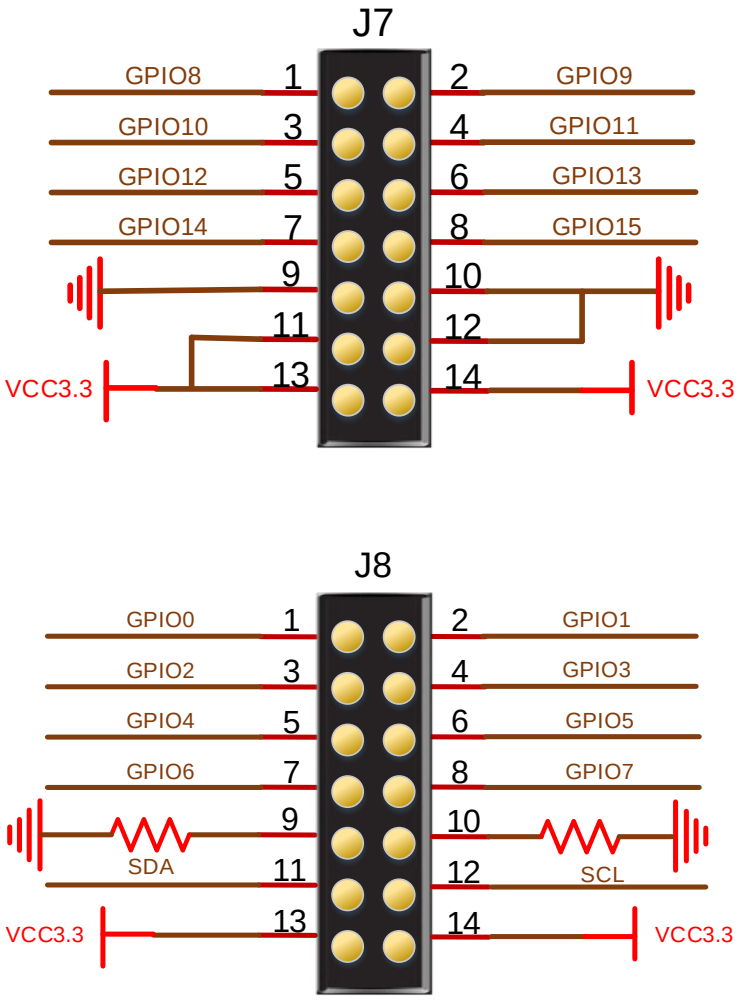
3.8.1 Introduction

In order to facilitate user testing, there are four dual-row pins with 2.54mm pitch reserved on the development board, including 14Pin pins, J5, J7, J8 and 10Pin pin, J6. There are 32 GPIO interfaces in total.

J6 pin is multiplexed pin. You can choose according to their needs.

Figure 3-6 GPIO Header Connection Diagram





3.8.2 Pinout

Table 3-5 J5 Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
GPIO16	V1	6	3.3V	General-purpose input/output
GPIO17	U1	6	3.3V	General-purpose input/output
GPIO18	T1	6	3.3V	General-purpose input/output
GPIO19	R1	6	3.3V	General-purpose input/output
GPIO20	P1	7	3.3V	General-purpose input/output
GPIO21	N1	7	3.3V	General-purpose input/output
GPIO22	M1	7	3.3V	General-purpose input/output

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
GPIO23	L1	7	3.3V	General-purpose input/output

Table 3-6 J7 Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
GPIO8	K1	7	3.3V	General-purpose input/output
GPIO9	J1	7	3.3V	General-purpose input/output
GPIO10	H1	8	3.3V	General-purpose input/output
GPIO11	G1	8	3.3V	General-purpose input/output
GPIO12	F1	8	3.3V	General-purpose input/output
GPIO13	E1	8	3.3V	General-purpose input/output
GPIO14	D1	8	3.3V	General-purpose input/output
GPIO15	C1	8	3.3V	General-purpose input/output

Table 3-7 J8 Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
GPIO0	A1	0	3.3V	General-purpose input/output
GPIO1	A2	0	3.3V	General-purpose input/output
GPIO2	A3	0	3.3V	General-purpose input/output
GPIO3	A4	0	3.3V	General-purpose input/output
GPIO4	C13	1	3.3V	General-purpose input/output
GPIO5	D13	1	3.3V	General-purpose input/output
GPIO6	C17	1	3.3V	General-purpose input/output
GPIO7	A19	1	3.3V	General-purpose input/output

Table 3-8 SSPI Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
SSPI_SCLK	W6	4	3.3V	Configuration Mode || General-purpose input/output
SSPI_SO	Y6	4	3.3V	Configuration Mode || General-purpose input/output
SSPI_SI	W20	4	3.3V	Configuration Mode || General-purpose input/output
SSPI_CS_N	Y20	4	3.3V	Configuration Mode || General-purpose input/output
SSPI_CLKHOLD_N	T14	4	3.3V	Configuration Mode || General-purpose input/output
SSPI_FASTRD_N	Y19	4	3.3V	Configuration Mode || General-purpose input/output

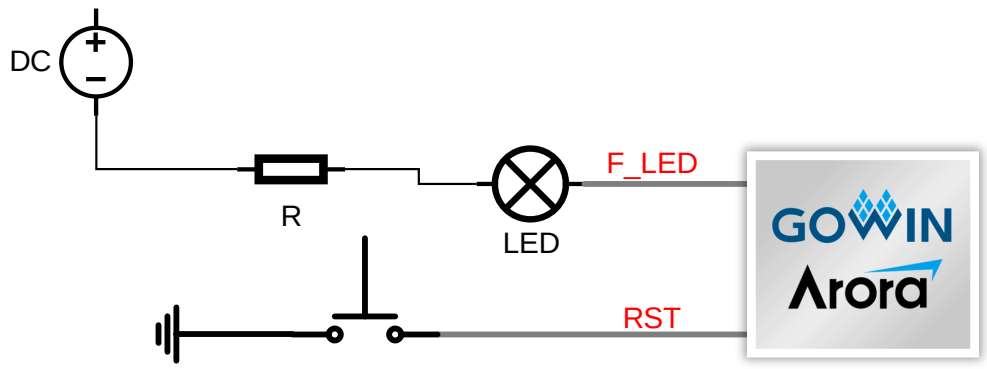
3.9 LED & Key

3.9.1 Introduction

The LED reserved in the development board connects to FPGA. The LED is lit when logic is low, while the LED is off when the logic is high.

There is one switch on the board connecting to FPGA. You can use the switch flexibly.

Figure 3-7 LED & Key Connection Diagram



3.9.2 Pinout

Table 3-9 LED & Key Module Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
F_RST_N	P20	8	3.3V	Key IO
F_LED	A10	0	3.3V	LED_IO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