Gowin USB 2.0 SoftPHY Device Peripheral Circuit Design Application Note

Overview

This application note mainly introduces the design methods of USB 2.0 SoftPHY circuits of Gowin FPGA devices, including FPGA I/O distribution, schematic design, PCB layout, reference plane design, etc., to help users quickly complete the hardware design of USB 2.0 SoftPHY circuits with good signal integrity and low noise

The Gowin USB 2.0 SoftPHY device peripheral circuit is called USB2.0-RC circuit for short in the application note.

FPGA I/O Distribution Principle

I/O Requirements of USB2.0-RC Circuit

For USB2.0-RC circuits, 11 I/Os need to be connected.

The I/O signals that need to be connected are shown in the following table.

Signal Name	Number of Required I/Os
USB_TERM_RXDP/N	2
USB_RX_D+/-	2
USB_TX_D+/-	2
USB_RXDP_D+/-	2
USB_RXDN_D+/-	2
USB_PULLUP_EN	1

I/O Distribution Rules of USB2.0-RC Circuit

Ensure that the signals (except for the signals of Arora-V series devices) of the USB2.0-RC I/O circuit are distributed on the same bank of the FPGA.

Ensure that the differential signals of the USB2.0-RC I/O circuit are placed on the TRUE LVDS pin of the FPGA.

When the FPGA chip belongs to the LittleBee or Arora family, the adjacent differential pair (the differential pair with a smaller numerical designation in the pin name) of the pins used for the USB_RX_D+/- differential signal must exist and remain unused. For example, on the GW1N-9 chip, if the USB_RX_D+/- differential signal is assigned to the IOB13A and IOB13B pins, then the IOB12A and IOB12B pins must exist and remain unused.

The following figure shows the pinout of the GW1N-9 chip. When the FPGA is in the LQ144 package, if the USB_RX_D+/- differential signal is assigned to pins 46 and 47, then pins 44 and 45 must remain unconnected. When the FPGA is in the LQ100 package, the USB_RX_D+/- differential signal is assigned to pins 31 and 32, and pins IOB12A and IOB12B exist but are not routed out, which meets the requirement that the adjacent differential pair exists and remains unused.

Pin Name	Function	BANK	Differential Pair	LVDS	X16	LQ100	LQ144
IOB12A	I/O	2	True_of_IOB12B	NONE	NONE		44
IOB12B	I/O	2	Comp_of_IOB12A	NONE	NONE		45
IOB13A	I/O	2	True_of_IOB13B	TRUE	x16	31	46
IOB13B	I/O	2	Comp_of_IOB13A	TRUE	NONE	32	47

3. Schematic Design

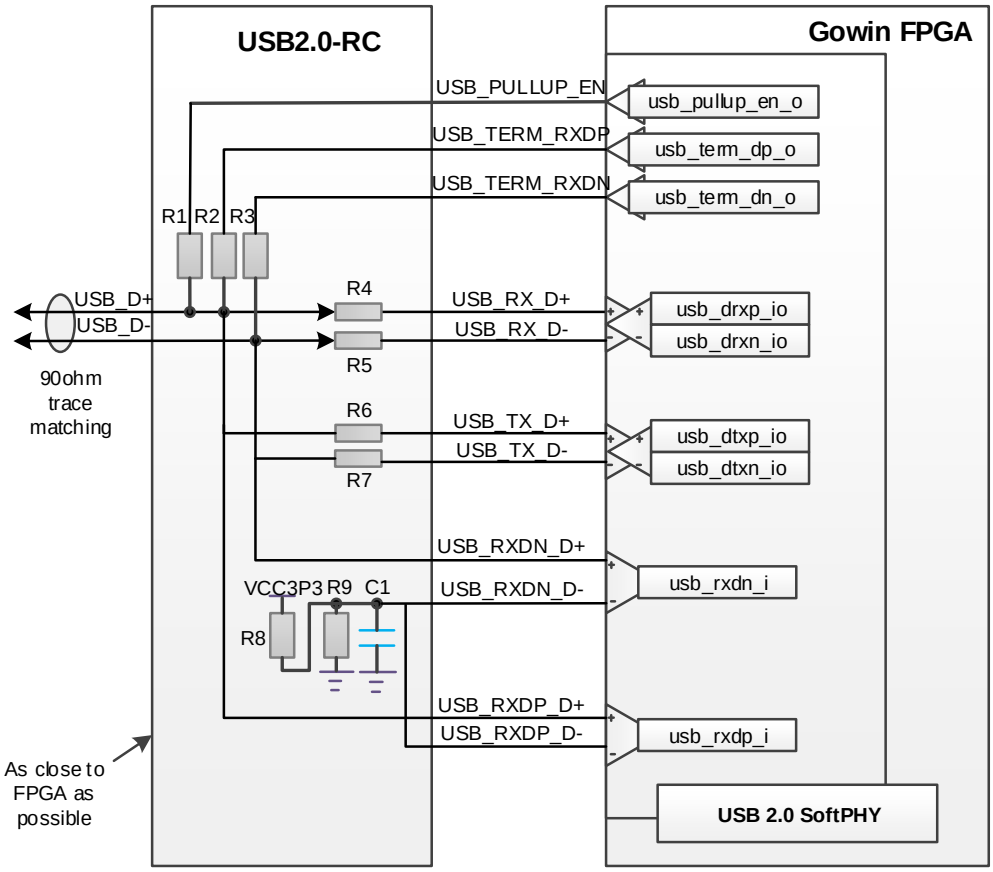
Bank Voltage Distribution

The bank voltage of Gowin FPGA connected to the USB2.0-RC circuit is 3.3V.

USB2.0-RC Circuit Design

Different series of Gowin FPGA chips have different resistance values for external USB2.0-RC circuits.

The schematic diagram of USB2.0-RC circuit connection is shown in the following figure.



Note!

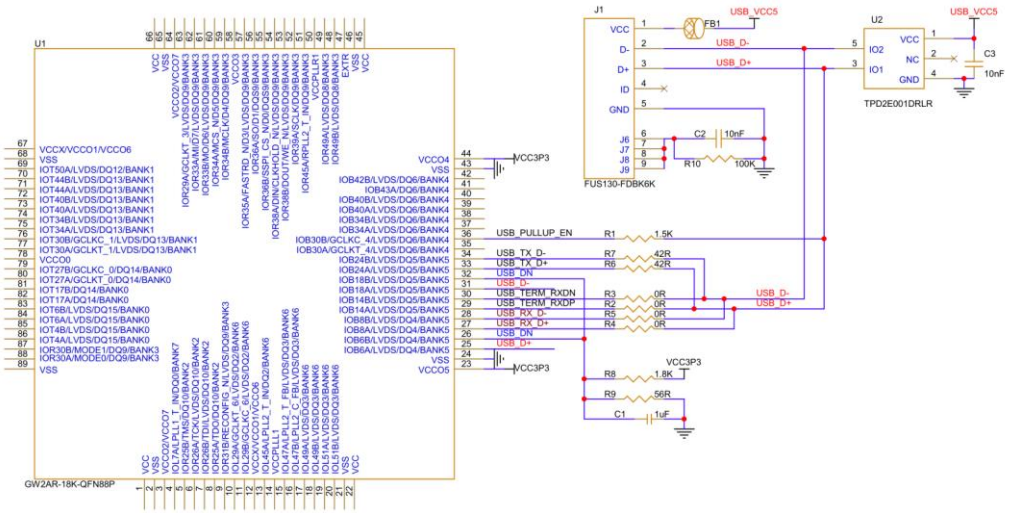
- Resistance accuracy is 1%, capacitance accuracy is 20%.
- It is recommended to select 0402 for the package size of the resistor capacitor.

The resistance values of USB2.0-RC circuit are shown in the following table.

Device	LittleBee	Arora	Arora-V
R1	1.5K ohm	1.5K ohm	1.5K ohm
R2	0 ohm	0 ohm	36 ohm
R3	0 ohm	0 ohm	36 ohm
R4	0 ohm	0 ohm	0 ohm
R5	0 ohm	0 ohm	0 ohm
R6	42 ohm	42 ohm	100 ohm
R7	42 ohm	42 ohm	100 ohm
R8	1.8K ohm	1.8K ohm	1.8K ohm
R9	75 ohm	56 ohm	75 ohm
C1	1uF	1uF	1uF

Schematic Reference Design

The following diagram is a schematic reference design for the USB 2.0 RC circuit. The FPGA chip used is the Gowin GW2AR-18-QFN88P, the USB connector model is FUS130-FDBK6K, and the ESD protection device model is TPD2E001DRLR. This schematic design is for reference only.



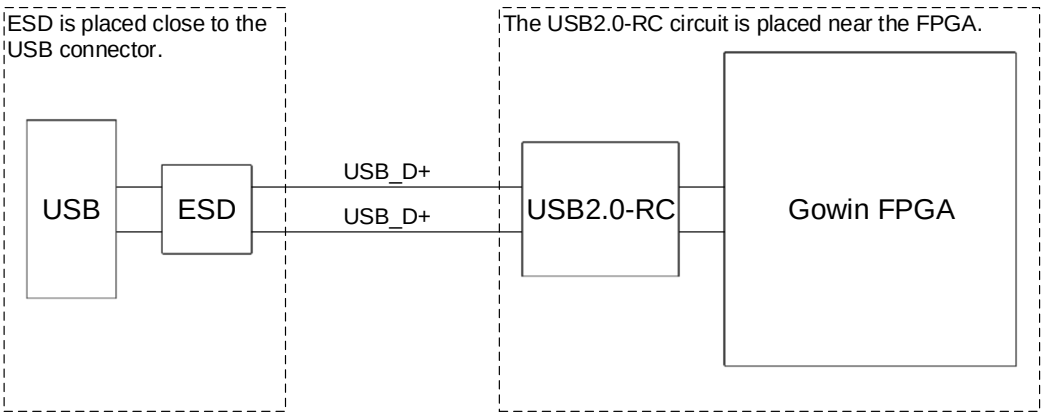
PCB Design

Device Placement

The placement of the device directly affects the difficulty of routing, and reasonable placement not only makes the routing easier, but also makes the routing shorter and has fewer vias, which ultimately improves the communication quality of the signal.

The resistor capacitors of the USB2.0-RC circuit are placed as close to the FPGA as possible.

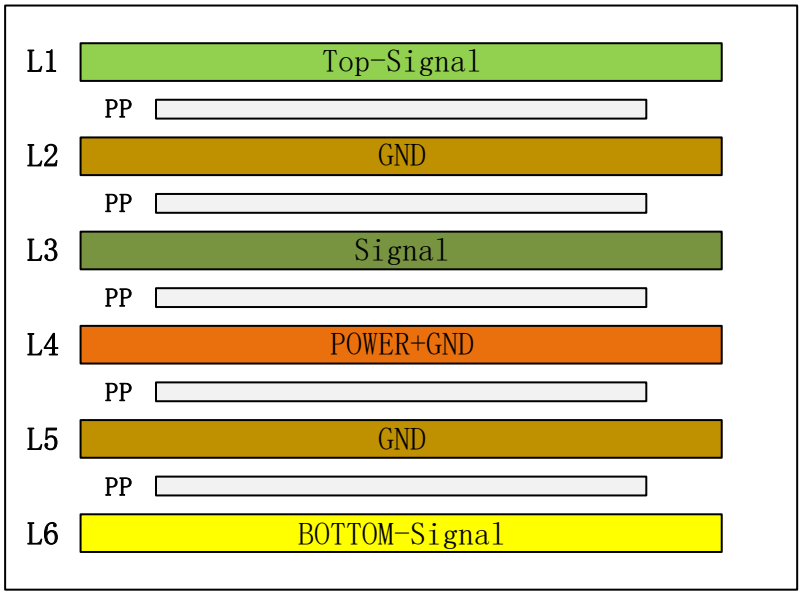
The schematic diagram of Gowin FPGA and USB2.0-RC circuit placement is shown in the following figure.



PCB Stack-up

A good PCB stack-up is the key to eliminating noise interference. The GND reference layer provides a low-impedance return path for digital circuitry. All signals are routed to the GND layer as much as possible. The design adopts a 6-layer stack-up structure as shown in the following figure. The 1st, 3rd, and 6th layers are the signal layers, the 2nd and 5th layers are complete GND layers, and the 4th layer is a shared layer for power and GND.

The USB 2.0-RC circuit connected to the FPGA is routed at 1st, 3rd, and 6th layers and the reference planes are selected at 2nd, 4th and 5th layers. The differential signal of the USB2.0-RC circuit should have a complete GND reference layer.



Signal Routing

The impedance of the single-ended signal of the USB2.0-RC circuit is 50Ω, and the impedance of the differential signal is 90Ω.

The wiring of the differential signal of USB2.0-RC circuit should be processed of equal length, and the error should be controlled within ± 10mil.

USB2.0-RC circuit differential signal in the process of wiring, if the layer is changed, 2~4 GND vias can be placed next to the vias to reduce the reflow path, improve signal integrity and reduce electromagnetic radiation.

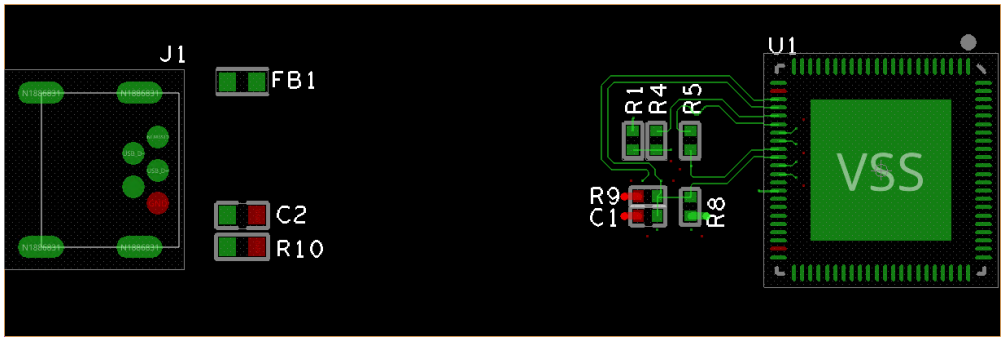
The USB2.0-RC circuit device can be hollowed out directly below to accommodate impedance changes.

USB2.0-RC circuit signal trace should have a complete GND reference layer, the reference layer discontinuity will lead to the

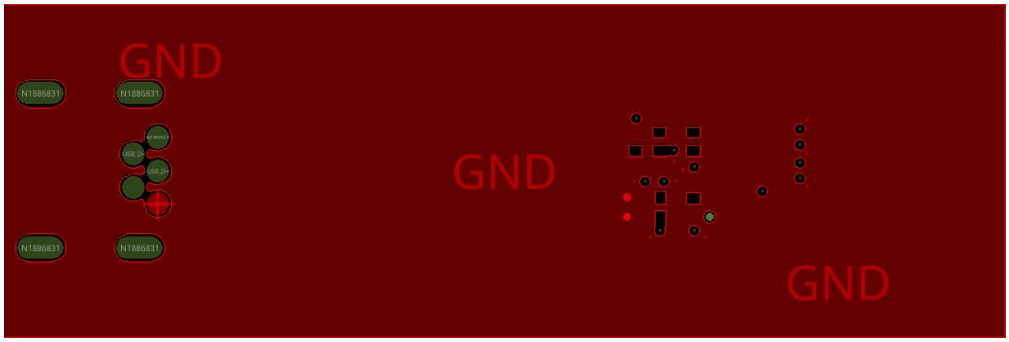
impedance of the signal trace, the signal reflow path will be affected, and the signal reflection will occur, affecting the signal quality and signal integrity.

PCB Reference Design

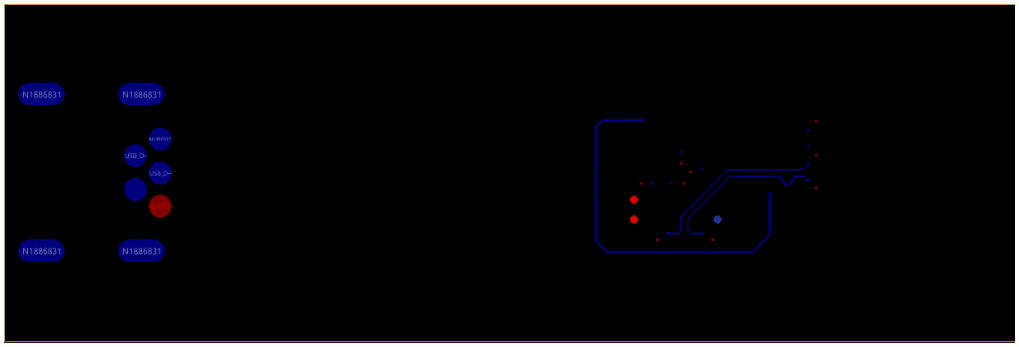
The TOP layer is the signal layer and the reference design is shown in the following figure.



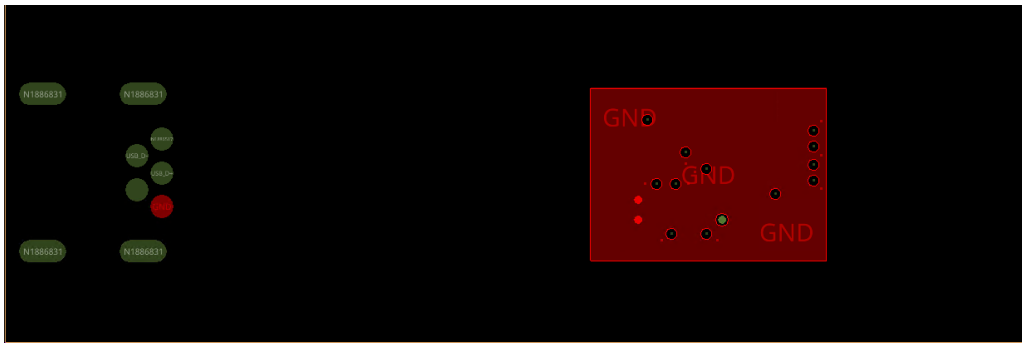
The LY2 layer is the GND layer, and the reference design is shown in the following figure.



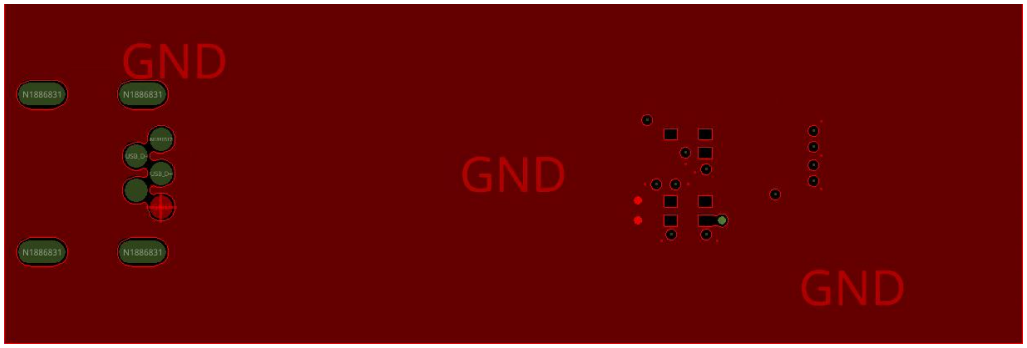
The LY3 layer is the signal layer, and the reference design is shown in the following figure.



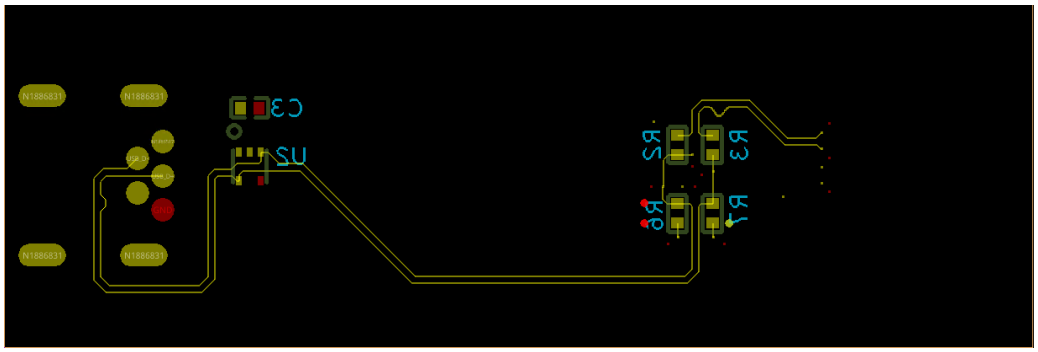
The LY4 layer is the GND and power layer, and the reference design is shown in the following figure.



The LY5 layer is the GND layer, and the reference design is shown in the following figure.



The BOTTOM layer is the signal layer, and the reference design is shown in the following figure.



Considerations

When selecting Gowin FPGA devices, if the LittleBee or Arora family devices are selected, the speed level of the LittleBee or Arora family devices is not less than C7.

Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

Revision History

Date	Version	Description
10/14/2022	1.0E	Initial version published.
04/11/2024	1.0.1E	The resistance value for GW5A-25 devices updated.
02/07/2025	1.1E	The content of each chapter updated.

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