



Gowin BCH Encoder IP

Release Note

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Revision History

Date	Version	Description
08/26/2022	1.0E	Initial version published.

Contents

Contents	i
1 About This Guide	1
2 Overview	2
3 Documentation	3
4 IP Support	4

1 About This Guide

This release includes Gowin BCH Encoder IP reference design and user guide.

Gowin BCH Encoder IP and reference design are available at Gowin Website. Take specific parameters as an example for the reference design, which can be used for testing after simulation, synthesis, placement and routing.

2 Overview

Gowin BCH Encoder IP is an encoder based on Bose-Chaudhuri-Hocquenghem code, and this IP can encode the input message using primitive polynomials. Gowin BCH Encode IP can be used for error checking and correction. Multiple configurations make it flexible and easy to use.

Table 1 Gowin BCH Encoder IP Overview

Gowin BCH Encoder IP	
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.8.07 and above)

3 Documentation

The software release file contains Gowin BCH Encoder IP manuals, which are listed below:

Document	Description
IPUG1010 , Gowin BCH Encoder IP User Guide	PDF
RN1010, Gowin BCH Encoder IP Release Note	PDF

4 IP Support

Since the requirements of user design and the maximum frequency are different, the reference design does not include FPGA specific location (.cst) and timing constraints (.sdc) documents, and you can determine the location and timing constraints on your own.

For the customized IP design and support, please contact Gowin sales and support line.

Website: www.gowinsemi.com

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