



Gowin BCH Encoder IP

User Guide

IPUG1010-1.0E, 08/26/2022

Copyright © 2022 Guangdong Gowin Semiconductor Corporation. All Rights Reserved.

GOWIN is a trademark of Guangdong Gowin Semiconductor Corporation and is registered in China, the U.S. Patent and Trademark Office, and other countries. All other words and logos identified as trademarks or service marks are the property of their respective holders. No part of this document may be reproduced or transmitted in any form or by any denotes, electronic, mechanical, photocopying, recording or otherwise, without the prior written consent of GOWINSEMI.

Disclaimer

GOWINSEMI assumes no liability and provides no warranty (either expressed or implied) and is not responsible for any damage incurred to your hardware, software, data, or property resulting from usage of the materials or intellectual property except as outlined in the GOWINSEMI Terms and Conditions of Sale. GOWINSEMI may make changes to this document at any time without prior notice. Anyone relying on this documentation should contact GOWINSEMI for the current documentation and errata.

Revision History

Date	Version	Description
08/26/2022	1.0E	Initial version published.

Contents

Contents	i
List of Figures	ii
List of Tables	iii
1 About This Guide	1
1.1 Purpose	1
1.2 Related Documents	1
1.3 Terminology and Abbreviations	1
1.4 Support and Feedback	2
2 Overview	3
2.1 Introduction to Gowin BCH Encoder IP	3
2.2 Features	4
2.3 Max. Frequency	4
2.4 Latency	4
2.5 Resource Utilization	4
3 Functional Description	5
3.1 System Block Diagram	5
3.2 Algorithm Introduction	5
4 Port Description	7
5 Timing Description	9
6 Call and Configure IP	10
7 Reference Design	12
8 File Delivery	13
8.1 Documentation	13
8.2 Reference Design	13

List of Figures

Figure 3-1 System Block Diagram	5
Figure 3-2 BCH Encoder Implementation Diagram	6
Figure 4-1 I/O Port Diagram.....	7
Figure 5-1 Timing Diagram	9
Figure 6-1 Open GUI Via Icon	10
Figure 6-2 Configuration Interface	11

List of Tables

Table 1-1 Terminology and Abbreviations	2
Table 2-1 Gowin BCH Encoder IP	3
Table 2-2 Resource Utilization (GW2A-18 C8/I7)	4
Table 4-1 I/O List of Gowin BCH Encoder IP	7
Table 6-1 Configuration Options	11
Table 8-1 Documentation List	13
Table 8-2 Ref. Design File List	13

1 About This Guide

1.1 Purpose

The purpose of Gowin BCH Encoder IP User Guide is to help you learn the features and usage of Gowin BCH Encoder IP by providing the descriptions of functions, ports, timing, GUI, and reference design.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS821, GW1NS series of FPGA Products Data Sheet](#)
- [DS861, GW1NSR series of FPGA Products Data Sheet](#)
- [DS871, GW1NSE series of SecureFPGA Products Data Sheet](#)
- [DS881, GW1NSER series of SecureFPGA Products Data Sheet](#)
- [DS891, GW1NRF series of Bluetooth FPGA Products Data Sheet](#)
- [DS841, GW1NZ series of FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS961, GW2ANR series of FPGA Products Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)
- [DS971, GW2AN-9X & 18X Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
IP	Intellectual Property
DSP	Digital Signal Processing
SRAM	Static Random Access Memory
BSRAM	Block Static Random Access Memory
ECC	Error Checking and Correction
BCH Code	Bose-Chaudhuri-Hocquenghem Code

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Introduction to Gowin BCH Encoder IP

Gowin BCH Encoder IP is an encoder based on Bose-Chaudhuri-Hocquenghem code, and this IP can encode the input message using primitive polynomials. Gowin BCH Encode IP can be used for error checking and correction.

Table 2-1 Gowin BCH Encoder IP

Gowin BCH Encoder IP	
IP Core Application	
Supported Devices	● GW1N series ● GW1NR series ● GW1NS series ● GW1NSR series ● GW1NSE series ● GW1NSER series ● GW1NRF series ● GW1NZ series ● GW2A series ● GW2AR series ● GW2ANR series ● GW2AN series
Logic Resource	Please refer to Table 2-2.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	

Gowin BCH Encoder IP	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.8.07 and above)

2.2 Features

- Can configure I/O data bit width
- Can configure Galois field
- Can configure message bit width

2.3 Max. Frequency

The maximum frequency of Gowin BCH Encoder IP is mainly determined by the speed grade of the devices and configuration parameters. For example, when GW2A-18 series of devices are used, the system clock can reach a maximum frequency of 200MHz.

2.4 Latency

The latency of Gowin BCH Encoder IP usually depends on the codeword length and message length.

2.5 Resource Utilization

Gowin BCH Encoder IP resource utilization mainly depends on the configuration of codeword length and message length. The resource utilization may be different with different devices. Take GW2A-18 series of products as an example, Gowin BCH Encoder IP resource utilization is as shown in Table 2-2.

Table 2-2 Resource Utilization (GW2A-18 C8/I7)

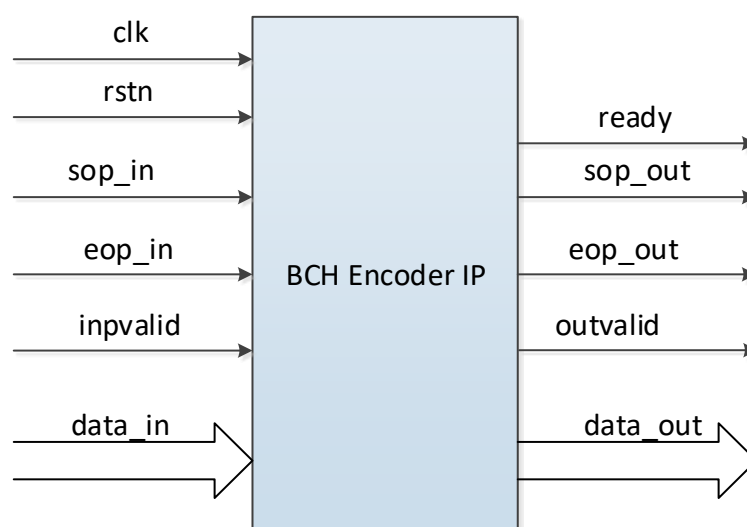
Device	Speed Grade	Codeword Length	Message Length	Name	Resource Utilization	Note
GW2A-18	C8/I7	15	7	LOGICS	63	-
				REGS	154	
				CLS	100	
				BSRAMS	0	

3 Functional Description

3.1 System Block Diagram

In Gowin BCH Encoder IP, the output is from the selected coefficient matrix and offset operation, and the block diagram is as shown Figure 3-1.

Figure 3-1 System Block Diagram



3.2 Algorithm Introduction

BCH code is an ECC algorithm proposed by Bose, Chaudhuri and Hocquenghem in 1959 for correcting multi-bit random errors. BCH has been widely used in the consumer electronics market, especially in the field of removable mass storage, such as USB flash disk, solid state disk due to its high error correction capability, high efficiency, low resource, and ease of use.

BCH code is a cyclic code capable of correcting multiple random errors, and BCH code can be described by the roots of generator polynomial $g(x)$. Given any finite field $GF(q)$ and its expansion $GF(q^m)$,

where q is a prime number or power of a prime number and m is a positive integer. When the symbol is taken from a cyclic code on $GF(q)$ and the roots set R of its generator polynomial $g(x)$ contains the following $\delta-1$ consecutive roots.

$$R \supseteq \{\alpha^{m0}, \alpha^{m0+1}, \dots, \alpha^{m0+\delta-2}\}$$

In this case, the cyclic code generated by $g(x)$ is called q -system BCH code. This IP is binary BCH code.

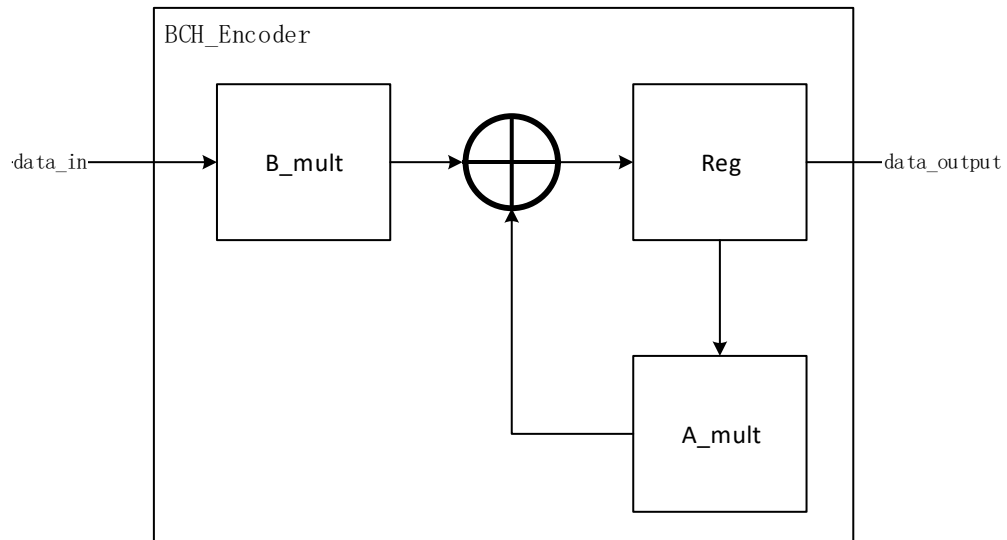
In the process of constructing BCH code, there are two decisive parameters constituting $g(x)$, that is, M and $t_{\max}$. M represents that the Galois field where the generator polynomial is located is $GF(2^M)$, and it also represents the encoded code length $N=2^M-1$; $t_{\max}$ represents that the BCH encoder can find and correct t errors at most, and it also shows that $g(x)$ is a minimum number polynomial based on the elements in $GF(2^M)$ as roots. $\alpha, \alpha^2, \dots, \alpha^{2t_{\max}}$

The process of BCH encoding can be regarded as the polynomial code $m(x)$ in the Galois field taking the remainder of the generator polynomial $g(x)$, and the remainder is the checking digit polynomial.

Therefore, for any positive integer M and T ($M \geq 3$, $T < 2^{M-1}$), there is a BCH code with symbol from $GF(2^M)$ and error correction capability t , and its code length is $N=2^M-1$; the message length is $K=N-2T$.

The following is the BCH Encoder implementation diagram.

Figure 3-2 BCH Encoder Implementation Diagram



4 Port Description

The I/O ports of Gowin BCH encoder IP is as shown in Figure 4-1; for the details, you can see Table 4-1.

Figure 4-1 I/O Port Diagram

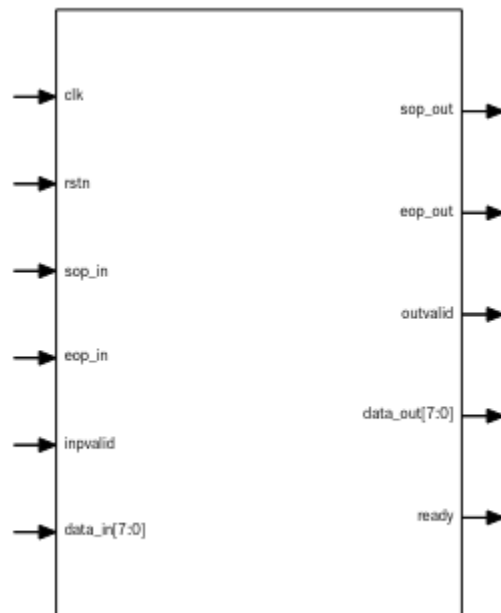


Table 4-1 I/O List of Gowin BCH Encoder IP

Signal	I/O	Data Width	Description
clk	I	1	Input clock signal
rstn	I	1	Reset signal, active-low.
sop_in	I	1	Start signal for input data
eop_in	I	1	End signal for input data
invalid	I	1	Input data valid signal
data_din	I	Optional	Input data signal
sop_out	O	1	Start signal for output data
eop_out	O	1	End signal for output data
outvalid	O	1	Output valid signal, active-high.

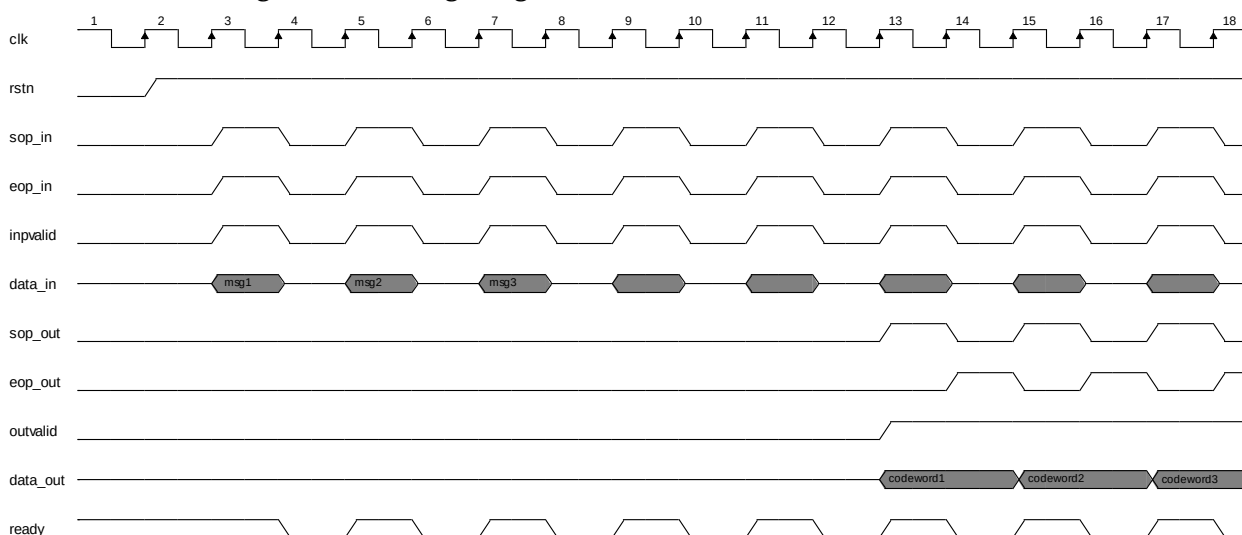
Signal	I/O	Data Width	Description
data_out	O	Optional	Output data signal
ready	O	Optional	Ready signal

5 Timing Description

This chapter mainly introduces the timing of Gowin BCH Encoder IP.

In the default configuration, the input valid data cycle is 1, and the output valid data cycle is 2. After Gowin BCH Encoder IP operation, the data will be output with a delay of 10 clock cycles. For IP timing, see Figure 5-1.

Figure 5-1 Timing Diagram

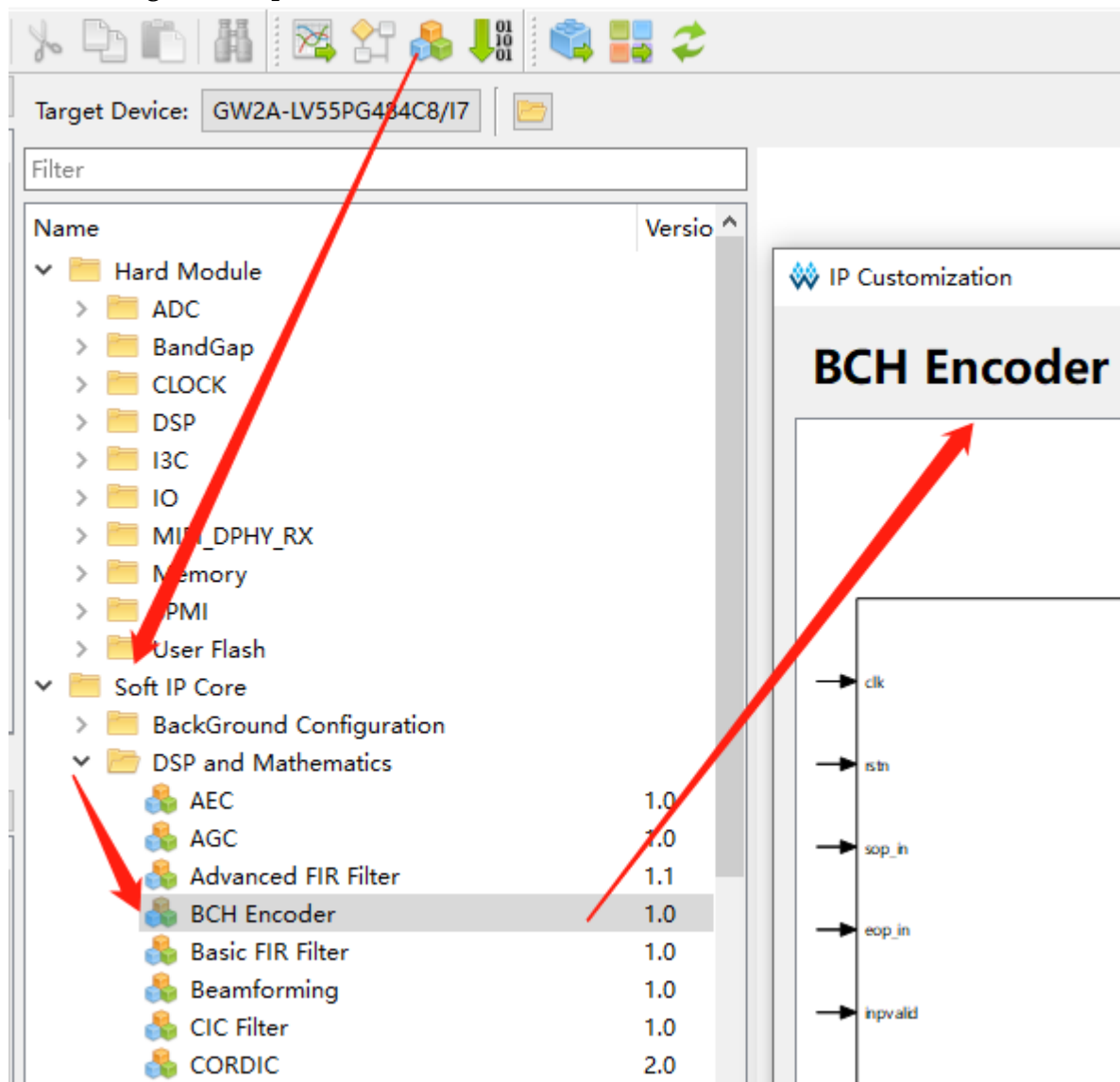


As shown in the figure, when the data is input to the IP, the sop_in signal needs to be pulled high in the first cycle of the input, the eop_in signal needs to be pulled high in the last cycle; and in the remaining time, keep low. The ininvalid signal needs to be continuously pulled high during the cycle when the data is valid. The ready signal is high by default, and will be pulled low after the eop_in signal becomes high, and will not be pulled high again until the next set of data can be input. When the IP outputs data, the sop_out signal will be pulled high in the first cycle of the output, and the eop_in signal will be pulled high in the last cycle; in the remaining time, keep low. The outvalid signal will be continuously pulled high during the cycle when the data is valid.

6 Call and Configure IP

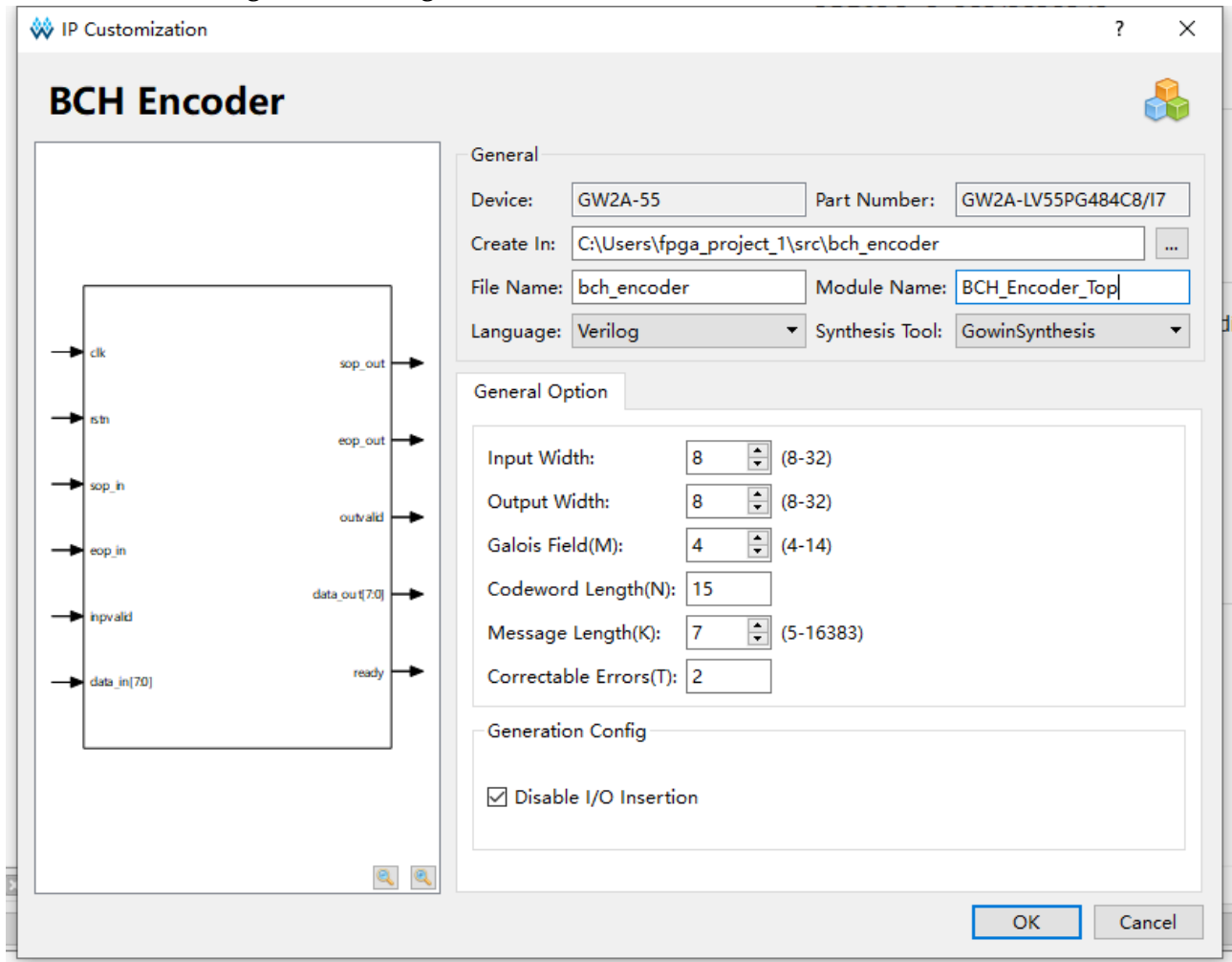
Click "Tools > IP Core Generator > DSP and Mathematics > BCH Encoder" to call and configure Gowin BCH Encoder IP. Toolbar icon is also available as shown in Figure 6-1.

Figure 6-1 Open GUI Via Icon



Gowin BCH Encoder IP configuration interface is shown in Figure 6-2.

Figure 6-2 Configuration Interface



- You can configure the generated file name by modifying the File Name.
- You can configure the module name by modifying the Module Name.
- You can configure IP working mode and other options by Options.

Gowin BCH Encoder IP configuration options are shown in Table 6-1.

Table 6-1 Configuration Options

Option	Description
Input Width	Input data width, 8-32 bits.
Output Width	Output data width, 8-32 bits.
Galois Field	Galois Field range, 4-14.
Codeword Length	Codeword length, determined by Galois field.
Message Length	Message length, maximum configurable range determined by Galois field.
Correctable Errors	The maximum number of correctable errors, determined by both Galois field and message length.

7 Reference Design

Please refer to the related test cases in [RefDesign](#).

8 File Delivery

The delivery file of Gowin BCH Encoder IP includes documentation and reference design.

8.1 Documentation

The documents folder mainly contains the user guide and release note in PDF.

Table 8-1 Documentation List

Name	Description
IPUG1010, Gowin BCH Encoder IP User Guide	Gowin IP User Guide, namely this one.
RN1010 , Gowin BCH Encoder IP Release Note	Gowin IP Release Note

8.2 Reference Design

The Ref. Design folder contains the netlist file, the user reference design, the constraints file, the top file, and the project folder, etc.

Table 8-2 Ref. Design File List

Name	Description
bch_encoder_exp.v	Top module and stimulus generation module of reference design
bch_encoder.vo	BCH Encoder netlist file
demo.cst	BCH Encoder physical constraints file
fpga_project.gao	Capture output data of BCH Encoder
bch_encoder	Gowin BCH Encoder IP project file

