



Gowin LPC Peripheral IP

Release Note

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Revision History

Date	Version	Description
2022/07/28	1.0	Initial version published.

Contents

Contents.....	i
1 About This Guide.....	1
2 Overview.....	2
3 Documents	3
4 IP Support	4

1 About This Guide

This release includes Gowin LPC Peripheral IP reference design and user guide.

Gowin LPC Peripheral IP user guide and reference design can be downloaded from Gowin website, and the reference design has been configured with specific parameters that can be used for simulation, synthesis, placement and routing after adding user design.

2 Overview

Gowin LPC Peripheral IP is a general-purpose LPC peripheral interface that complies with LPC standard protocol, and this IP can implement I/O read and I/O write functions of the LPC protocol.

Table -1 Gowin LPC Peripheral IP Overview

Gowin LPC Peripheral IP	
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	–
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.8.07 and above)

3 Documents

The software release file contains Gowin LPC Peripheral IP documents, which are listed below.

Table 2 Gowin LPC Peripheral IP Documents

Documents	Description
IPUG799, Gowin LPC Peripheral IP User Guide.pdf	PDF
RN799, Gowin LPC Peripheral IP Release Note.pdf	PDF

4 IP Support

Since the requirements of user design and the maximum frequency are different, the reference design does not include FPGA specific location (.cst) and timing constraints (.sdc) documents, and you can determine the location and timing constraints on your own.

For the customized IP design and support, please contact Gowin sales and support line.

Website: www.gowinsemi.com

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