DK_Motor_GW2A-LV55PG484C8I7_V3.0

User Guide

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Revision History

Date	Version	Description
06/28/2022	1.0E	Initial version published.
03/17/2023	1.0.1E	● Chapter 4 “Quick Start” removed. ● “Figure 2-4 System Block Diagram” in Chapter 2 “Development Board Introduction” updated. ● “Table 3-3 Ethernet Interface Pinout” in Chapter 3.5.2 "Pinout” updated.

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1 About This Guide

1.1 Purpose

The DK_Motor_GW2A-LV55PG484C8I7_V3.0 development board (hereinafter referred to development board) user guide consists of following three parts:

- A brief introduction to the features of the development board;
- An introduction to the development board system architecture and hardware resources;
- An introduction to the functions, circuits, and pinouts of each module;

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com/en:

- DS102, GW2A series of FPGA Products Data Sheet
- UG113, GW2A-55 Pinout
- UG111, GW2A series of FPGA Products Package and Pinout User Guide
- UG290, GW1N series of FPGA Products Programming and Configuration User Guide
- SUG100, Gowin Software User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Abbreviations and Terminology

Terminology and Abbreviations	Meaning
BSRAM	Block Static Random Access Memory
DDR	Double Data Rate
DSP	Digital Signal Processing
FLASH	Flash Memory
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable Input/Output
LDO	Low Dropout Regulator
LUT4	Four-input Look-up Table
LVDS	Low-voltage Differential Signaling
SSRAM	Shadow Static Random Access Memory

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

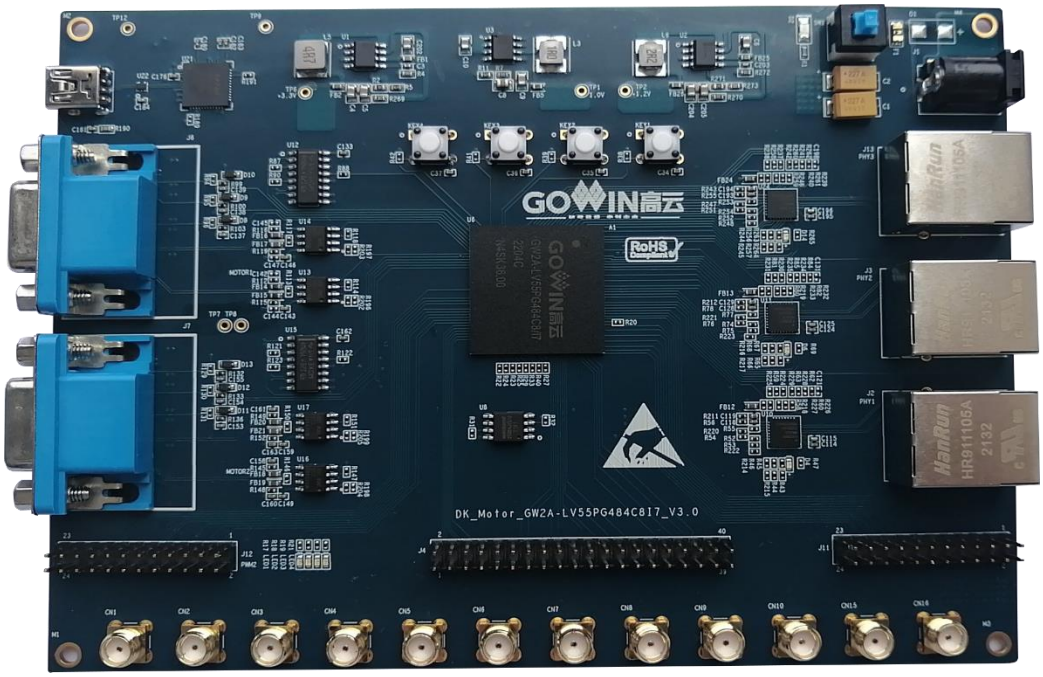
Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Development Board Introduction

2.1 Overview

Figure 2-1 DK_Motor_GW2A-LV55PG484C8I7_V3.0 Development Board



The development board uses the GW2A- LV55PG484 FPGA device, which is the first generation product of Gowin Arora family. The GW2A series of FPGA products offer abundant resources like high-performance DSP, high-speed LVDS interface and BSRAM. These embedded resources combine a streamlined FPGA architecture with a 55nm process to make the GW2A series of FPGA products ideal for high-speed and low-cost applications.

The development board integrates three Ethernet interfaces, supporting 10M/100M industrial Ethernet communication; It also provides abundant external interfaces, including ELVDS, PWM, PSMC, Ethernet,

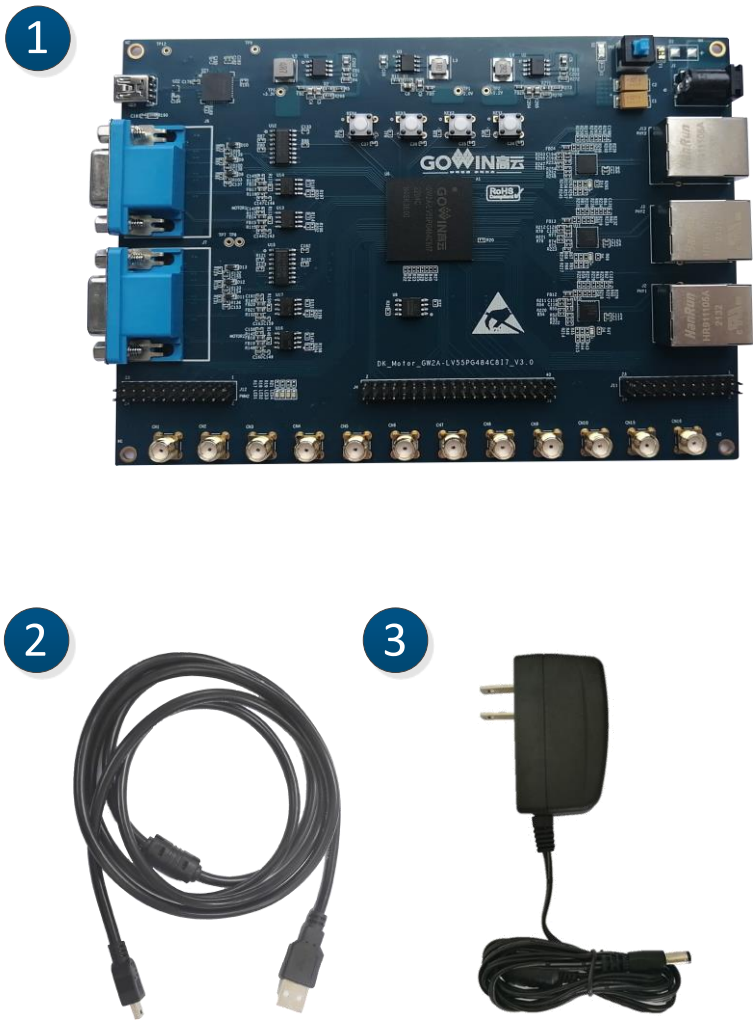
motor communication, and GPIO interface. External FLASH chip is used to store FPGA configuration programs; There are keys and LEDs that you can use to debug.

2.2 A Development Board Kit

The development board kit includes the following items:

1. DK_Motor_GW2A-LV55PG484C8I7_V3.0 development board
2. 5V power (Input: 100-240V~50/60Hz 0.5A, output: DC 5V 2A)
3. USB Mini B Cable

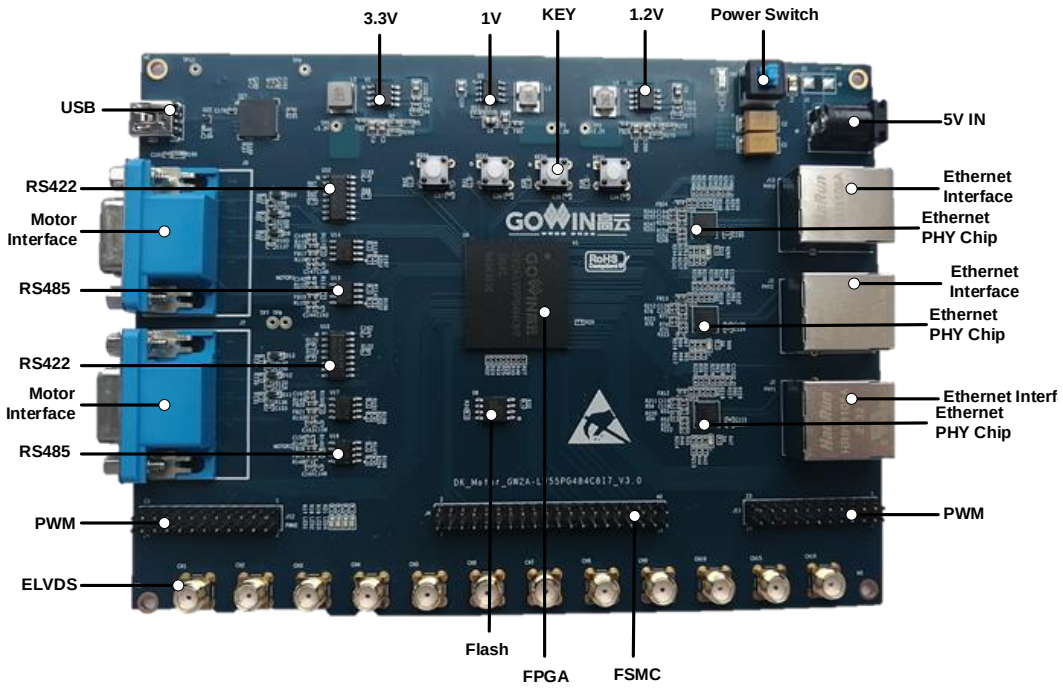
Figure 2-2 A Development Board Suite



① DK_Motor_GW2A-LV55PG484C8I7_V3.0 development board
② 5V power (Input: 100-240V~50/60Hz 0.5A, output: DC 5V 2A)
③ USB Mini B data cable

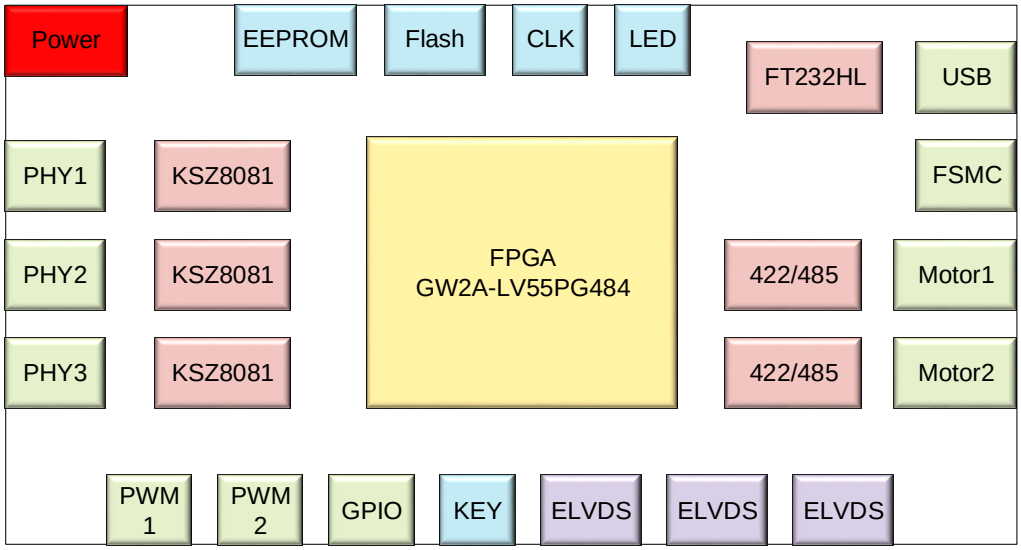
2.3 PCB Components

Figure 2-3 PCB Components



2.4 System Block Diagram

Figure 2-4 System Block Diagram



2.5 Features

The key features are as follows:

1. The FPGA device
   - Gowin GW2A-LV55PG484 FPGA
   - 319 Max. user I/O
2. Download and Boot
   - Integrate download module on the board, download through Mini B cable
   - External Flash boot
3. Power
   - External DC 5V 2A
   - The green POWER light is on after power on
   - The development board can generate 3.3V, 1.2V, 1.0V
4. Clock system
   - 25MHz crystal oscillator input
5. Memory Device
   - 32Kbit EEPROM
   - 64Mbit FLASH
6. Ethernet interface
   - Three Ethernet interfaces
   - Adopt KSZ8081MNXCA-TR chip and supports MII interface
   - RJ45 connector with built-in transformer
7. ELVDS interface
   - Three ELVDS interfaces, including six pairs of differential signals
8. FSMC interface
   - One FSMC interface for the communication between FPGA and MCU
9. PWM interface
   - Two PWM interfaces for transmitting PWM signal
10. Motor control interface
    - Two motor control interfaces
    - Each motor interface is connected to one RS422 transceiver and two RS485 transceiver chips
11. USB interface
    - For downloading test program
12. GPIO Interface
    - There are 40 PIN double-row pins, including 36 GPIOs. I/O Bank voltage is 3.3V, leading to two 3.3V voltage and two ground pins.

- Two 24 PIN double-row pins, each including 19 GPIOs. I/O Bank voltage is 3.3V, leading to three ground pins.

13. Debug module
    - Four keys
    - Four green LEDs

3 Development Board Circuit

3.1 FPGA Module

Overview

For the resources of GW2A-LV55PG484 FPGA products, please refer to *DS102, GW2A Series of FPGA Products*.

I/O BANK Introduction

For the I/O BANK, package, and pinout information, see *UG111, GW2A Series of FPGA Products Package and Pinout User Guide* for more details.

3.2 Download Module

3.2.1 Introduction

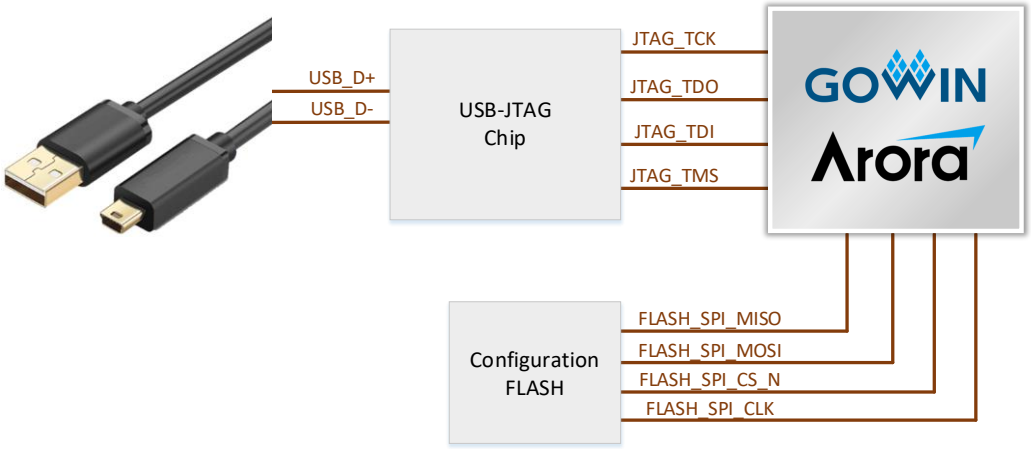
The development board provides a USB downloading interface realized by channel A of FT232HL USB conversion chip. You can set the MODE value to download the programs to the on-chip SRAM or external Flash. When downloaded to SRAM, the bitstream file will be lost if the device powers down. When downloaded to Flash, the bitstream file will not be lost if the device powers down.

The MODE value configuration is as follows:

1. In any mode, you can download the bitstream file to the on-chip SRAM and run it immediately.
2. Set MODE as "011" to download the bitstream file to the external Flash. Set MODE to "000" and power on again. The device will read the FPGA configuration data from the Flash automatically.

The connection diagram of download and configuration is as shown in Figure 3-1：

Figure 3-1 FPGA Download and Configuration Connection Diagram



3.2.2 Pinout

Table 3-1 FPGA Download and Configuration Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
JTAG_TCK	N20	2	3.3V	JTAG Signal
JTAG_TDO	M22	2	3.3V	JTAG Signal
JTAG_TDI	M20	2	3.3V	JTAG Signal
JTAG_TMS	N22	2	3.3V	JTAG Signal
FLASH_SPI_MISO	P19	3	3.3V	Configure FLASH Signal
FLASH_SPI_MOSI	P20	3	3.3V	Configure FLASH Signal
FLASH_SPI_CS_N	N18	3	3.3V	Configure FLASH Signal
FLASH_SPI_CLK	P18	3	3.3V	Configure FLASH Signal

3.3 Power Supply

3.3.1 Introduction

The development board is powered via a power adapter. The input parameter is 100-240V~50/60MHz 0.5A, and the output is DC +5V 2A.

The input 5V power can generate 3.3V, 1.2V, and 1.0V via the power supply chip on the development board.

Adopt two NCP3170ADR2G DC-DC power chips to generate 3.3V and 1.2V, and the maximum output current is 3A.

Adopt one FP6165ADXR-G1 DC-DC power supply chip to generate 1.0V, and the maximum output current is 3A.

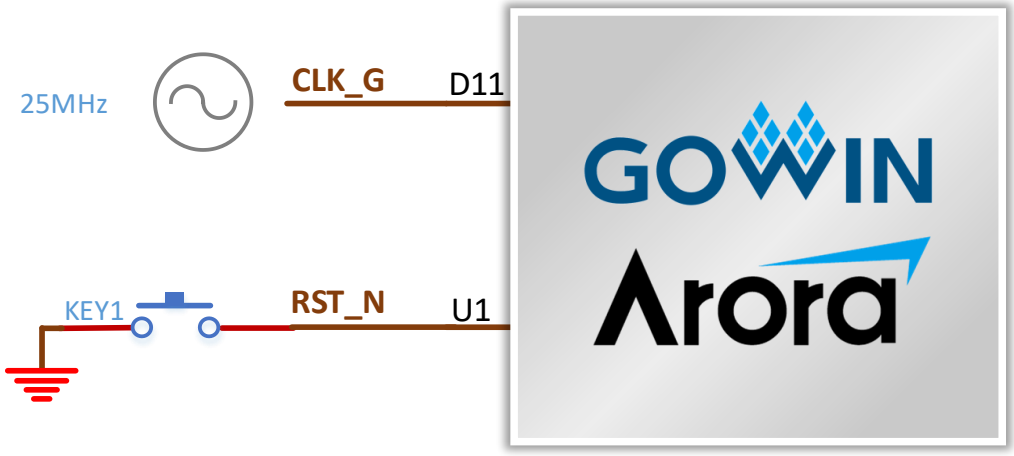
3.4 Clock and Reset

3.4.1 Introduction

The development board offers a 25MHz oscillator connecting to the global clock pins.

The reset circuit of the development board adopts the key reset design. Press the key to reset FPAG.

Figure 3-2 Clock and Reset Connection Diagram



3.4.2 Pinout

Table 3-2 Clock and Reset Pinout

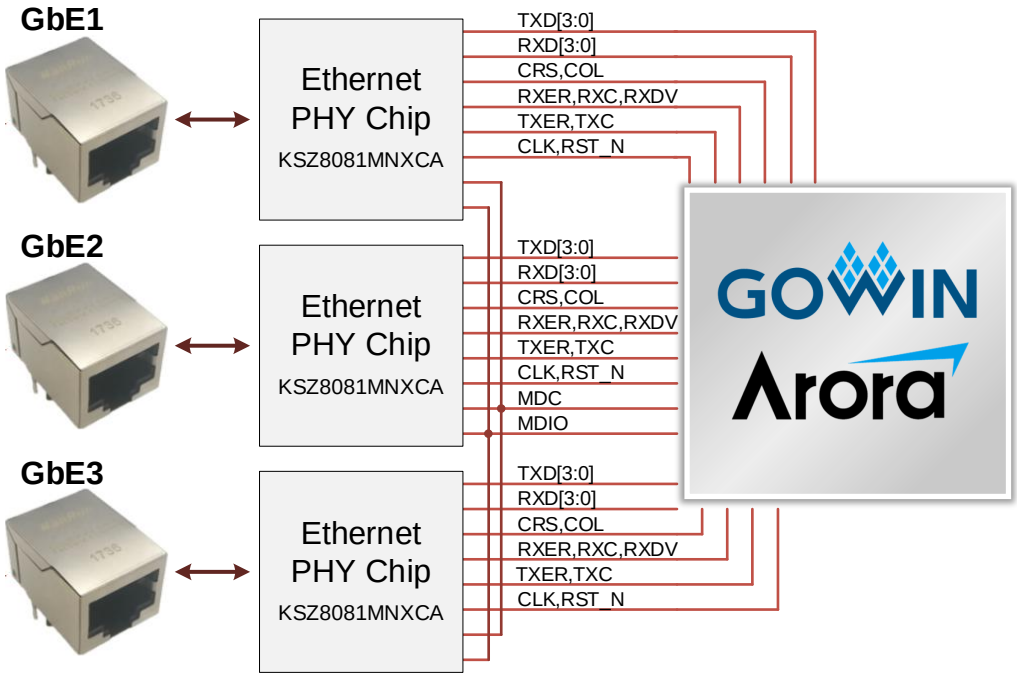
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
CLK_G	D11	1	3.3V	25MHz crystal oscillator Input
RST_N	U1	6	3.3V	Reset signal, active-high

3.5 Ethernet

3.5.1 Introduction

The development board is equipped with three KSZ8081MNXCA-TR chips, supporting MII interface.

Figure 3-3 FPGA and Ethernet Interface Connection Diagram



3.5.2 Pinout

Table 3-3 Ethernet Interface Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
PHY1_CRS	E16	1	3.3V	MII carrier sense
PHY1_COL	C15	1	3.3V	MII collision test
PHY1_TXD0	D12	1	3.3V	MII transmitting data
PHY1_TXD1	D10	0	3.3V	MII transmitting data
PHY1_TXD2	C11	1	3.3V	MII transmitting data
PHY1_TXD3	D14	1	3.3V	MII transmitting data
PHY1_TXEN	E12	1	3.3V	MII transmitting error
PHY1_TXC	D16	1	3.3V	MII transmitting clock
PHY1_RXER	E13	1	3.3V	MII receiving error
PHY1_RXC	A15	1	3.3V	MII receiving clock
PHY1_RXDV	B15	1	3.3V	MII receiving data, valid

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
PHY1_RXD0	A14	1	3.3V	MII receiving data
PHY1_RXD1	A13	1	3.3V	MII receiving data
PHY1_RXD2	C12	1	3.3V	MII receiving data
PHY1_RXD3	A12	0	3.3V	MII receiving data
PHY_MDC	C20	2	3.3V	MII clock input
PHY_MDIO	C8	0	3.3V	MII data input/output
PHY1_CLK	M4	6	3.3V	Clock input
PHY1_RST_n	F16	1	3.3V	Chip select
PHY2_CRS	A9	0	3.3V	MII collision test
PHY2_COL	A8	0	3.3V	MII carrier sense
PHY2_TXD0	D5	0	3.3V	MII transmitting data
PHY2_TXD1	B7	0	3.3V	MII transmitting data
PHY2_TXD2	A7	0	3.3V	MII transmitting data
PHY2_TXD3	B8	0	3.3V	MII transmitting data
PHY2_TXEN	D4	0	3.3V	MII transmitting error
PHY2_TXC	A6	0	3.3V	MII transmitting clock
PHY2_RXER	B6	0	3.3V	MII receiving error
PHY2_RXC	A5	0	3.3V	MII receiving clock
PHY2_RXDV	C4	0	3.3V	MII receiving data, valid
PHY2_RXD0	A4	0	3.3V	MII receiving data
PHY2_RXD1	A3	0	3.3V	MII receiving data
PHY2_RXD2	A2	0	3.3V	MII receiving data
PHY2_RXD3	A1	0	3.3V	MII receiving data
PHY2_CLK	B11	0	3.3V	Clock input
PHY2_RST_n	A11	0	3.3V	Chip select
PHY3_CRS	F2	7	3.3V	MII collision test
PHY3_COL	F1	7	3.3V	MII carrier sense
PHY3_TXD0	D3	7	3.3V	MII transmitting data
PHY3_TXD1	H2	7	3.3V	MII transmitting data
PHY3_TXD2	G1	7	3.3V	MII transmitting data
PHY3_TXD3	G2	7	3.3V	MII transmitting data
PHY3_TXEN	E4	7	3.3V	MII transmitting error
PHY3_TXC	H1	7	3.3V	MII transmitting clock
PHY3_RXER	J1	7	3.3V	MII receiving error
PHY3_RXC	K1	7	3.3V	MII receiving clock

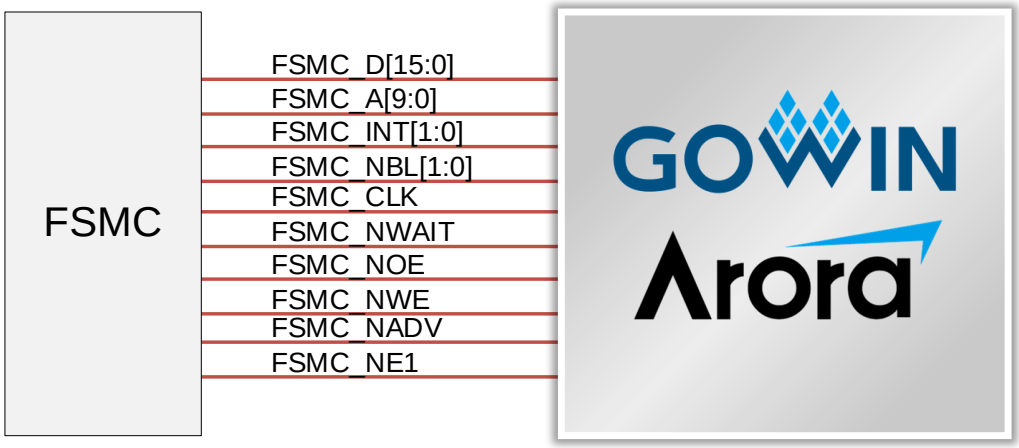
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
PHY3_RXDV	L2	7	3.3V	MII receiving data, valid
PHY2_RXD0	L1	7	3.3V	MII receiving data
PHY2_RXD1	M2	7	3.3V	MII receiving data
PHY2_RXD2	M1	7	3.3V	MII receiving data
PHY2_RXD3	P1	7	3.3V	MII receiving data
PHY2_CLK	R1	7	3.3V	Clock input
PHY2_RST_n	D1	7	3.3V	Chip selected

3.6 FSMC interface

3.6.1 Introduction

There is one FSMC interface on the development board for the communication between FPGA and MCU. These pins can be used as GPIOs. The connection diagram is as follows:

Figure 3-4 FPGA and FSMC Interface Connection Diagram



3.6.2 Pinout

Table 3-4 FSMC Interface Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
FSMC_D0	Y18	4	3.3V	Data
FSMC_D1	Y19	4	3.3V	Data
FSMC_D2	AB19	4	3.3V	Data
FSMC_D3	AA20	4	3.3V	Data
FSMC_D4	W19	4	3.3V	Data
FSMC_D5	L22	2	3.3V	Data

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
FSMC_D6	K18	2	3.3V	Data
FSMC_D7	J19	2	3.3V	Data
FSMC_D8	J22	2	3.3V	Data
FSMC_D9	H19	2	3.3V	Data
FSMC_D10	H22	2	3.3V	Data
FSMC_D11	H21	2	3.3V	Data
FSMC_D12	G18	2	3.3V	Data
FSMC_D13	G20	2	3.3V	Data
FSMC_D14	F19	2	3.3V	Data
FSMC_D15	F22	2	3.3V	Data
FSMC_A0	AB18	4	3.3V	Address
FSMC_A1	W18	4	3.3V	Address
FSMC_A2	AB20	4	3.3V	Address
FSMC_A3	Y20	4	3.3V	Address
FSMC_A4	L19	2	3.3V	Address
FSMC_A5	K19	2	3.3V	Address
FSMC_A6	K22	2	3.3V	Address
FSMC_A7	J18	2	3.3V	Address
FSMC_A8	F20	2	3.3V	Address
FSMC_A9	D22	2	3.3V	Address
FSMC_NWE	H20	2	3.3V	Write enable
FSMC_NOE	G19	2	3.3V	Read enable
FSMC_NWAIT	F18	2	3.3V	Wait
FSMC_INT0	F21	2	3.3V	Interrupt
FSMC_INT1	E22	2	3.3V	Interrupt
FSMC_NE1	J20	2	3.3V	Chip selected
FSMC_NADV	H18	2	3.3V	Multiplexing Mode
FSMC_NBL0	G21	2	3.3V	Select channel
FSMC_NBL1	G22	2	3.3V	Select channel
FSMC_CLK	AB12	4	3.3V	Clock

3.7 ELVDS interface

3.7.1 Introduction

ELVDS interface are 12 SMA sockets, including 6 pairs of differential signals. These interfaces are also used as GPIOs. The connection diagram is as follows:

Figure 3-5 ELVDS Interface Diagram

3.7.2 Pinout

Table 3-5 ELVDS Interface Pinout

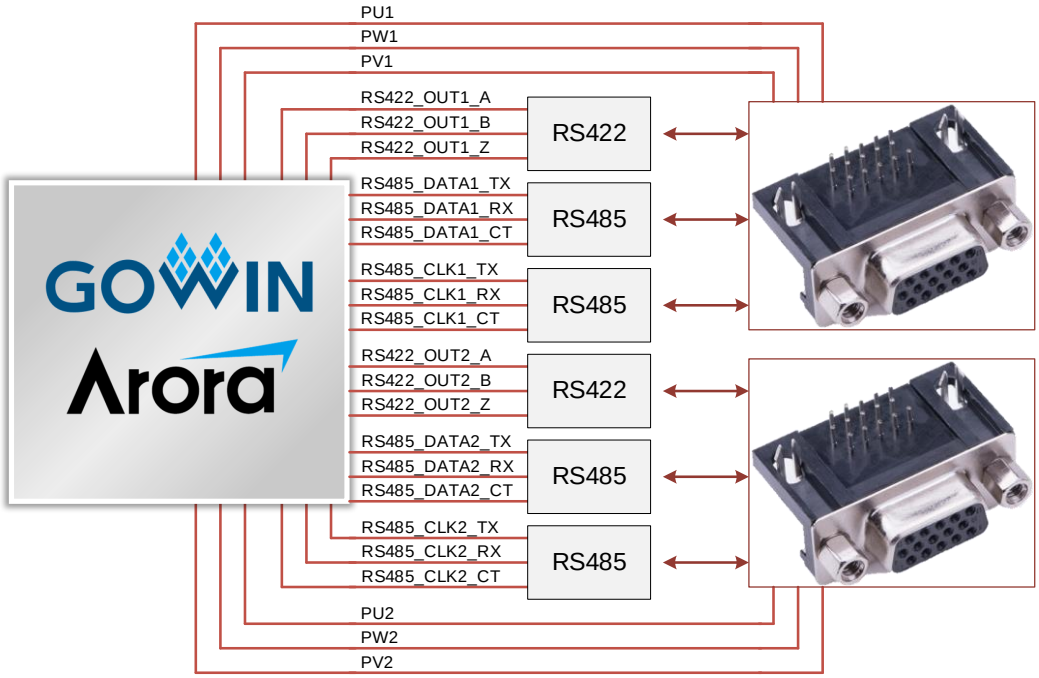
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
ELVDS_D0P	AB22	3	3.3V	Differential Channel 0+
ELVDS_D0N	AB21	3	3.3V	Differential Channel 0-
ELVDS_D1P	Y22	3	3.3V	Differential Channel 1+
ELVDS_D1N	AA22	3	3.3V	Differential Channel 1-
ELVDS_D2P	V22	3	3.3V	Differential Channel 2+
ELVDS_D2N	W22	3	3.3V	Differential Channel 2-
ELVDS_D3P	W20	3	3.3V	Differential Channel 3+
ELVDS_D3N	V20	3	3.3V	Differential Channel 3-
ELVDS_D4P	U19	3	3.3V	Differential Channel 4+
ELVDS_D4N	U18	3	3.3V	Differential Channel 4-
ELVDS_D5P	T17	3	3.3V	Differential Channel 5+
ELVDS_D5N	U17	3	3.3V	Differential Channel 5-

3.8 Motor Control Interface

3.8.1 Introduction

There are two motor control interfaces on the development board for the communication between FPGA and motor. The connection diagram is as follows:

Figure 3-6 Connection Diagram of Motor Control Interface



3.8.2 Pinout

Table 3-6 Motor Control Interface Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
PU1	AB3	5	3.3V	Incremental Encoder U Signal
PW1	AA3	5	3.3V	Incremental Encoder W Signal
PV1	AB4	5	3.3V	Incremental Encoder V Signal
RS422_OUT1_A	Y3	5	3.3V	Incremental Encoder Phase A Pulse Signal
RS422_OUT1_B	AB1	5	3.3V	Incremental Encoder Phase B Pulse Signal
RS422_OUT1_Z	AB2	5	3.3V	Incremental Encoder Phase Z Pulse Signal
RS485_DATA1_TX	AB5	5	3.3V	RS485 Transceiver Transmitting Signal

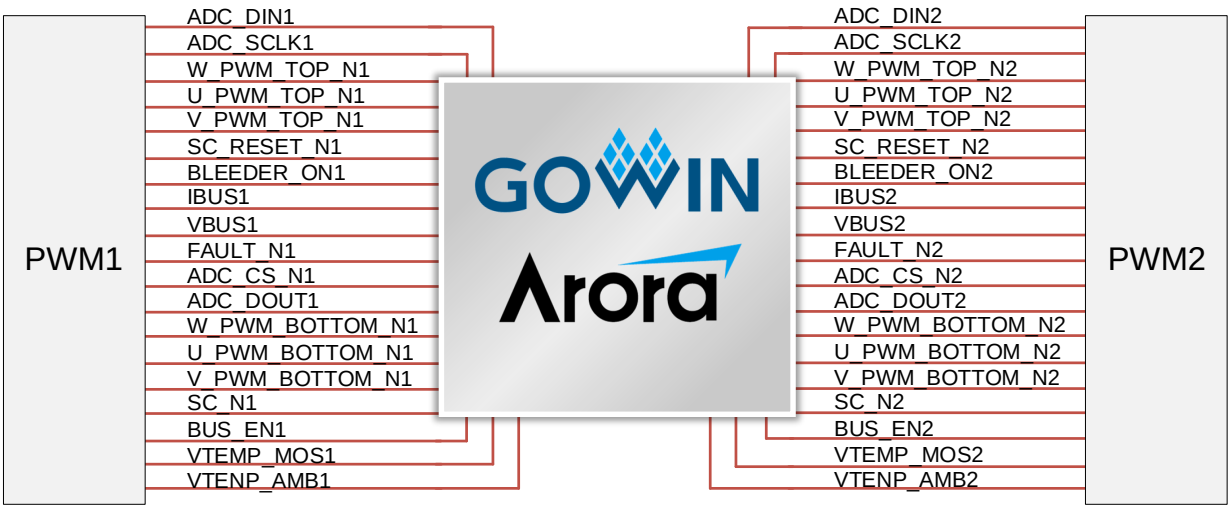
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
RS485_DATA1_RX	V6	5	3.3V	RS485 Transceiver Receiving Signal
RS485_DATA1_CT	U6	5	3.3V	RS485 Transceiver Signal Direction Control
RS485_CLK1_TX	Y4	5	3.3V	RS485 Transceiver Transmitting Signal
RS485_CLK1_RX	Y5	5	3.3V	RS485 Transceiver Receiving Signal
RS485_CLK1_CT	W5	5	3.3V	RS485 Transceiver Signal Direction Control
PU2	W6	5	3.3V	Incremental Encoder U Signal
PW2	AA7	5	3.3V	Incremental Encoder W Signal
PV2	AB7	5	3.3V	Incremental Encoder V Signal
RS422_OUT2_A	Y6	5	3.3V	Incremental Encoder Phase A Pulse Signal
RS422_OUT2_B	AA6	5	3.3V	Incremental Encoder Phase B Pulse Signal
RS422_OUT2_Z	AB6	5	3.3V	Incremental Encoder Phase Z Pulse Signal
RS485_DATA2_TX	U7	5	3.3V	RS485 Transceiver Transmitting Signal
RS485_DATA2_RX	W8	5	3.3V	RS485 Transceiver Receiving Signal
RS485_DATA2_CT	V8	5	3.3V	RS485 Transceiver Signal Direction Control
RS485_CLK2_TX	U7	5	3.3V	RS485 Transceiver Transmitting Signal
RS485_CLK2_RX	V7	5	3.3V	RS485 Transceiver Receiving Signal
RS485_CLK2_CT	W7	5	3.3V	RS485 Transceiver Signal Direction Control

3.9 PWM interface

3.9.1 Introduction

There are two PWM interfaces on the development board. These pins can also be used as GPIOs. The connection diagram is as follows:

Figure 3-7 PWM Interface Connection Diagram



3.9.2 Pinout

Table 3-7 PWM Interface Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
ADC_DIN1	A16	1	3.3V	ADC data input
ADC_SCLK1	AB10	5	3.3V	ADC clock signal
ADC_CS_N1	B17	1	3.3V	ADC enable signal
ADC_DOUT1	A17	1	3.3V	ADC data output
FAULT_N1	B16	1	3.3V	Reserved IO
W_PWM_TOP_N1	D17	1	3.3V	Phase W PWM upper leg control signal
U_PWM_TOP_N1	C18	1	3.3V	Phase U PWM upper leg control signal
V_PWM_TOP_N1	A19	1	3.3V	Phase V PWM upper leg control signal
W_PWM_BOTTOM_N1	C17	1	3.3V	Phase W PWM upper leg control signal
U_PWM_BOTTOM_N1	A18	1	3.3V	Phase U PWM upper leg control signal

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
V_PWM_BOTTOM_N1	D18	1	3.3V	Phase V PWM upper leg control signal
SC_RESET_N1	D19	2	3.3V	Reserved IO
SC_N1	C19	1	3.3V	Reserved IO
BLEEDER_ON1	D20	2	3.3V	Reserved IO
BUS_EN1	A20	1	3.3V	Reserved IO
IBUS1	A22	1	3.3V	Reserved IO
VBUS1	C22	2	3.3V	Reserved IO
VTEMP_MOS1	A21	1	3.3V	Reserved IO
VTEMP_AMB1	B22	1	3.3V	Reserved IO
ADC_DIN2	AA16	4	3.3V	ADC data input
ADC_SCLK2	AB16	4	3.3V	ADC clock signal
ADC_CS_N2	V17	4	3.3V	ADC enable signal
ADC_DOUT2	AA15	4	3.3V	ADC data output
FAULT_N2	U16	4	3.3V	Reserved IO
W_PWM_TOP_N2	V16	4	3.3V	Phase W PWM upper leg control signal
U_PWM_TOP_N2	W16	4	3.3V	Phase U PWM upper leg control signal
V_PWM_TOP_N2	AB14	4	3.3V	Phase V PWM upper leg control signal
W_PWM_BOTTOM_N2	Y16	4	3.3V	Phase W PWM upper leg control signal
U_PWM_BOTTOM_N2	W17	4	3.3V	Phase U PWM upper leg control signal
V_PWM_BOTTOM_N2	AB15	4	3.3V	Phase V PWM upper leg control signal
SC_RESET_N2	W15	4	3.3V	Reserved IO
SC_N2	Y15	4	3.3V	Reserved IO
BLEEDER_ON2	W14	4	3.3V	Reserved IO
BUS_EN2	V15	4	3.3V	Reserved IO
IBUS2	AB13	4	3.3V	Reserved IO
VBUS2	AA12	4	3.3V	Reserved IO
VTEMP_MOS2	V14	4	3.3V	Reserved IO
VTEMP_AMB2	Y14	4	3.3V	Reserved IO

3.10 GPIO

3.10.1 Introduction

There are one 40 PIN double-row pin and two 24 PIN double-row pins. These pins are used as IOs to facilitate user testing. Among them:

There are 40 PIN double-row pins, including 36 GPIOs. I/O Bank voltage is 3.3V, leading to two 3.3V voltage and two ground pins.

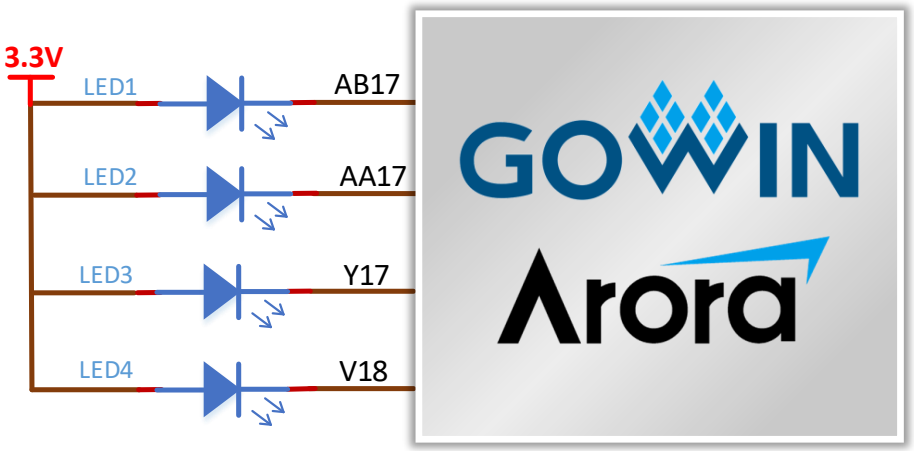
Two 24 PIN double-row pins, each including 19 GPIOs. I/O Bank voltage is 3.3V, leading to three ground pins.

3.11 LED Module

3.11.1 Introduction

Four green LEDs are integrated into the development board and are used to display the required status. When the output signal of FPGA corresponding pin is low, the LED is lit up. When the output signal is high, the LED is off. The connection diagram is shown in Figure 3-8.

Figure 3-8 LED Connection Diagram



3.11.2 Pinout

Table 3-8 LED Pinout

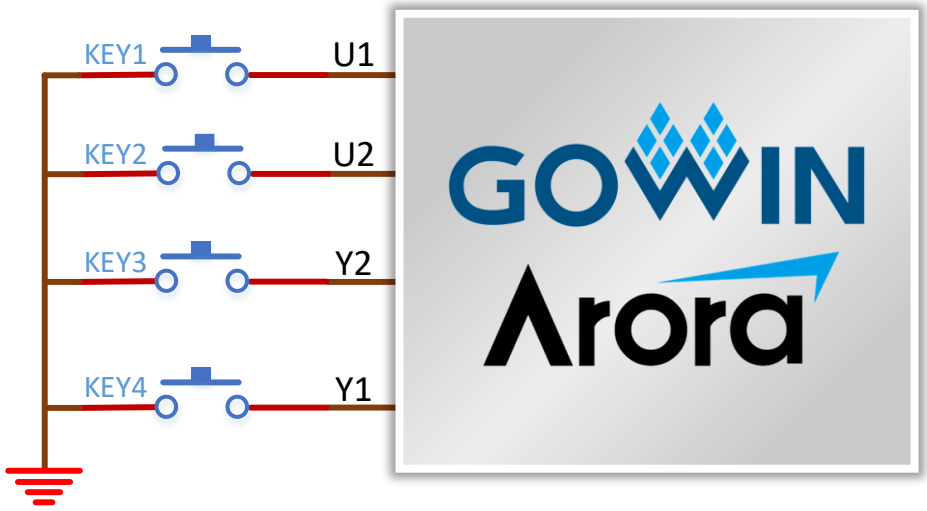
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
LED1	AB17	4	3.3V	LED1
LED2	AA17	4	3.3V	LED2
LED3	Y17	4	3.3V	LED3
LED4	V18	4	3.3V	LED4

3.12 Key Module

3.12.1 Introduction

The development board has four keys that can be used to control input during testing. When the key is pressed, the input is low. The connection diagram is shown in Figure 3-9.

Figure 3-9 Key Circuit



3.12.2 Pinout

Table 3-9 Key Module Pinout

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
KEY1	U1	6	3.3V	KEY1
KEY2	U2	6	3.3V	KEY2
KEY3	Y2	6	3.3V	KEY3
KEY4	Y1	6	3.3V	KEY4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