



Gowin I3C Dual Clock IP

Release Note

RN787-1.0E,10/28/2021

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Revision History

Date	Version	Description
10/28/2021	1.0E	Initial version published.

Contents

Contents i

About This Release 1

Overview..... 2

Documents 3

IP Support 4

About This Release

This release includes Gowin I3C Dual Clock IP user guide and reference design.

Gowin I3C Dual Clock IP user guide and reference design can be downloaded from the Gowin website, and the reference design has been configured with specific parameters that can be used for simulation, synthesis, placement and routing after adding user design.

Overview

Gowin I3C Dual Clock IP is used for serial communication interface and serial sensor interface to send or receive data. Gowin I3C Dual Clock IP provides an I3C bus communication controller with REG interface and APB interface.

Table 1 Gowin I3C Dual Clock IP Overview

I3C Dual Clock IP	
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis [®]
Application Software	Gowin Software (V1.9.8.01 and above)

Documents

The software release file contains Gowin I3C Dual Clock IP manuals, which are listed below:

Table 2 Gowin I3C Dual Clock IP Documents

Documents	Description
IPUG787, Gowin I3C Dual Clock IP User Guide.pdf	PDF
RN787, Gowin I3C Dual Clock IP Release Note.pdf	PDF

IP Support

Since the requirements of user design and the maximum frequency are different, the reference design does not include FPGA specific location (.cst) and timing constraints (.sdc) documents, and you can determine the location and timing constraints on your own.

For the customized IP design and support, please contact Gowin sales and support line.

Website: www.gowinsemi.com

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