



Gowin HDLC IP

Release Note

RN763-1.0E, 03/16/2021

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Revision History

Date	Version	Description
03/16/2021	1.0E	Initial version published.

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About This Guide

This release includes the Gowin HDLC IP reference design and user guide.

Gowin HDLC IP user guide and reference design are available at Gowin Website. Take specific parameters as an example for the reference design, and it can be used for simulation, synthesis, placement and routing after adding user design.

Overview

Gowin HDLC IP is a controller based on the basic frame of the HDLC protocol, which is located at the link layer of the OSI reference model released by ISO.

Table 1 Gowin HDLC IP Overview

Gowin HDLC IP	
Delivered Doc.	–
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	–
Synthesis Software	Synplify Pro/GowinSynthesis
Application Software	Gowin Software

Documents

This IP release file contains the following documents.

Table 2 Gowin HDLC IP Documents

Documents	Description
IPUG763 , Gowin HDLC IP User Guide.pdf	PDF
RN763, Gowin HDLC IP Release Note.pdf	PDF

IP Support

Since the requirements of user design and the highest frequency are different, the reference design does not include FPGA specific location (.cst) and timing constraints (.sdc) documents, and you can determine the location and timing constraints on your own.

For the customized IP design and support, please contact Gowin sales and support line.

Official Website: www.gowinsemi.com

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