Gowin USB HSIC PHY IP

User Guide

IPUG792-1.0E, 01/24/2022

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Revision History

Date	Version	Description
01/24/2022	1.0E	Initial version published.

Contents

Contents i

List of Figures ii

List of Tables iii

1 About This Guide 1

1.1 Purpose 1

1.2 Related Documents 1

1.3 Terminology and Abbreviations 1

1.4 Support and Feedback 2

2 Function 3

2.1 Overview 3

2.2 Features 3

2.3 Resource Utilization 4

3 Functional Description 5

3.1 USB_HSIC_ PHY Diagram 5

3.2 USB HSIC PHY IO Constraints 6

4 Signal Description 7

5 Interface Configuration 9

List of Figures

Figure 3-1 Implementation Diagram 5
Figure 5-1 IP Core Generator 9
Figure 5-2 Open USB HSIC PHY Core..... 10
Figure 5-3 Configuration Interface 11

List of Tables

Table 1-1 Terminology and Abbreviations 1
Table 2-1 Resource Utilization 4
Table 4-1 Signal Description 7

1 About This Guide

1.1 Purpose

Gowin USB HSIC PHY IP User Guide is intended to help you learn the features and usage of Gowin USB HSIC PHY IP by the functional description, signal description, and interface configuration, etc.

1.2 Related Documents

You can find the related documents at GOWINSEMI website: www.gowinsemi.com.

1. DS102, GW2A series of FPGA Products Data Sheet
2. DS226, GW2AR series of FPGA Products Data Sheet
3. SUG100, Gowin Software User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
IP	Intellectual Property
HSIC	High-Speed Inter-Chip
NRZI	Non-Return to Zero Inverted
EOP	End-of-Packet

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com.

E-mail: support@gowinsemi.com

2 Function

2.1 Overview

High-Speed Inter-Chip (HSIC) interface consists of two signals, a bi-directional data strobe signal (STROBE) and a bi-directional DDR data signal (DATA) that is synchronous to the STROBE signal. The HSIC interface provides high-speed 480Mbps USB transfer.

Gowin USB HSIC PHY IP can implement the PHY layer functions of HSIC interface, including synchronization, bit stuffing, End-of-Packet (EOP), and Non-Return to Zero Inverted (NRZI) encoding.

2.2 Features

The features of Gowin USB HSIC PHY IP include:

- USB2.0 high-speed 480Mbps data rate only
- Source-synchronous serial interface
- No hot Plug-n-Play support; the interface is always connected.
- Signals driven at LVCMOS12V level
- Maximum trace length of 10cm
- Supports GW2A/GW2AR series of FPGA products only
- Supports PHY of Device only

2.3 Resource Utilization

Take Gowin GW2A-18 device as an instance, and Table 2-1 shows its resource utilization.

Table 2-1 Resource Utilization

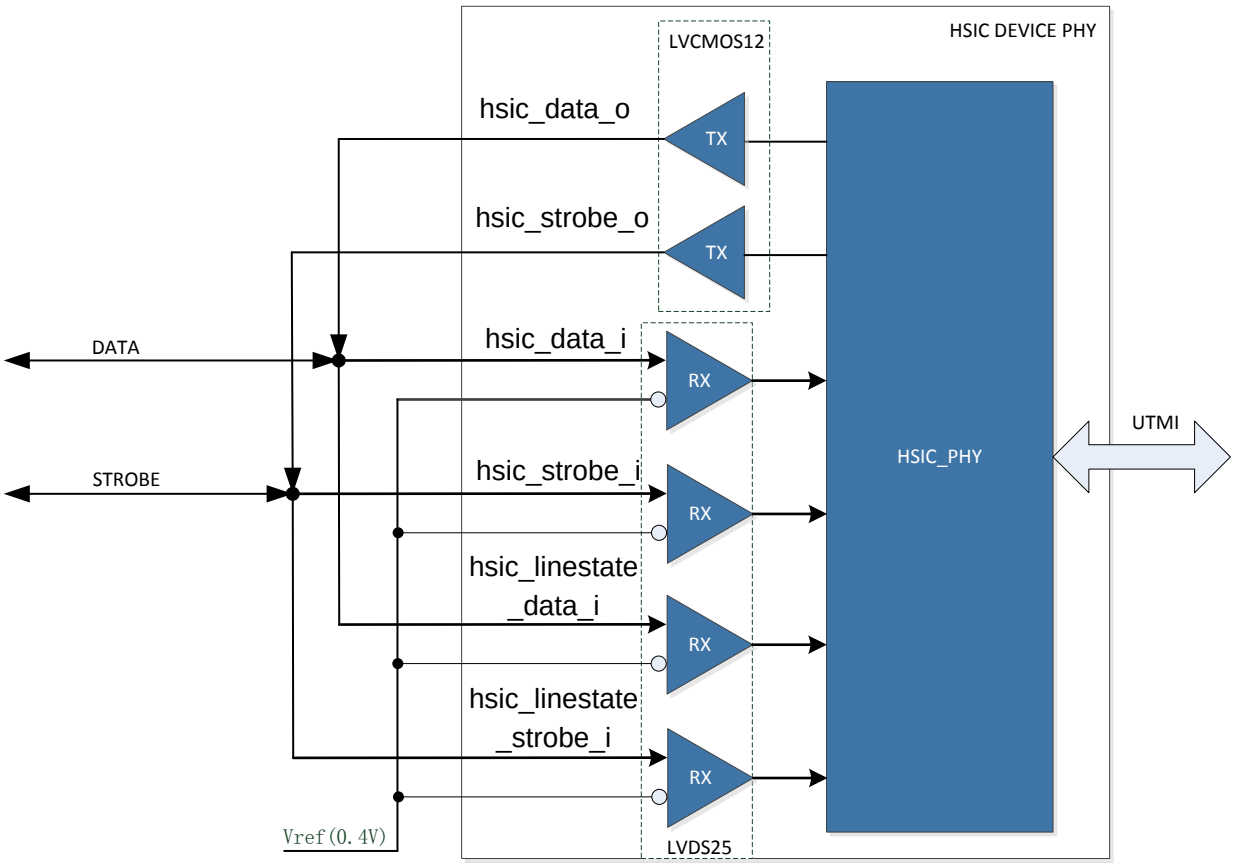
Part Number	Programming Language	LUT4	REG
GW2A-LV18PG484C8/I7	Verilog	682	150

3 Functional Description

3.1 USB_HSIC_ PHY Diagram

Gowin USB HSIC PHY IP can implement the PHY functions of HSIC interface, including synchronization, bit stuffing, EOP, and NRZI encoding, and the implementation diagram is as shown below.

Figure 3-1 Implementation Diagram



3.2 USB HSIC PHY IO Constraints

1. You can see the followings for the IO port attribute constraints.

NO.	Port Name	IO_TYPE	PULL_MODE	DRIVE
1	hsic_data_i	LVDS25	NONE	--
2	hsic_strobe_i	LVDS25	NONE	--
3	hsic_data_o	LVCMOS12	NONE	8
4	hsic_strobe_o	LVCMOS12	NONE	8
5	hsic_linestate_data_i	LVDS25	NONE	--
6	hsic_linestate_strobe_i	LVDS25	NONE	--

2. The supply voltage of the I/O Bank is 1.2V, and the supply voltage of VCCX is 2.5V.

4 Signal Description

Signal Description

The descriptions of signals are as shown in Table 4-1.

Table 4-1 Signal Description

No.	Name	I/O	Data Width	Description
1	fclk_i	input	1	Input clock signal (240MHz)
2	clk60m_o[1]	output	1	Output clock signal (60MHz)
3	rst_n_i	input	1	Input reset signal, active-low.
4	hsic_data_i	input	1	HSIC DATA input signal
5	hsic_strobe_i	input	1	HSIC STROBE input signal
6	hsic_data_o	output	1	HSIC DATA output signal
7	hsic_strobe_o	output	1	HSIC STROBE output signal
8	hsic_linestate_data_i	input	1	HSIC DATA line state input signal
9	hsic_linestate_strobe_i	input	1	HSIC STROBE line state input signal
10	utim_reset_i	input	1	Reset signal output by USB controller, active-high.
11	utim_dataout_i	input	8	8-bit TX data parallel
12	utim_txvalid_i	input	1	TX data valid indicator, active-high.
13	utim_txready_o	output	1	TX data ready signal, indicating that PHY can receive the data to be transmitted from the controller.
14	utim_datain_o	output	8	8-bit RX data parallel
15	utim_rxvalid_o	output	1	Rx data valid, active-high.
16	utim_rxactive_o	output	1	Rx data active indicator, indicating that PHY detects the SYNC signal and then starts

No.	Name	I/O	Data Width	Description
				receiving data.
17	utim_rxerror_o	output	1	RX data error; high indicates RX error.
18	utim_linestate_o	output	2	UTMI line status: ● 2’B00: RESET ● 2’B01: CONNECT/RESUME ● 2’B10: IDLE/SUSPEND ● 2’B11: DATA RX&TX
19	utim_opmode_i	input	2	Mode selection signal: ● 2’b00: Normal ● 2’b10: Disable bit stuffing and NRZI encoding ● Others: Reserved
20	utim_termselect_i	input	1	UTMI control selection; fixed input 1'b0.
21	utim_xcvrselect_i	input	2	Transfer mode selection; fixed input 2'b00, only works in HS mode.

Note!

[1] Take this clock as reference for all UTMI interface signals output and input.

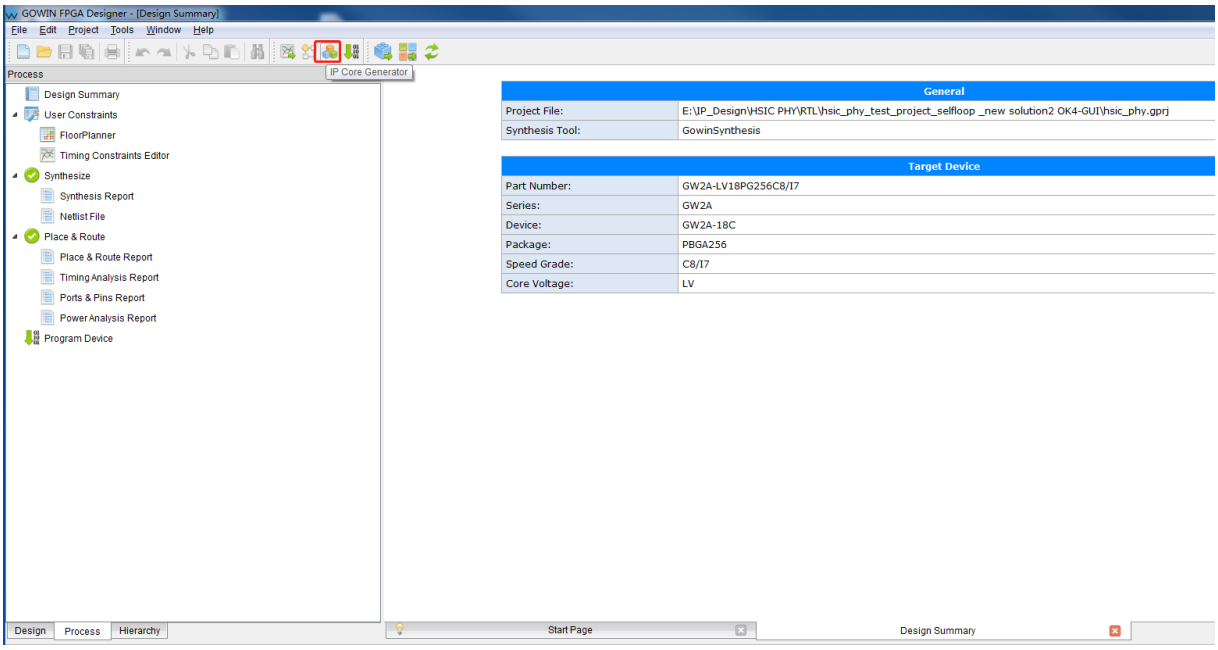
5 Interface Configuration

You can select Tools in Gowin Software to start the IP Core Generator to invoke and configure USB HSIC PHY.

1. Open IP Core Generator

After creating the project, you can click the “Tools” tab in the upper left, then click the IP Core Generator via the drop-down list, as shown in Figure 5-1.

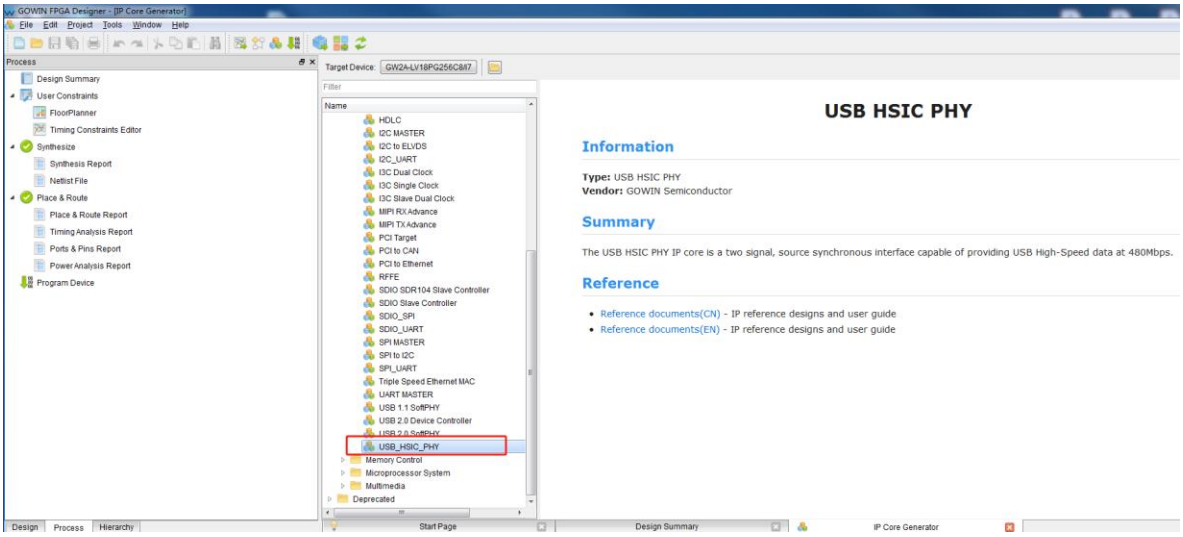
Figure 5-1 IP Core Generator



2. Open USB HSIC PHY IP core

Select “Soft IP Core > Interface and Interconnect > USB HSIC PHY IP”, as shown in Figure 5-2. Double click to open the configuration interface.

Figure 5-2 Open USB HSIC PHY Core

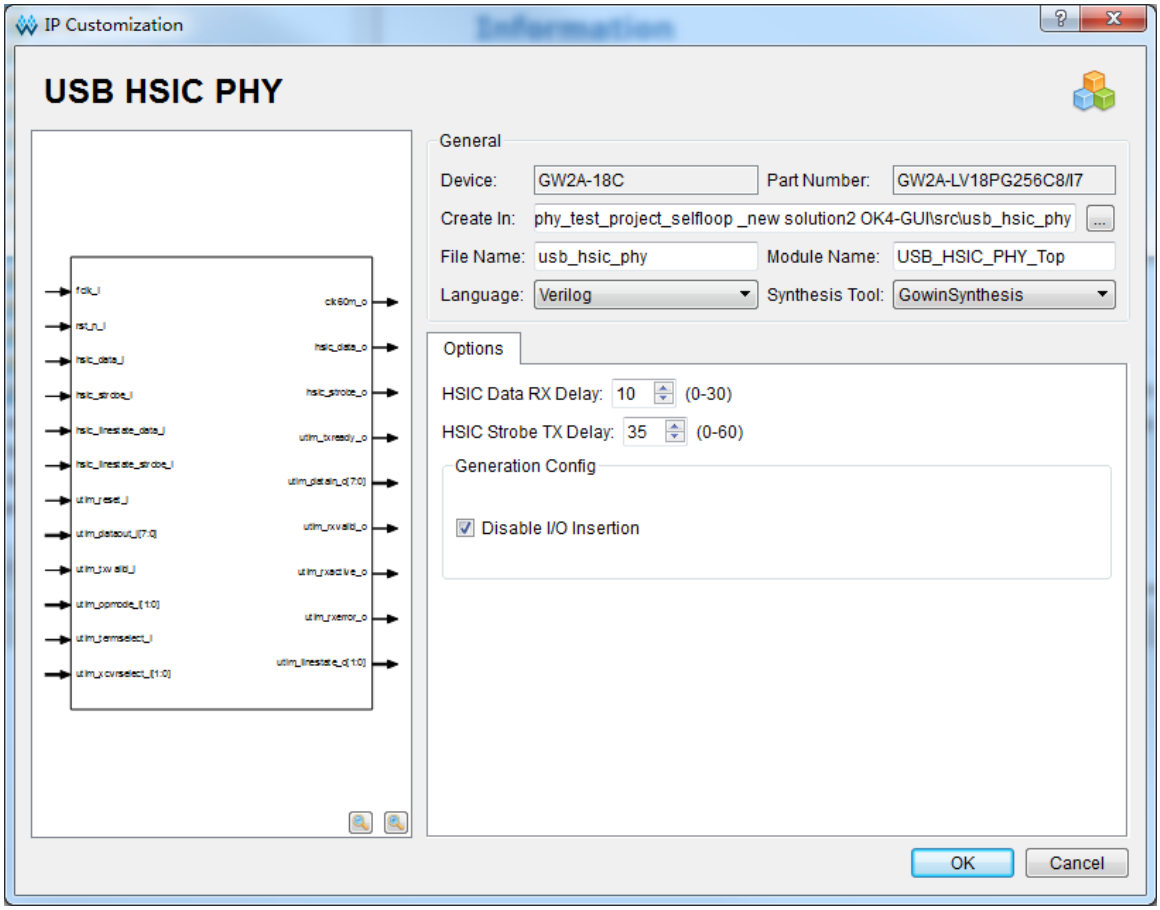


3. USB HSIC PHY IP Configuration Interface

Figure 5-3 shows the configuration interface. The port diagram is on the left, and options are on the right.

- You can configure the file name in File Name.
- You can configure the top module name in Module Name.

Figure 5-3 Configuration Interface

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