



Gowin SPI to I²C IP

User Guide

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Revision History

Date	Version	Description
03/12/2021	1.0E	Initial version published.
01/11/2022	1.1E	● IP structure diagram updated. ● Parameter configuration removed.
04/11/2025	1.2E	Reference design removed.

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1 About This Guide

1.1 Purpose

Gowin SPI to I²C IP user guide provides the descriptions of features and performance, functions, GUI and reference design to help you learn the usage of Gowin SPI to I²C IP.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find related documents at www.gowinsemi.com.

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS821, GW1NS series of FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS841, GW1NZ series of FPGA Products Data Sheet](#)
- [DS861, GW1NSR series of FPGA Products Data Sheet](#)
- [DS881, GW1NSER series of SecureFPGA products Data Sheet](#)
- [DS891, GW1NRF series of Bluetooth FPGA Products Data Sheet](#)
- [DS961, GW2ANR series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Abbreviations and Terminology

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
I ² C	Inter-Integrated Circuit
IP	Intellectual Property

Terminology and Abbreviations	Meaning
SPI	Serial Peripheral Interface

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

SPI is a high-speed, full-duplex, synchronous communication bus.

I²C is a two-wire serial bus that is used to connect the micro-controller with its peripherals.

Gowin SPI to I²C IP can meet the needs of FPGA users by reducing the complexity of system development and decreasing product development time. The IP is located between the SPI and I²C interfaces and has a user-friendly interface to implement the I²C data transceiver control function based on the SPI interface.

Table 2-1 Gowin PCI to I²C IP Overview

Gowin PCI to I ² C IP	
Logic Resource	See Table 3-1.
Delivered Doc.	
Design Files	Verilog (encryption)
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.7.02Beta and above)

Note!

For the devices supported, you can click [here](#) to get the information.

3 Features and Performance

3.1 Features

- Supports data communication between SPI and I²C.
- The SPI interface operates in Slave mode.
- SPI interface completes data interaction with the SPI Master by interrupts.
- The input working clock of the IP must be at least 4 times faster than the SPI input clock.
- SPI interface uses big-endian data format for transmission.
- I²C interface operates in master mode.
- I²C interface supports 7-bit address mode, and 10-bit address mode is not supported.
- I²C interface operating rate can be set flexibly via registers.
- SPI interface RX FIFO has a depth of 510 bytes.
- SPI interface TX FIFO has a depth of 255 bytes.
- Can be synthesized.
- Designed in Verilog.

3.2 Performance

The working frequency of Gowin SPI to I²C IP depends on the maximum working frequency supported by the IP on the selected chip.

3.3 Resource Utilization

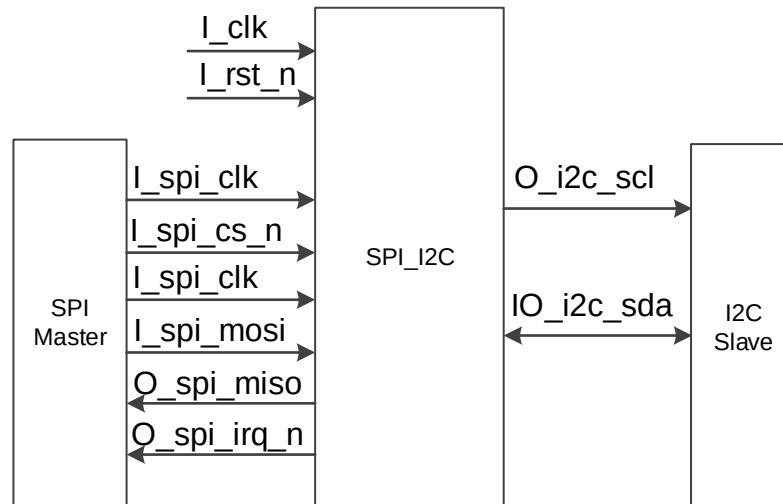
Table 3-1 Resource Utilization

Chip Type	Language	LUT4 Resources	REG Resources
GW2A-LV18PG256C7/I6	Verilog	≤660	≤386

4 Functional Description

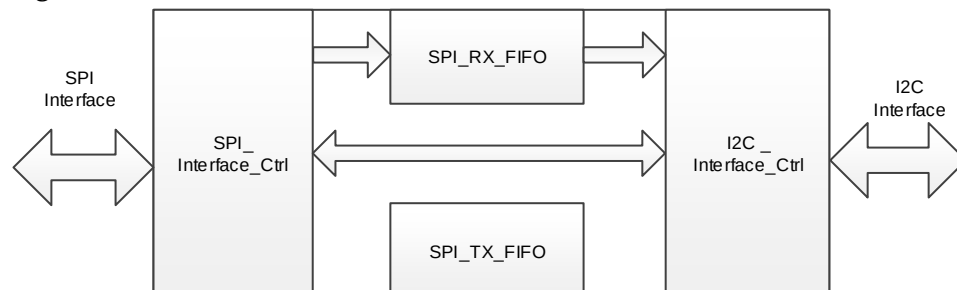
Gowin SPI to I²C IP is located between SPI interface and I²C interface. SPI mainly includes data, clock, chip selected, interrupt and other signals, and I²C includes data and clock signals.

Figure 4-1 System Block Diagram



Gowin SPI to I²C IP system block diagram is shown in Figure 4-2.

Figure 4-2 Structure



The IP includes SPI_Interface_Ctrl, SPI_RX_FIFO, SPI_TX_FIFO, I2C_Interface_Ctrl modules.

- SPI_Interface_Ctrl: Realizes data communication with SPI Master, completes SPI data receiving and sending, interrupt control, status

monitoring and other functions.

- SPI_RX_FIFO: Stores the data received from the SPI Master to be sent to the I²C interface.
- SPI_TX_FIFO: Stores the data received from I²C Slave to be sent to the SPI interface.
- I2C_Interface_Ctrl: Realizes data communication with I²C Slave and interface timing control.

4.1 SPI Interface Control Instruction

4.1.1 Control Instruction

SPI interface control instructions include operations of read, write, read/write, write/write, read register, write register, and read buffer, and the details are shown in the following table.

Table 4-1 SPI Interface Control Instruction

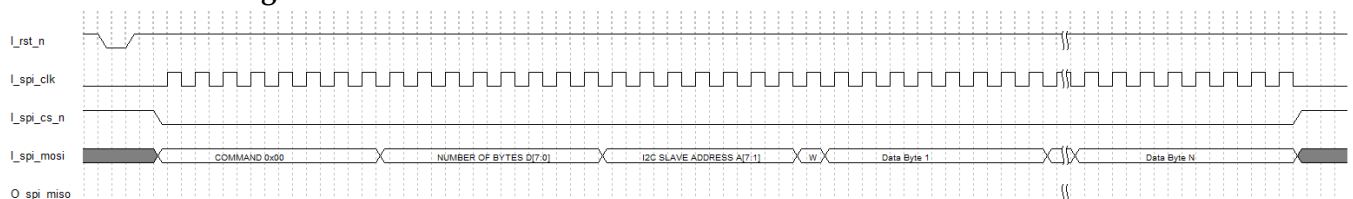
No.	Name	Definition	Width	Type	Description
1	WrI2cData	0x00	8 bits	Write-only	Write N bytes to I ² C bus slave device (N: 1~255)
2	RdI2cData	0x01	8 bits	Read-only	Read N bytes from I ² C bus slave device (N: 1~255)
3	RdAfterWrI2cData	0x02	8 bits	Read / Write	Write N bytes to I ² C bus slave device1 and read M bytes from I ² C bus slave device2 (N: 1~255, M: 1~255)
4	WrAfterWrI2cData	0x03	8 bits	Write-only	Write N bytes to I ² C bus slave device1 and write M Bytes to I ² C bus slave device2 (N: 1~255, M: 1~255)
5	RdBuffer	0x06	8 bits	Read-only	Read the received data from the local Buffer (maximum depth 255)
6	WrReg	0x20	8 bits	Write-only	Configure internal register
7	RdReg	0x21	8 bits	Read-only	Read internal register value

4.1.2 Description

WrI2cData

This instruction is to write N bytes to I²C bus slave device through the SPI interface, and N takes values from 1 to 255.

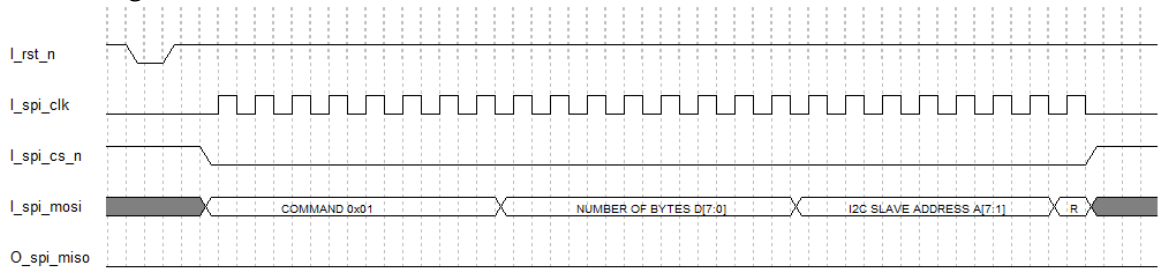
Figure 4-3 WrI2cData



RdI2cData

This instruction is to read N bytes from I²C bus slave device through the SPI interface, and N takes values from 1 to 255.

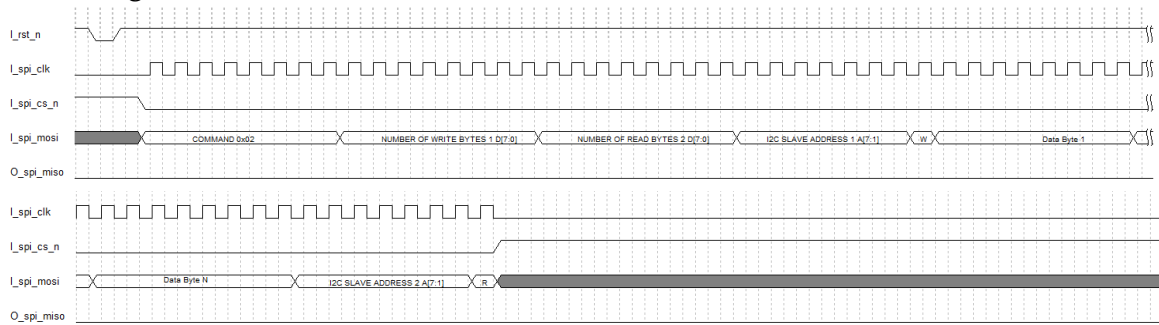
Figure 4-4 RdI2cData



RdAfterWrI2cData

This instruction is to read N bytes from I²C bus slave device1, and then read M bytes from I²C bus slave device2 through the SPI interface. N takes values from 1 to 255, and M takes values from 1 to 255.

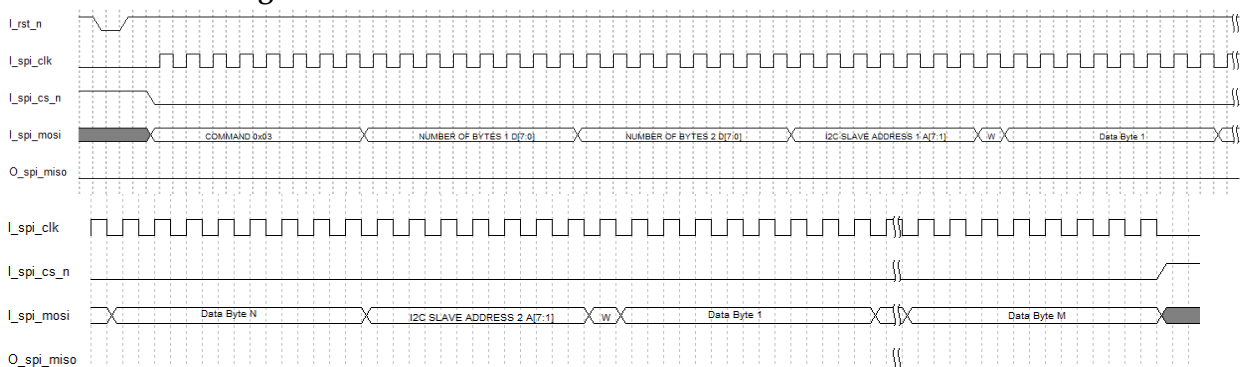
Figure 4-5 RdAfterWrI2cData



WrAfterWrI2cData

This instruction is to write N bytes to I²C bus slave device1, and then and then write M bytes to I²C bus slave device2 through the SPI interface, and N takes values from 1 to 255.

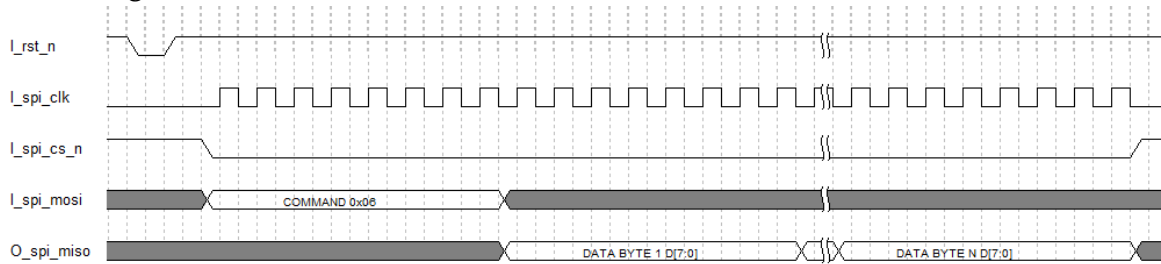
Figure 4-6 WrAfterWrI2cData



RdBuffer

This instruction is to read N bytes from received FIFO through the SPI interface, and N takes values from 1 to 255.

Figure 4-7 RdBuffer



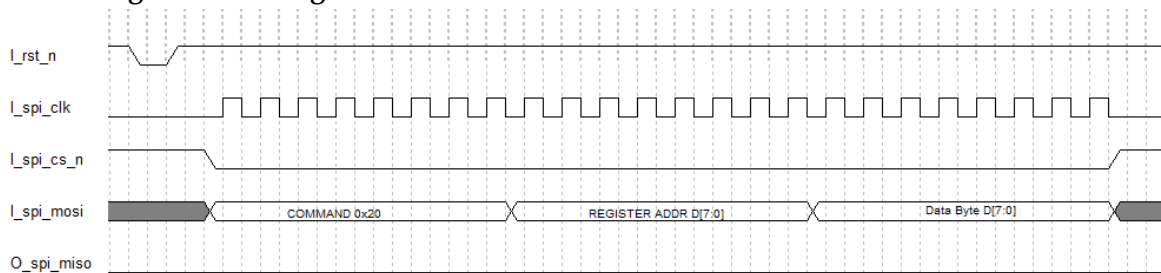
WrReg

This instruction is to configure internal register through SPI interface.

Table 4-2 Register Definition

Name	Address	Data Width	Default	Type	Description
I2CClk	0x00	8	0x00	Read/ Write	I ² C clock data rate configuring register I2C_Bus_Clk_Freq=F _{input operating} clock/4*(I2CClk+1) I2CClk: 0~ 255
I2CAdr	0x01	8	0x00	Read/ Write	I ² C Master address configuring register Bit[7:1]: I2C Master Addr Bit[0]: Reserved
I2CStat	0x02	8	0x00	Read	I ² C Status Register 0xF0: I ² C transmission succeed, triggering interrupt 0xF1: I ² C transmission, when the slave device has no ACK to Slave Addr, triggering interrupt. 0xF2: I ² C transmission, when the slave device has no ACK to Data, triggering interrupt. 0xF3: I ² C bus busy, no interrupt triggered. 0X00: I ² C idle Others: Reserved

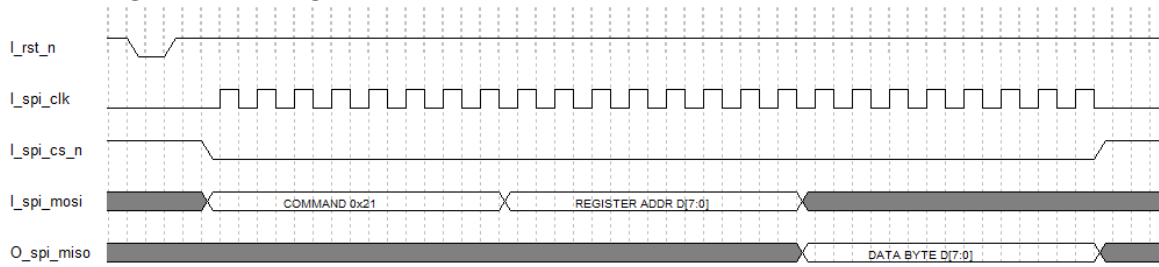
Figure 4-8 WrReg



RdReg

This instruction is to read internal register through SPI interface.

Figure 4-9 RdReg



4.2 Operating Flow

4.2.1 WrI2cData

1. First SPI Master sends instruction 0x00, which transmit the number of bytes sent to the I²C slave, the I²C address and the data to the IP via the SPI interface.
2. Then the IP sends the data to the I²C bus according to the I²C protocol.
3. When all the data is sent, IP sets the status register value to 0xF0 and triggers an interrupt signal to the SPI Master; if there is an ACK exception in the I²C bus transmission, it will abort the transmission and trigger an interrupt signal to the SPI Master.
4. The SPI Master responds to the interrupt and reads the status register value by instruction 0x21, and then determines whether the I²C bus transmission is completed or abnormal according to the read register value.

4.2.2 RdI2cData

1. First the SPI Master sends instruction 0x01 to transmit the number of bytes and I²C address of the I²C bus read operation to the IP through the SPI interface.
2. Then the IP will read the number of bytes from the I²C bus slave according to the I²C protocol.
3. When the number of bytes is read, IP will set the status register value to 0xF0 and trigger an interrupt signal to the SPI Master; if an ACK exception occurs in the I²C bus transmission, it will abort the transmission and trigger an interrupt signal to the SPI Master.
4. The SPI Master responds to the interrupt and reads the status register value by the instruction 0x21.
5. When the register value is 0xF0, it means the I²C read operation succeeds and the SPI Master will send the instruction 0x06 to read data from BUFFER.

4.2.3 RdAfterWrI2cData

1. First the SPI Master sends instruction 0x02 to transmit the number of read/write bytes, I²C address 1 (W) and I²C address 2 (R) to the IP through the SPI interface.
2. Then the IP will read and write the specified number of bytes to the I²C bus according to the I²C protocol.
3. When the specified byte read/write operation is completed, the IP will set the status register value to 0xF0 and trigger an interrupt signal to the SPI Master; if an ACK exception occurs in the I²C bus transmission, it will abort the transmission and trigger an interrupt signal to the SPI Master.
4. The SPI Master responds to the interrupt and reads the status register value by the instruction 0x21.
5. When the register value is 0xF0, it means the I2C read operation succeeds and the SPI Master will send the instruction 0x06 to read data from BUFFER.

4.2.4 WrAfterWrI2cData

1. First the SPI Master sends the instruction 0x03 to transmit the write byte number 1, write byte number 2, I²C address 1 (W), I²C address 2 (W) and the data to the IP through the SPI interface.
2. Then the IP will perform write operations of I²C bus specified number of bytes according to the I²C protocol.
3. When the specified byte write operation is completed, the IP will set the status register value to 0xF0 and trigger an interrupt signal to the SPI Master; if an ACK exception occurs in the I²C bus transmission, it will abort the transmission and trigger an interrupt signal to the SPI Master.
4. The SPI Master responds to the interrupt and reads the status register value by the instruction 0x21, and then determines whether the I²C transmission is completed or abnormal according to the read register value.

5 Port List

The ports of Gowin SPI to I²C IP are as shown in Table 5-1.

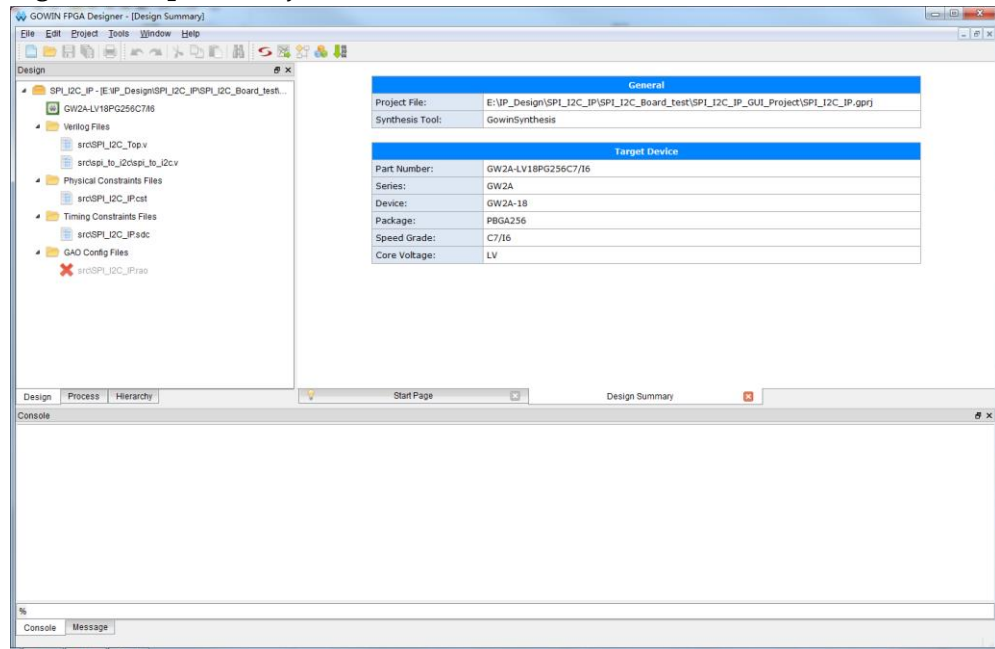
Table 5-1 Signals Description

No.	Signal Name	I/O	Description	Remarks
1	I_clk	I	Clock	The I/O of all the signals takes IP as reference
2	I_rst_n	I	Reset	
3	IO_i2c_sda	I/O	I ² C bus Data	
4	O_i2c_scl	O	I ² C bus Clock	
5	O_spi_irq_n	O	SPI Interface Interrupt	
6	I_spi_clk	I	SPI Interface Clock	
7	I_spi_cs_n	I	SPI Interface chip selected	
8	I_spi_mosi	I	SPI Interface input data	
9	O_spi_miso	O	SPI Interface output data	

6 Interface Configuration

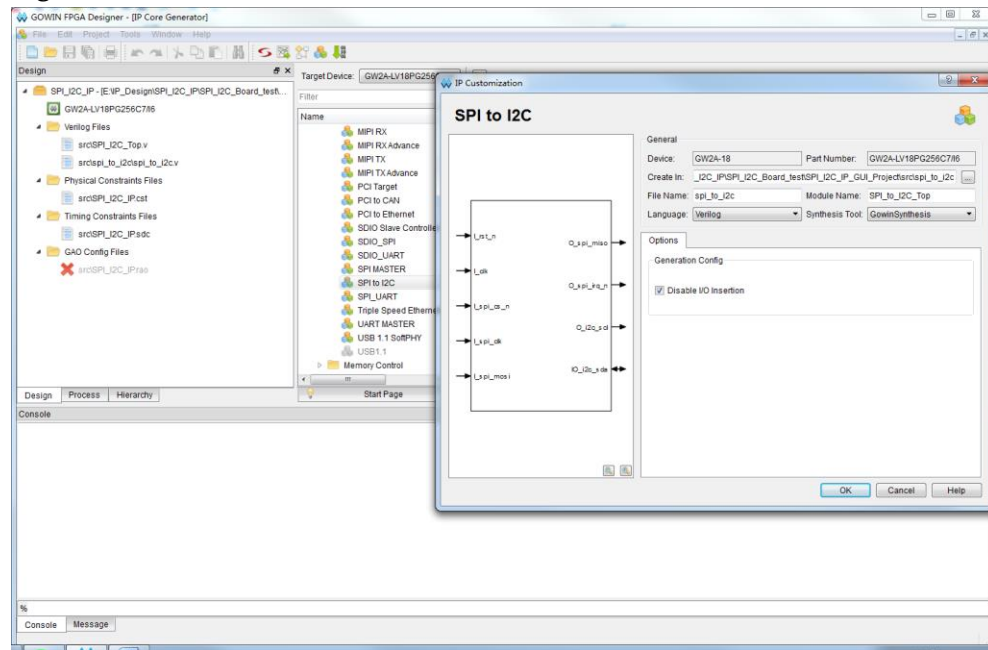
1. Start Gowin Software and open the project as shown below.

Figure 6-1 Open a Project



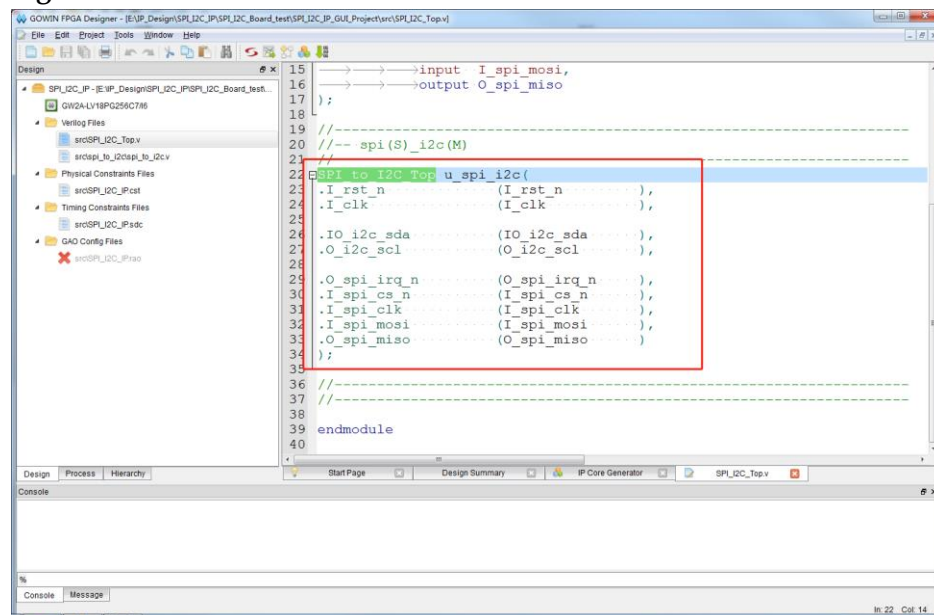
2. Select "Tools > IP Core Generator", then click "OK" to generate SPI_to_I2C Module.

Figure 6-2 Call SPI_to_I2C



3. Instantiate SPI_to_I2C in the user application as shown below .

Figure 6-3 Instantiate SPI to I2C



4. Synthesize, P&R, and download bitstream file to FPGA chip to implement SPI_to_I2C function.

