



Gowin HDLC IP

User Guide

IPUG763-1.0E, 03/16/2021

Copyright© 2021 Guangdong Gowin Semiconductor Corporation. All Rights Reserved.

No part of this document may be reproduced or transmitted in any form or by any denotes, electronic, mechanical, photocopying, recording or otherwise, without the prior written consent of GOWINSEMI.

Disclaimer

GOWINSEMI®, LittleBee®, Arora, and the GOWINSEMI logos are trademarks of GOWINSEMI and are registered in China, the U.S. Patent and Trademark Office, and other countries. All other words and logos identified as trademarks or service marks are the property of their respective holders, as described at www.gowinsemi.com. GOWINSEMI assumes no liability and provides no warranty (either expressed or implied) and is not responsible for any damage incurred to your hardware, software, data, or property resulting from usage of the materials or intellectual property except as outlined in the GOWINSEMI Terms and Conditions of Sale. All information in this document should be treated as preliminary. GOWINSEMI may make changes to this document at any time without prior notice. Anyone relying on this documentation should contact GOWINSEMI for the current documentation and errata.

Revision History

Date	Version	Description
03/16/2021	1.0E	Initial version published.

Contents

Contents	i
List of Figures.....	ii
List of Tables.....	iii
1 About This Guide	1
1.1 Purpose	1
1.2 Related Documents	1
1.3 Terminology and Abbreviations.....	2
1.4 Support and Feedback	2
2 Overview	3
2.1 Introduction to Gowin HDLC IP	3
2.2 Introduction to HDLC	3
3 Features and Performance	5
3.1 Features.....	5
3.2 Max. Frequency	5
3.3 Resource Utilization.....	5
4 Functional Description	6
4.1 HDLC Structure	6
4.2 Port Description	7
5 Timing Description.....	9
6 GUI.....	11
7 Reference Design.....	13

List of Figures

Figure 2-1 HDLC Frame Structure	3
Figure 2-2 Gowin HDLC IP Frame Structure.....	4
Figure 4-1 HDLC TX Implementation Block Diagram	6
Figure 4-2 HDLC RX Implementation Block Diagram	7
Figure 4-3 Gowin HDLC IP Port Diagram	7
Figure 5-1 Gowin HDLC IP TX Timing	10
Figure 5-2 Gowin HDLC IP RX Timing	10
Figure 6-1 Gowin HDLC IP Configuration Interface	11

List of Tables

Table 1-1 Terminology and Abbreviations.....	2
Table 2-1 Gowin HDLC IP Overview	3
Table 3-1 HDLC Resource Utilization.....	5
Table 4-1 Gowin HDLC IP Port Description.....	8
Table 6-1 Option Description	12

1 About This Guide

1.1 Purpose

The purpose of Gowin HDLC IP User Guide is to help you learn the features and usage of this product by providing the descriptions of features, functions, ports, timing, GUI and reference design.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find related documents at www.gowinsemi.com

- [DS100](#), GW1N series of FPGA Products Data Sheet
- [DS117](#), GW1NR series of FPGA Products Data Sheet
- [DS821](#), GW1NS series of FPGA Products Data Sheet
- [DS861](#), GW1NSR series of FPGA Products Data Sheet
- [DS871](#), GW1NSE series of FPGA Products Data Sheet
- [DS881](#), GW1NSER series of FPGA Products Data Sheet
- [DS891](#), GW1NRF series of FPGA Products Data Sheet
- [DS841](#), GW1NZ series of FPGA Products Data Sheet
- [DS102](#), GW2A series of FPGA Products Data Sheet
- [DS226](#), GW2AR series of FPGA Products Data Sheet
- [DS961](#), GW2ANR series of FPGA Products Data Sheet
- [DS976](#), GW2AN-55 Data Sheet
- [SUG100](#), Gowin Software User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
IP	Intellectual Property
LUT	Look-up Tables
HDLC	High-Level Data Link Control
ISO	International Organization for Standardization
OSI	Open System Interconnection

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Introduction to Gowin HDLC IP

Gowin HDLC IP is a controller based on the basic frame of the HDLC protocol, which is located at the link layer of the OSI reference model released by ISO.

Table 2-1 Gowin HDLC IP Overview

Gowin HDLC IP	
Logic Resource	Please refer to Table 3-1.
Delivered Doc.	–
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	–
Synthesis Software	Synplify Pro/GowinSynthesis
Application Software	Gowin Software

2.2 Introduction to HDLC

HDLC is an international standard for data link layer protocol. It is defined by ISO/IEC 13239 and widely used in the field of communication. The frame of HDLC contains five fields: flag field F, address field A, control field C, information field I, and check field FCS.

The HDLC frame structure is shown in Figure 2-1. The first and last fields are both F.

Figure 2-1 HDLC Frame Structure

FLAG	ADDR	CTRL	INFO	FCS	FLAG
------	------	------	------	-----	------

Gowin HDLC IP does not distinguish A field, C field, I field, and FCS field. These fields are all parsed as valid data, as shown in the Figure 2-2.

Figure 2-2 Gowin HDLC IP Frame Structure



3 Features and Performance

3.1 Features

- Supports Flag sequence generation and detection.
- Supports Abort sequence generation and detection.
- Supports Zero insertion and deletion.
- Support 8-bit parallel data interface.

3.2 Max. Frequency

The maximum frequency of Gowin HDLC IP is primarily determined by the device used and the speed grade of the devices. Take GW1NZ-1 series of FPGA for an instance. It can reach up to 100MHz.

3.3 Resource Utilization

Gowin HDLC IP can be implemented by Verilog language. Its performance and resource utilization may vary when the design is employed in different devices, or at different density, speed, grade or the different modes of IP configuration.

Take GW1NZ-1 series of FPGA with default configuration for an instance to introduce resource utilization. The resource utilization is shown in Table 3-1. For application verification on other Gowin FPGA, please pay attention to the post-released information.

Table 3-1 HDLC Resource Utilization

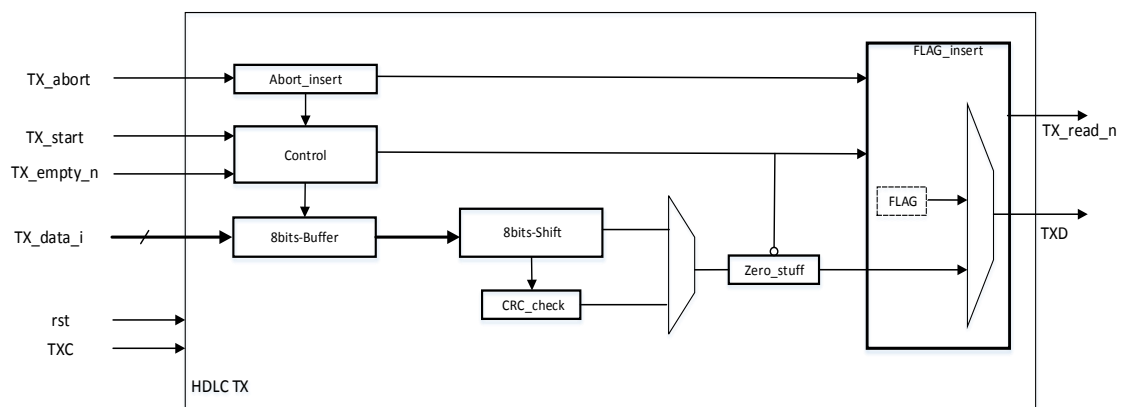
Device Series	Speed Grade	Name	Resource Utilization	Remarks
GW1NZ-1	C6/I5	LUT	111	-
		REG	129	

4 Functional Description

4.1 HDLC Structure

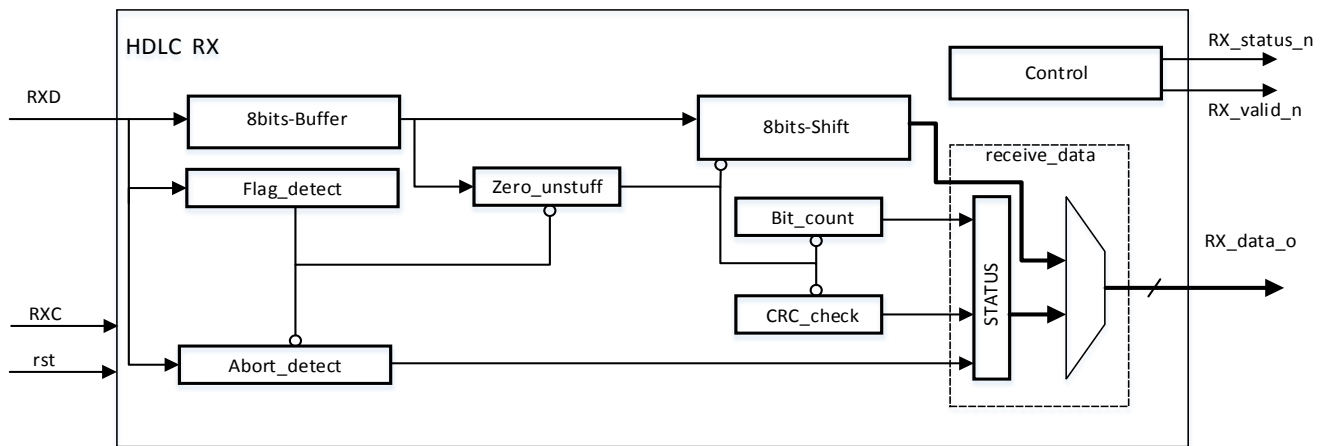
Gowin HDLC IP can convert parallel data to serial through HDLC TX module to complete the HDLC transmission as shown in Figure 4-1. The TX uses TXC as the clock to convert the 8-bit parallel data TX_data_i to serial data and transmits it to TXD.

Figure 4-1 HDLC TX Implementation Block Diagram



Gowin HDLC IP can convert serial data to parallel through HDLC RX to complete HDLC reception. Its diagram is shown in Figure 4-2. The RX uses RXC as the clock to convert the serial data RXD into 8-bit parallel data to transmit to RX_data_o. In one reception, after the valid data transmission is completed, RX_data_o also transmits the status information.

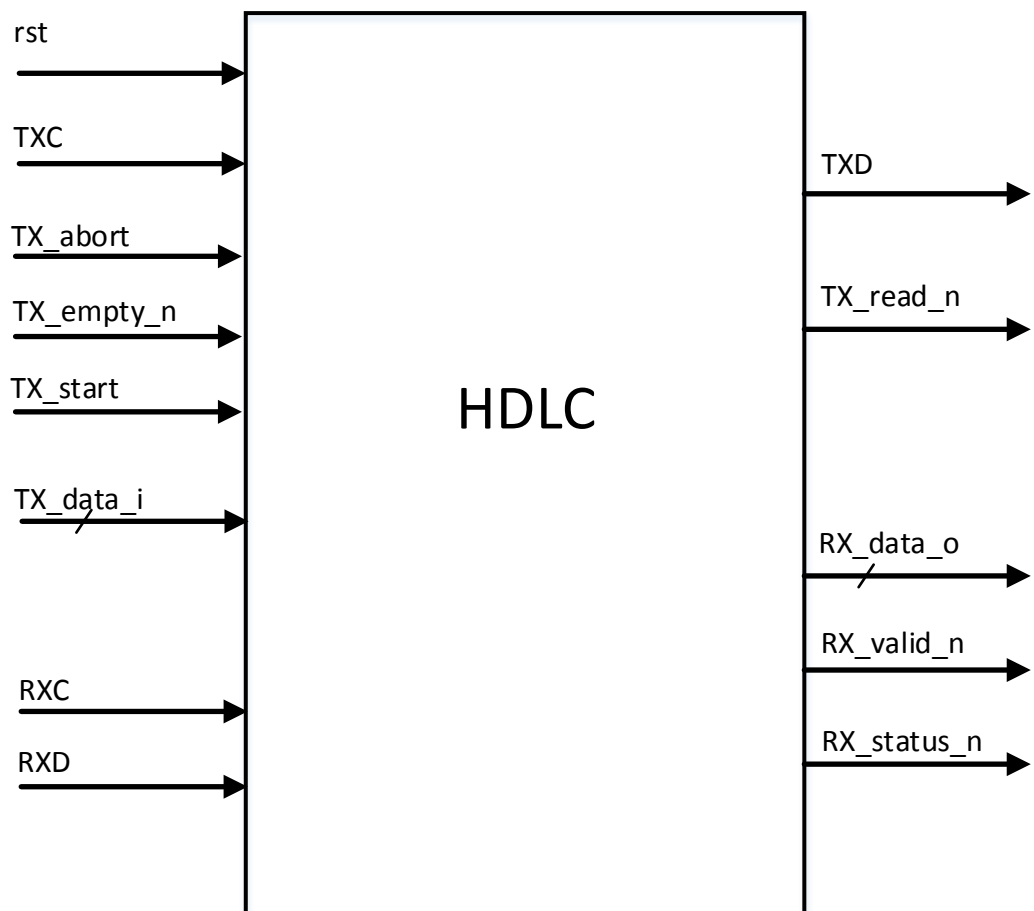
Figure 4-2 HDLC RX Implementation Block Diagram



4.2 Port Description

The IO ports of the Gowin HDLC IP are shown in Figure 4-3 below.

Figure 4-3 Gowin HDLC IP Port Diagram



For the detailed IO ports description, please refer to Table 4-1.

Table 4-1 Gowin HDLC IP Port Description

Signal	I/O	Data Width	Description
rst	input	1	Reset, active-high
TXC	input	1	TX clock
TX_abort	input	1	Abort sequence enable, active-high.
TX_empty_n	input	1	Data empty enable, active-low.
TX_start	input	1	Start enable, active-high.
TX_data_i	input	8	TX parallel input data
RXC	input	1	RX clock
RXD	input	1	RX serial data
TX_read_n	output	1	TX samples TX_data_i, active-low.
TXD	output	1	TX serial data
RX_data_o	output	8	RX parallel output data
RX_valid_n	output	1	RX parallel output data valid, active-low.
RX_status_n	output	1	RX status data valid, active-low.

5 Timing Description

The timing diagram of the Gowin HDLC IP is shown in Figure 5-1 and Figure 5-2.

HDLC TX Timing

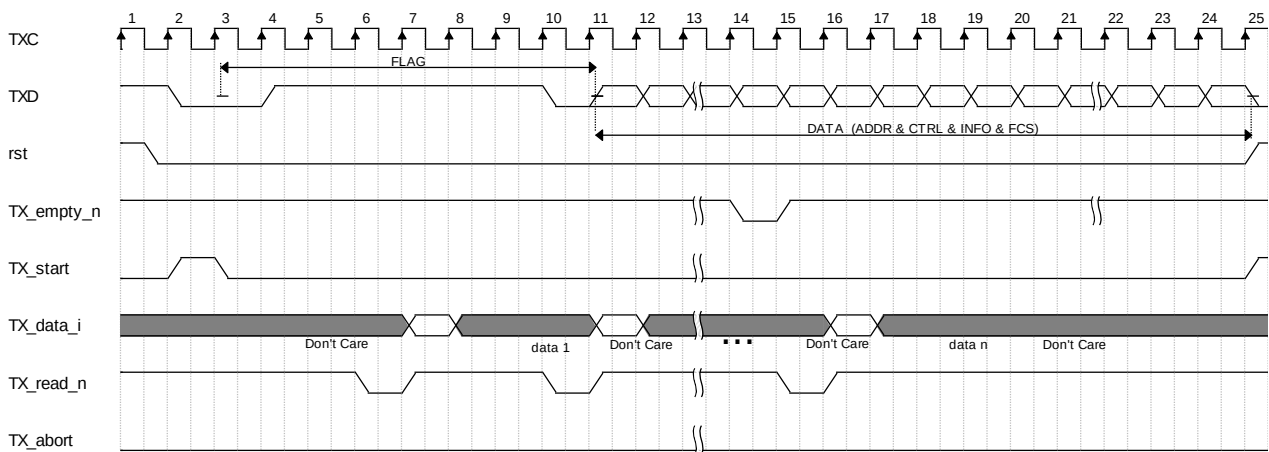
The Gowin HDLC IP TX timing is shown in Figure 5-1. The TX uses TXC as the clock and transmits data on the rising edge of TXC.

When idle, TXD will keep transmitting F field cyclically according to the clock TXC, i.e. 01111110 > 01111110 > 01111110 >

When transmitting data, TX_start is required to hold at least 1 TXC cycle; after a period of time, TX_read_n will be pulled down; IP will sample the TX_data_i, which is on the next TXC rising edge after TX_read_n is pulled down, and it is used as valid parallel data to serially transmit to TXD; after 8 TXC clock cycles, TX_read_n will be pulled down again and the IP repeats sampling parallel data and serially transmits it to the TXD. After 8 TXC clock cycles, the data transmission will be repeated again until TX_empty_n is pulled down; the next TX_data_i sampled by the IP TX will be the last valid data.

After the data transmission is completed, the IP TX will automatically send the FCS field, which can be 8/16/32 bits depending on the configuration.

After the FCS field is sent, it will enter the idle state and keep sending the F field cyclically until the next data transmission comes.

Figure 5-1 Gowin HDLC IP TX Timing

HDLC RX Timing

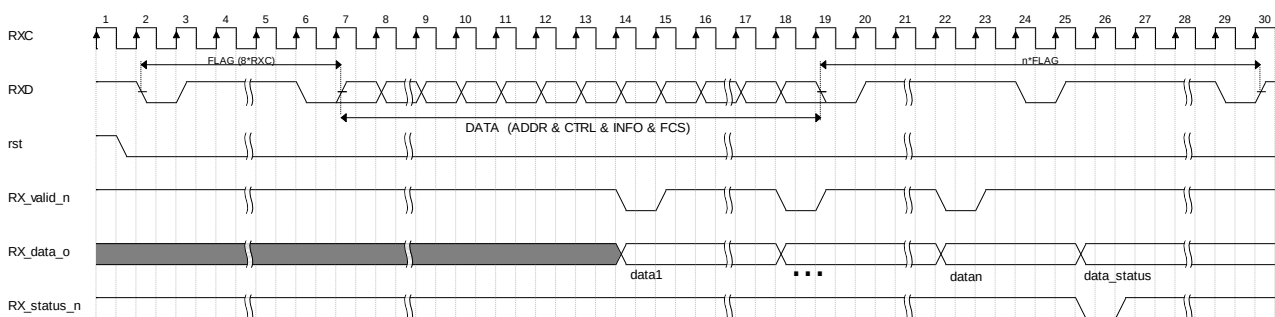
The Gowin HDLC IP RX timing is as shown in Figure 5-2. IP RX uses RXC as the clock and detects data on the rising edge of RXC.

IP RX detects RXD data based on RXC. Between the two F fields is one data transmission. IP RX is divided into data and status in one parsing. The status information of this parsing will be given after the data parsing is completed.

When the RX_valid_n signal pulled down, the RX_data_o is the received valid data. When the RX_status_n signal is pulled down, the status information is given on RX_data_o.

Note!

The status information (8 bits) are: Bit7~ Bit3:5'b11111; Bit2:Abort detection; Bit1:Byte error; Bit0:CRC error.

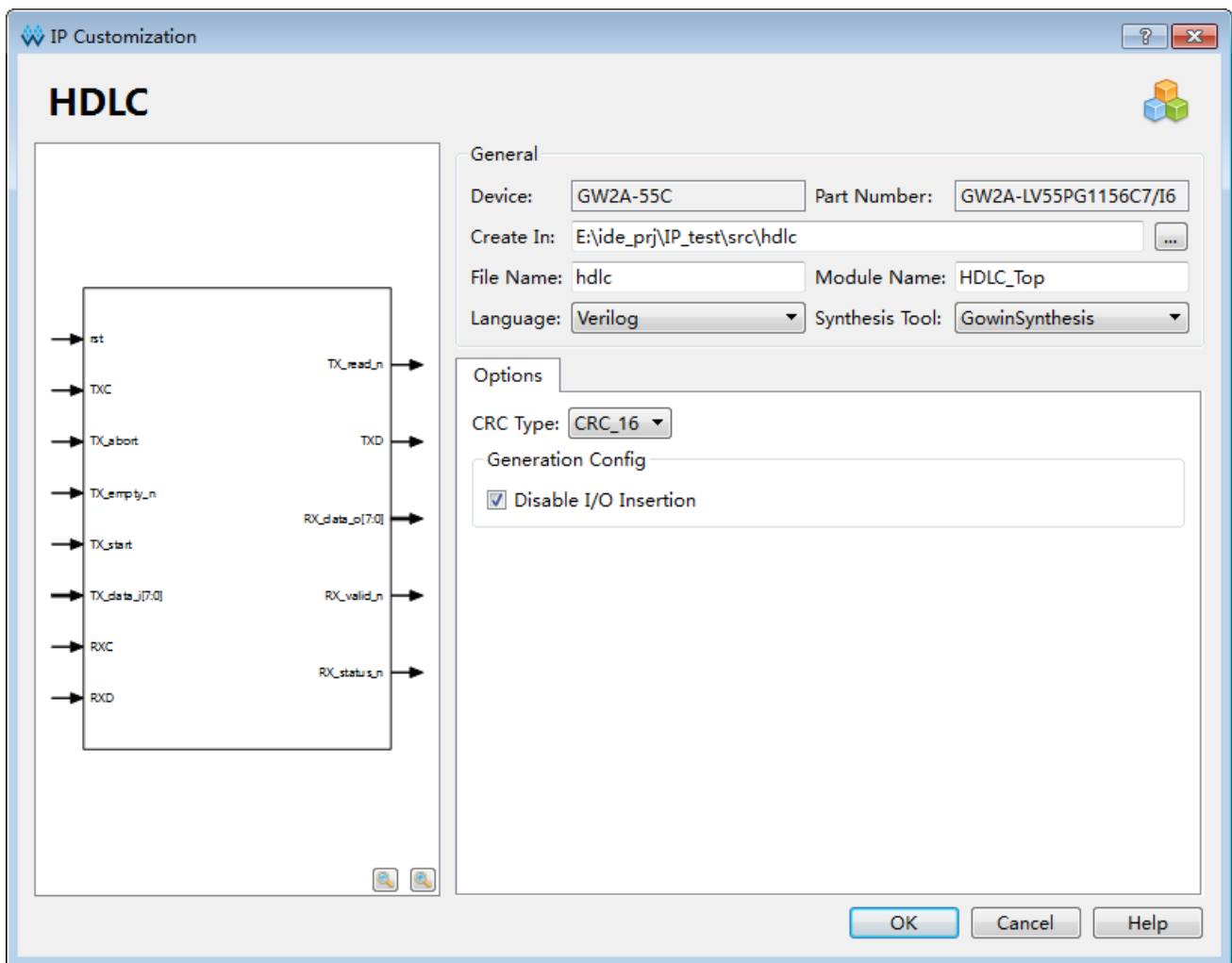
Figure 5-2 Gowin HDLC IP RX Timing

6 GUI

Start "IP Core Generator" from the "Tools" menu in the Gowin software and you can call and configure Gowin HDLC IP.

The Gowin HDLC IP configuration interface is shown in Figure 6-1.

Figure 6-1 Gowin HDLC IP Configuration Interface



The option description is as shown in Table 6-1.

Table 6-1 Option Description

Option	Description
CRC Type	Selects CRC type CRC_8 $x^8+x^2+x^1+1$ CRC_16 $x^{16}+x^{12}+x^5+1$ CRC_32 $x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x^1+1$

7 Reference Design

Please see the Gowin HDLC [Reference Design](#) for details on Gowinsemi website.

