



Gowin XCORR IP

User Guide

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Revision History

Date	Version	Description
02/08/2019	1.0E	Initial version published.
07/04/2025	1.1E	● Section 1.2 Related Documents updated. ● Descriptions of Section 3.3 Latency updated. ● Section 3.4 Resource Utilization updated. ● Gowin XCORR IP port diagram, timing diagram, and interface screenshots updated.

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1 About This Guide

1.1 Purpose

Gowin XCORR IP User Guide provides functional features, port descriptions, timing information, configuration, and reference designs, etc. It is intended to help users quickly understand the features and usage of Gowin XCORR IP. The software screenshots and the supported products listed in this manual are based on Gowin Software V1.9.11.02. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS821, GW1NS series of FPGA Products Data Sheet](#)
- [DS861, GW1NSR series of FPGA Products Data Sheet](#)
- [DS881, GW1NSER Series of SecureFPGA Products Datasheet](#)
- [DS891, GW1NRF series of Bluetooth FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS971, GW2AN-18X & 9X Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)
- [DS961, GW2ANR series of FPGA Products Data Sheet](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)

- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1239, GW5AST series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)
- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1118, GW5ART series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Abbreviations and Terminology

The abbreviations and terminology used in this manual are as shown in Table 1-1 below.

Table 1-1 Abbreviations and Terminologies

Abbreviations and Terminologies	Meaning
ALU	Arithmetic Logical Unit
LUT	Look-up Table
BSRAM	Block Static Random Access Memory
DSP Macros	Digital Singal Processing Macros
I/O Logic	Input/Output Logic

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2Overview

2.1 Gowin XCORR IP

Gowin XCORR IP is designed to perform cross-correlation computations.

Table 2-1 Gowin XCORR IP Overview

Gowin XCORR IP	
Logic Resource	Please refer to Table 3-1.
Delivered Doc.	
Design Files	Verilog
Reference Designs	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software

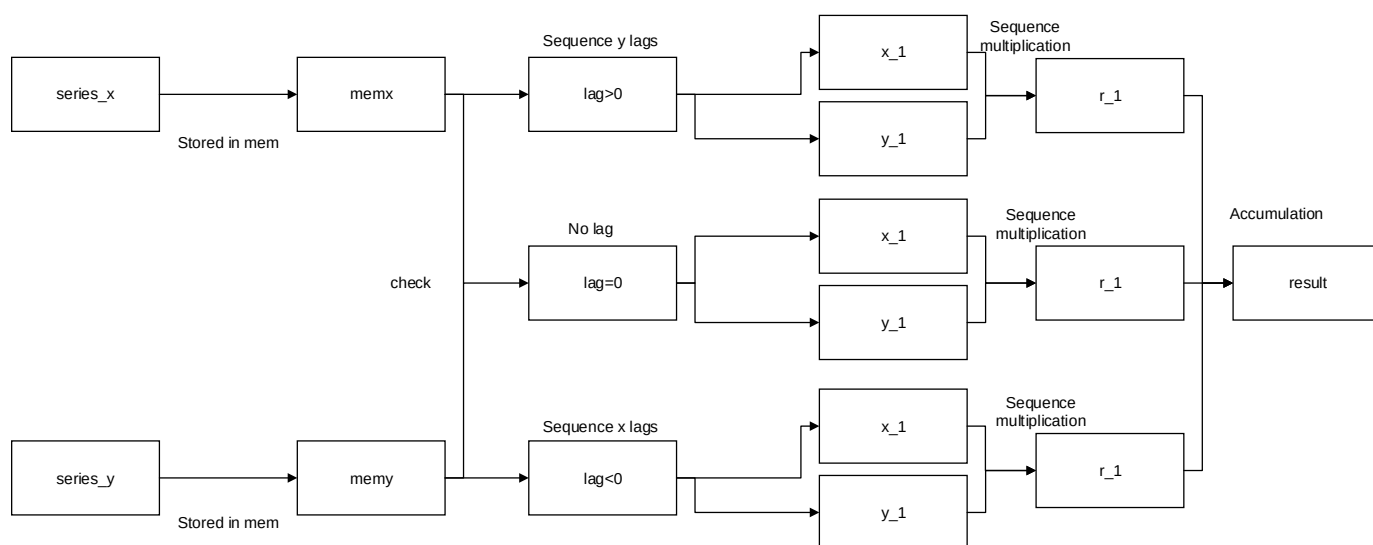
Note !

For the devices supported, you can click [here](#) to get the information.

2.2 Introduction to XCORR

XCORR is the IP that provides cross-correlation operation between two random sequences. Gowin XCORR IP can get cross-correlation values between two random sequences in a maximum delay range. It offers comprehensive functions. The structure diagram is shown as Figure 2-1.

Figure 2-1 XCORR Structure



3 Features and Performance

3.1 Features

- Provides cross-correlation operation between random sequences.
- The length of the input sequence can be customized.
- The data width can be customized.
- The data delay can be customized.

3.2 Max. Frequency

The max. frequency of Gowin XCORR IP is related to the configured length of the input sequence and the data delay.

3.3 Latency

Gowin XCORR IP output latency corresponds to the duration of one delay unit.

3.4 Resource Utilization

Gowin XCORR IP can be realized by Verilog language. Its performance and resource utilization may vary when the design is employed in a different device, or at a different density, speed, or grade.

Take the GW5A-55 device as an example. See Table 3-1 for the Gowin XCORR IP resource utilization. For the applications on the other GOWINSEMI devices, please refer to the later release.

Table 3-1 Gowin XCORR IP Resource Utilization

Device	Speed Grade	Name	Resource Utilization	Note
GW5A-55	C8/I7	Registers	80	Input Data Width = 17
		LUT	246	

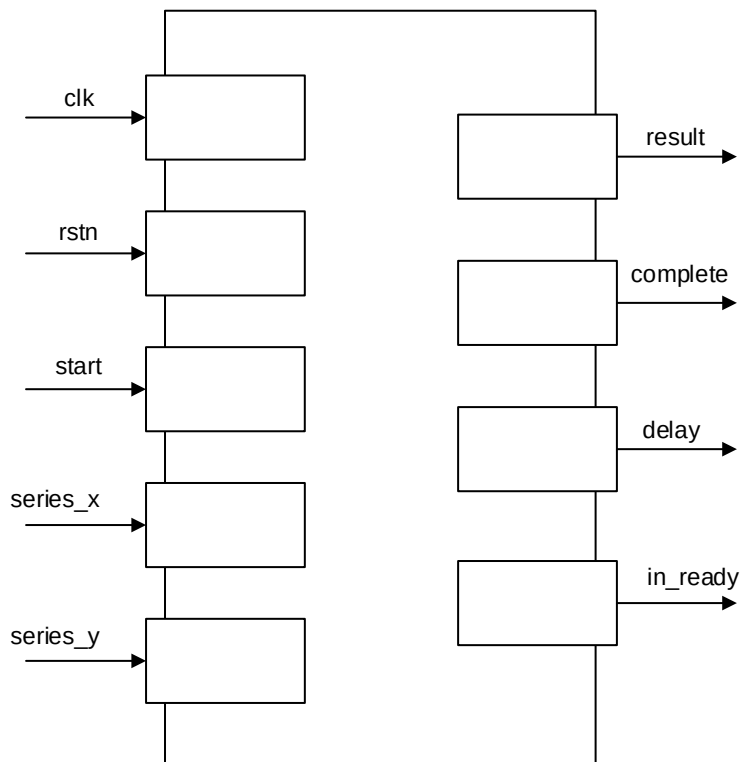
Device	Speed Grade	Name	Resource Utilization	Note
		ALU	24	Sequence Length = 1024 Data Delay = 3
		BSRAM	2	
		DSP	1	

4Function

4.1 XCORR Structure and Function

Gowin XCORR IP can get cross-correlation values between two random sequences in a maximum delay range, and then know the correlation between two sequences. Partial configuration of the IP can be customized by the user including data bit width, sequence length, etc. The functional diagram is presented in Figure 4-1.

Figure 4-1 Gowin XCORR IP Interface Implementation



Users input series_x (sequence x) and series_y (sequence y), and the IP computes the result.

4.2 Data Width Configuration

The data width can be configured in the GUI. The XCORR IP supports the signed bit data. The highest bit is the sign bit. The maximum bit width is 18 bits. The minimum bit width is 16 bits.

4.3 Sequence Length Configuration

The sequence length can be configured through the GUI. The length includes 256, 512, 1024, and 2048.

4.4 Data Delay Configuration

The data delay can be configured through the GUI. The range is from 1 to 16.

5 Port Description

For Gowin XCORR IP ports description, see Table 5-1.

Table 5-1 Gowin XCORR IP IO List

Signal	I/O	Description
series_x	input	Input a random sequence series_x
series_y	input	Input a random sequence series_y
clk	input	Clock signal
rstn	input	Reset signal, active-low.
start	input	Starting signal
result	output	result
delay	output	Delay signal,signed.
complete	output	Completion signal; when it is high, the value on result is valid.
in_ready	output	Input ready

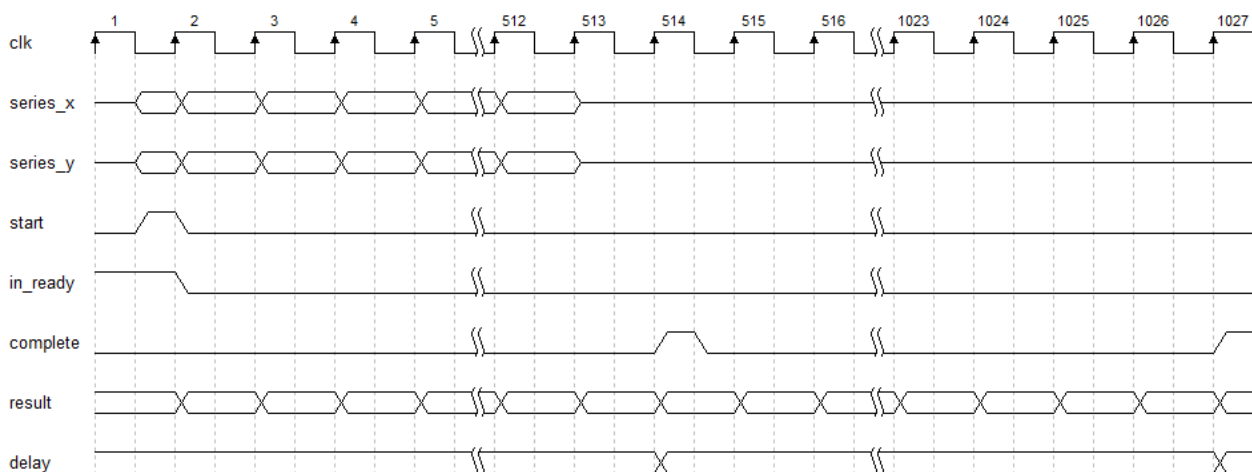
The port diagram is as shown in Figure 4-1.

6 Timing Description

This chapter describes the XCORR IP timing.

Gowin XCORR IP signal timing is as shown in Figure 6-1. Following the falling edge of the start signal, input data series_x and series_y are processed. The computation result is output upon arrival of the complete signal.

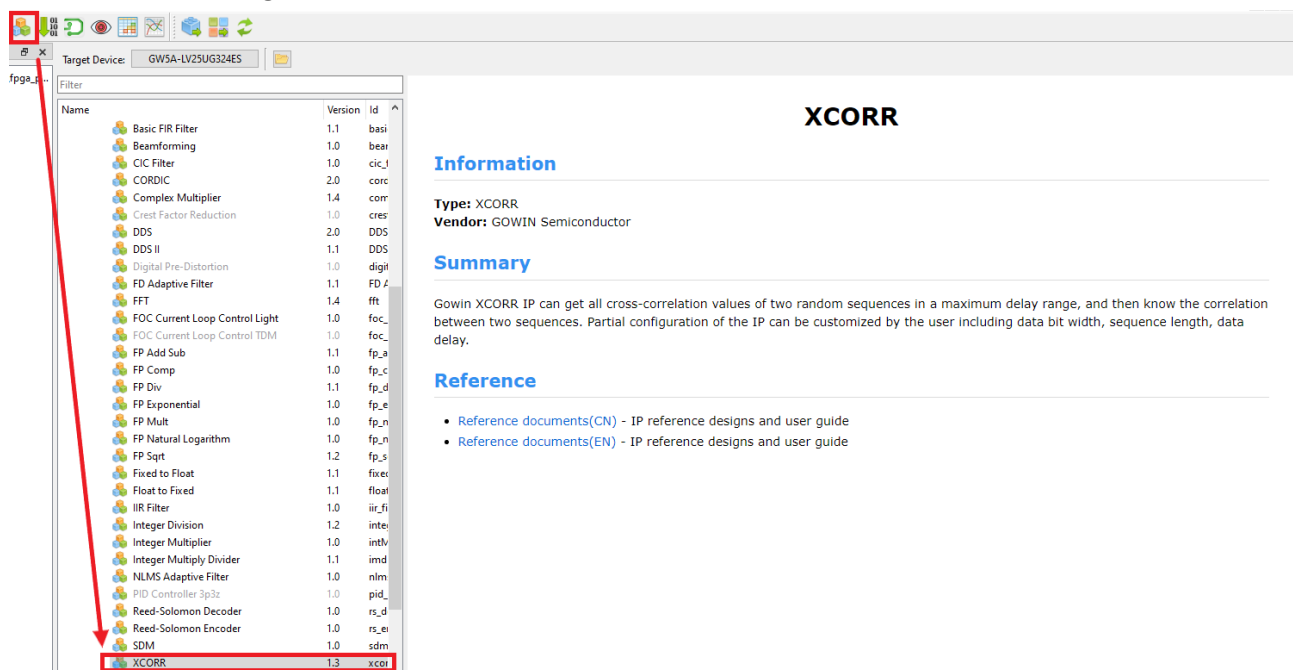
Figure 6-1 Gowin XCORR IP Signal Timing



7 GUI

1. In Gowin Software, the "IP Core Generator" tool can be launched from the "Tools" menu to call and configure XCORR IP. After creating a project, navigate to "IP Core Generator > Soft IP Core > DSP and Mathematics > XCORR" to launch the XCORR, as shown in Figure 7-1.

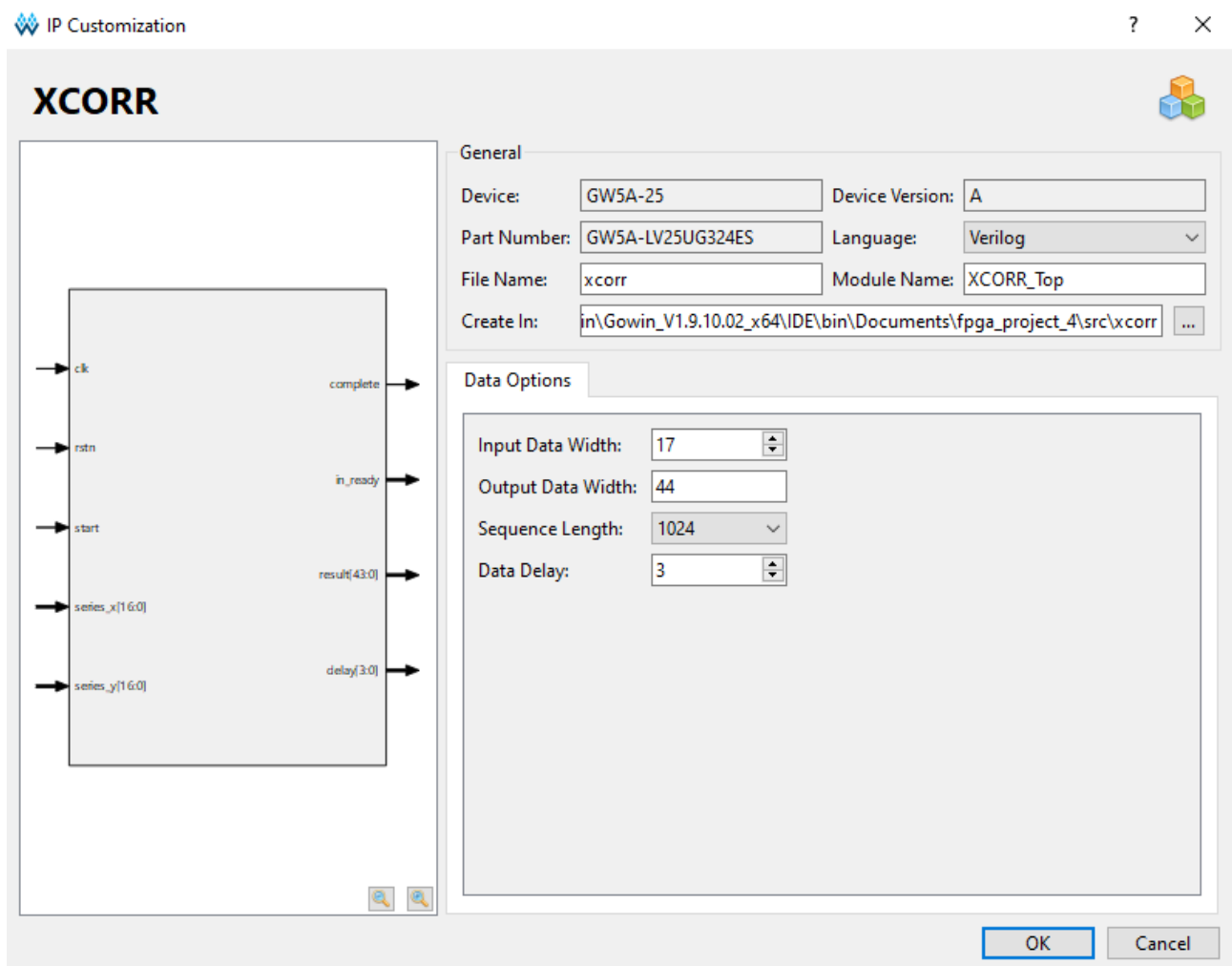
Figure 7-1 Call XCORR



2. Open the XCORR IP core.

Gowin XCORR IP interface is as shown in Figure 7-2. Configure the parameters according to your requirements, then click "OK" to generate the XCORR IP.

Figure 7-2 Gowin XCORR IP Interface



The parameter configuration descriptions on the GUI are as follows:

- Input Data Width: Used to select input data width (16–18).
- Output Data Width: Output data width (read-only).
- Sequence Length: Used to select input sequence length (256/512/1024/2048).
- Data Delay: Data delay (1–16).

8 Reference Designs

Please refer to the test cases in the [ref design](#) folder.

