



Gowin FFT IP

User Guide

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Revision

Date	Revision	Description
12/20/2018	1.0E	Initial version released.
03/28/2019	1.1E	Supported products updated.
12/18/2019	1.2E	• Figures updated. • Fixed the maximum number of points supported. • Description of resource utilization added.
07/02/2021	1.3E	• I/O Description added when dynamic configuration added. • Description of section 5.3.3 updated.
05/12/2022	1.4E	IP configuration interfaces and descriptions updated.

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1 About This Guide

1.1 Purpose

Gowin FFT IP User Guide mainly includes function description, signal definition, working principle, GUI call, etc., which is designed to help you quickly understand the features and usage of Gowin FFT IP.

1.2 Related Documents

The latest user guides are available on the Gowin website. Refer to the related documents at www.gowinsemi.com:

1. [DS100, GW1N series of FPGA Products Data Sheet](#)
1. [DS821, GW1NS series of FPGA Products Data Sheet](#)
2. [DS117, GW1NR series of FPGA Products Data Sheet](#)
3. [DS861, GW1NSR series of FPGA Products Data Sheet](#)
4. [DS841, GW1NZ series of FPGA Product Data Sheet](#)
5. [DS871, GW1NSE series of SecureFPGA Products](#)
6. [DS881, GW1NSER series of SecureFPGA Products](#)
7. [DS891, GW1NRF series of Bluetooth FPGA Product Data Sheet](#)
8. [DS102, GW2A series of FPGA Products Data Sheet](#)
9. [DS226, GW2AR series of FPGA Products Data Sheet](#)
10. [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1 below.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
FFT	Fast Fourier Transformation
BSRAM	Block Static Random Access Memory
REG	Register
DSP	Digital Signal Processing

1.4 Technical Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

Gowin FFT IP provides low resource architecture. Its parameter configuration is flexible; it can support forward and reverse conversion, 8-16384 points, optional DSP acceleration, forward/reverse output, scaling, etc. to meet your requirements.

2.1 Features

- Data bit width supports 8-36 bits.
- The twiddle factor width supports 8-36 bits.
- Supports 8-16384 points.
- Forward and reverse FFT transform.
- An optional base 2nd-order digital reduction scheme, including a specified number of bits per right shift (RS111), dynamic configuration through a port without shifting.
- Supports forward/ reverse output.

2.2 Resource Utilization

Gowin FFT IP employs the Verilog language. The resource utilization varies greatly due to different configuration. The detailed resource is subject to the generated IP. Take the default configuration (1024 points) as an instance, the resource utilization is as listed in Table 2-1.

Table 2-1 Resource Utilization

Device series	Speed Grade	IP	LOGICS	REGS	BSRAMS	DSP
GW2A-55	C8/I7	FFT	656	210	DP: 4	MULTADDALU18X18: 2
					rROM: 2	

3 Working Principle

3.1 Structure

The basic structure of the Gowin FFT IP is shown in Figure 3-1. FFT is a fast algorithm of direct Fourier transform (DFT). The DFT is given by:

$$X(k) = \sum_{n=0}^{N-1} x(n)W_N^{nk}$$

Here W_N is determined by

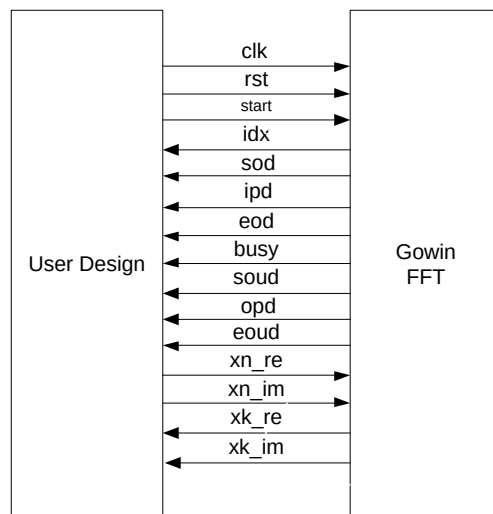
$$W_N = e^{-j\frac{2\pi}{N}}$$

The inverse Fourier transform is given by

$$x(n) = \frac{1}{N} \sum_{k=0}^{N-1} X(k)W_N^{-nk}$$

Because W_N has a strong periodicity, the fast arithmetic form FFT of DFT can be obtained through a certain mathematical transformation, namely the fast Fourier algorithm such as base 2 and base 4.

Figure 3-1 Gowin FFT IP Structure



3.2 Static Configuration

3.2.1 Set the Number of Points

The number of FFT points can be configured as a fixed point through the GUI, or it can be configured to be input through the port at runtime. In practical applications, if you can determine the number of FFT points, try to configure the mode of FFT points as fixed point, because the dynamic port input will consume additional logic resources. In dynamic mode, the FFT IP will occupy as many resources as the maximum number of points. Therefore, when setting the maximum number of points, it should be calculated accurately in advance. Currently only fixed point configuration mode is supported.

3.2.2 FFT mode

The FFT IP supports forward, reverse, and transitions determined by the port signal at runtime. Dynamic mode will take up more logical resources and timing performance may be worse.

3.2.3 Output Sequence

The output sequence order can be selected as natural sequential output or reverse output.

3.2.4 Reduction Method

FFT IP supports several schemes for shifting 1 bit right after each

base 2, dynamically determining the port, and not shifting. The low resource structure also supports the data block floating point mode.

3.2.5 Data Width

The internal operation of the FFT converter supports a bit width of 8-36 bits, and the rotation factor width supports 8-36 bits. When the data is not reduced, the internal decimal width can be selected, and the decimal width supports 0-6 bits. The converter supports arbitrarily setting the input bit width and the decimal width as long as the sum of the two falls within 8-36 bits. The output bit width is automatically determined by the system. Usually, the output bit width is not less than the sum of the input bit width and the decimal place width.

3.2.6 Precision Reduction Method

FFT IP supports two methods of precision reduction, including truncation and rounding. The truncation saves more chip resources, and the result obtained by the rounding will be more accurate.

3.2.7 Multiplier Type

FFT IP supports a DSP-accelerated circuit structure that also supports a multiplier circuit composed of logic devices, and allows the synthesizer to be dynamically determined at the time of integration. Dynamically determining the type of device may result in an excessively long synthesis time and a poor synthesis result.

3.2.8 Data and Twiddle Factor Memory Types

Since the FFT algorithm processes a large amount of data online, it inevitably requires a large amount of memory. The IP design supports BLOCK RAM memory, distributed memory, Logic, REG & LUT memory, or allows the synthesizer to dynamically determine when synthesizing. Dynamically determining the type of device may result in an excessively long synthesis time and a poor synthesis result.

3.3 Dynamic Configuration

The dynamic configuration feature is enabled only for static configurations, and the generated FFT IP has dynamic configuration capabilities. The runtime parameters of all dynamic configuration items must be set before the FFT transform is started and at the appropriate time according to the specified signal. Dynamic configuration is done through the port signal.

3.3.1 Dynamic Configuration Transformation Direction

This feature works when the Dynamic Through Port in FFT MODE is enabled. When the FFT MODE setting is available, iset will go high, and the data on the ifft will be acquired on the next clock edge. Low level indicates forward conversion and high level indicates reverse conversion.

3.3.2 Dynamic Configuration Points

This feature works when Variable Points is enabled. When FFT points can be set, pset will become high level, and data on point will be collected at the next clock edge. It is an unsigned integer whose value is $\text{Log}_2 N$, and N must be the integral power of 2 between Minimum Points and Maximum Points. This configuration item is currently not supported.

3.3.3 Dynamic Configuration Data Reduction Ratio

This function works when the data reduction ratio option is selected as Dynamic Through Port. When the data reduction ratio setting is available, sfset will go high and the setting value of scal will be sampled in the next clock cycle. scal is an unsigned number. The sfact port has not been supported at present.

3.4 Handshake Agreement

The overall protocol is divided into four steps. The first step is to configure dynamic parameters (if any), the second is to enter data, the third is to calculate data, and the fourth is to read data.

3.4.1 Dynamic Parameters Configuration

Please refer to the description of the dynamic configuration section for dynamic parameter configuration according to the timing requirements. It should be noted that the dynamic parameter configuration may overlap with other steps in the time domain.

3.4.2 Start Input Data

Once everything is ready, you can initiate an FFT transformation by setting start high. After several cycles, sod goes high for one cycle, while ipd goes high and stays high for the entire data input phase, indicating that data is being input, and in addition, idx outputs the sequence label of the current clock sample. When a data input ends, eod goes high for one cycle while ipd goes low. At this point, one data entry is complete.

3.4.3 FFT Calculation Data

The FFT calculation process will start automatically after several cycles of data input, and the busy will become high, indicating that the inner core is calculating the FFT data, and the bus will go low after the calculation is completed.

3.4.4 Output Data Unloading

When FFT calculates several cycles, it automatically enters the data unloading stage. The soud will go high during the first unload data cycle for one cycle, opd will also go high and remain high during the entire unload of data. During the last cycle of data unloading, eoud will go high for one cycle and opd will also go low for the next cycle.

4 Signal Definition

Gowin FFT IP signal is defined as shown in Table 4-1.

Table 4-1 FFT IP Signal Definition

No.	Signal name	I/O	Bit width	Description
1	xn_re	I	8-36	The real part of the sequence to be converted
2	xn_im	I	8-36	The imaginary part of the sequence to be converted
3	xk_re	O	8-36	The real part of the converted sequence
4	xk_im	O	8-36	The imaginary part of the converted sequence
5	clk	I	1	Clock input
6	rst	I	1	System reset
7	idx	O	3-16	Indicates the position of the data sequence to be loaded on the next trigger edge when loading data, and indicates the location of the current output data sequence when unloading data.
8	start	I	1	Synchronous start signal, active high, at least one clock cycle, and only sampled when the core is idle, initiate a conversion.
9	sod	O	1	Time domain sequence starts signal, active high, indicating that the sample data will be input at the next trigger edge.
10	ipd	O	1	Data is being input, active high, indicating that input data is being sampled.
11	eod	O	1	Time domain sequence end signal, active high, indicating data input is complete.
12	busy	O	1	FFT inner core conversion indication,

No.	Signal name	I/O	Bit width	Description
				active high, indicating that the FFT inner core is undergoing transformation calculation.
13	soud	O	1	Frequency domain sequence start signal, active high, indicating that the first data is being unloaded.
14	opd	O	1	Data is being output, and active high, indicating that the data being output is valid.
15	eoud	O	1	Frequency domain sequence end signal, active high, indicating completion of data unloading.
FFT Mode selects Dynamic Through Port				
16	ifft	input	1	When ifft=1, IP completes IFFT function. When ifft=0, IP completes FFT function.
Scaling Mode selects Dynamic Through Port				
17	sfset	input	1	Sets reduction ratio enable, active-high.
18	sfact	input	4	This function not supported yet, and the input can be any value.
19	scal	input	2	Reduction ratio value, unsigned.

5 GUI Parameters

You can configure Gowin FFT parameters according to requirements. The parameters are as shown in Table 5-1.

Table 5-1 Gowin FFT Parameters

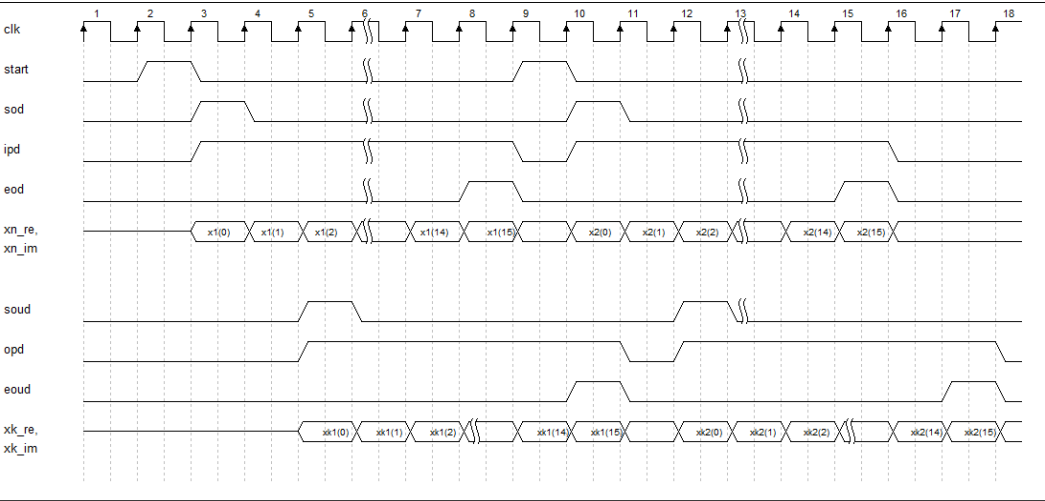
No.	Parameter	Description	Option
1	Number of Points	Supported points	8,16,32,64,128,256,512,1024, 2048,4096,8192,16384.
2	Architecture	FFT architecture	Currently only supports Low Resource
3	FFT Mode	FFT transform mode	Forward, Inverse, Dynamic Through Port.
4	Output Order	Output sequence	Natural, Bit-Reverse
5	Scaling Mode	Zoom mode	RS111, Dynamic Through Port, None.
6	Input Data Width	Input data bit width	8-36
7	Twiddle Factor Width	Rotation factor bit width	8-36
8	Output Data Width	Output data bit width	8-36
9	Precision Reduction Method	Mantissa processing mode	Truncation, Rounding.
10	Multiplier Type	Multiplier implementation type	DSP Block Based, LUT Based, Automatic.
11	Data Memory Type	Data storage type	EBR Memory, Distributed, REG&LUT, Automatic.
12	Twiddle Memory Type	Rotation factor storage type	EBR Memory, Distributed, Logic, Automatic.

6 Interface Timing

6.1 Data Protocol

The timing diagram in continuous data mode (16 points) is shown in Figure 6-1.

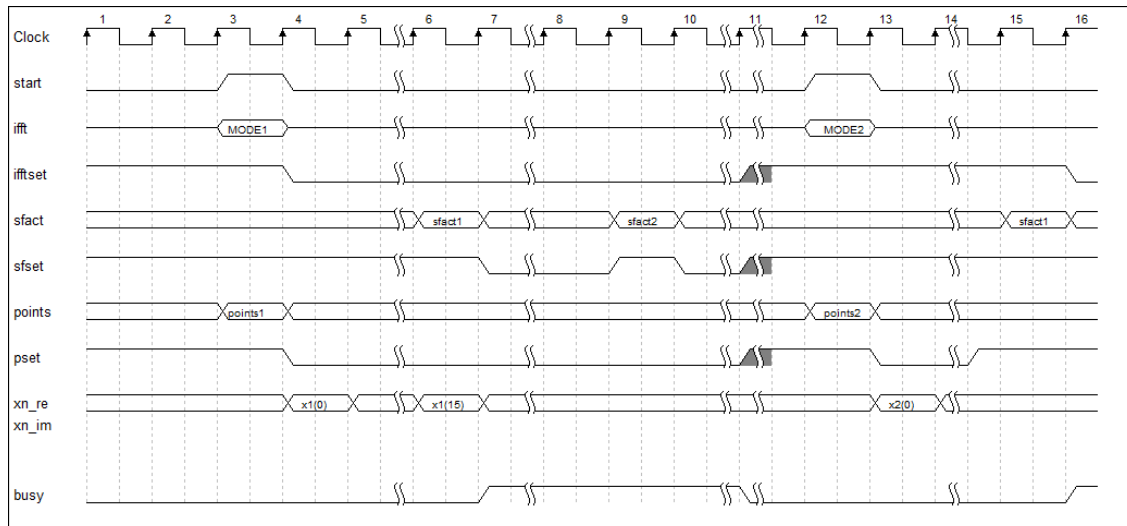
Figure 6-1 Point Data Protocol Timing Diagram



6.2 Handshake Agreement

The low resource control signal handshake protocol timing is shown in Figure 6-2.

Figure 6-2 Handshake Protocol Timing Diagram



7 Application

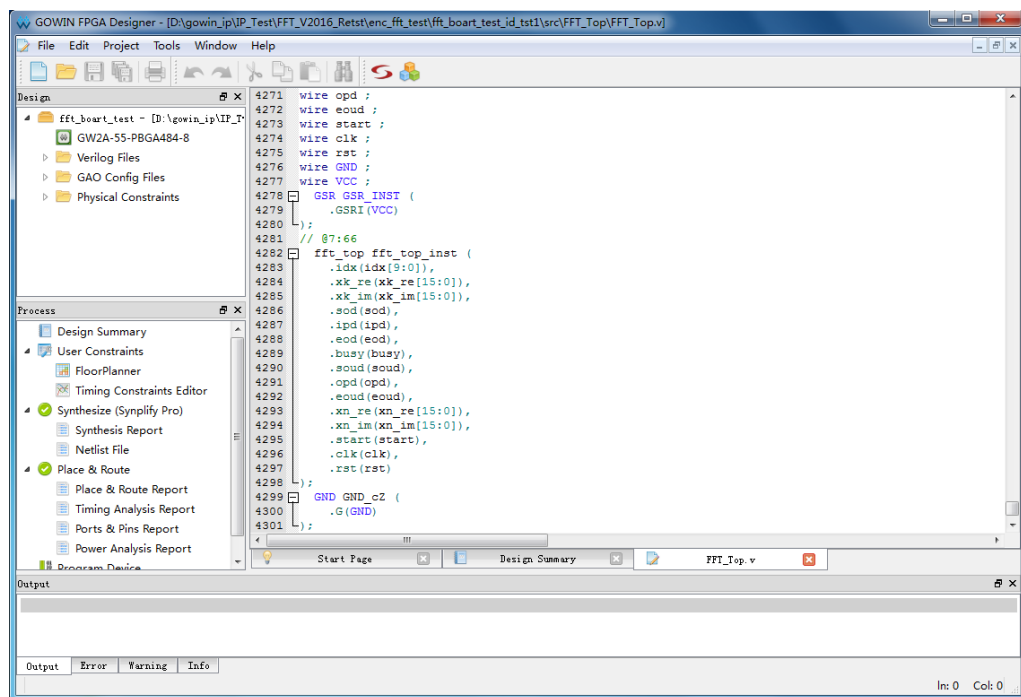
7.1 Open Project

Click "File> Open..." to open the "Open File" dialog box, select the required project file (*.gprj), and open the project, as shown in Figure 7-1.

Note!

There are three ways to open the project. For other open-projects, please refer to [SUG100](#), Gowin Software User Guide.

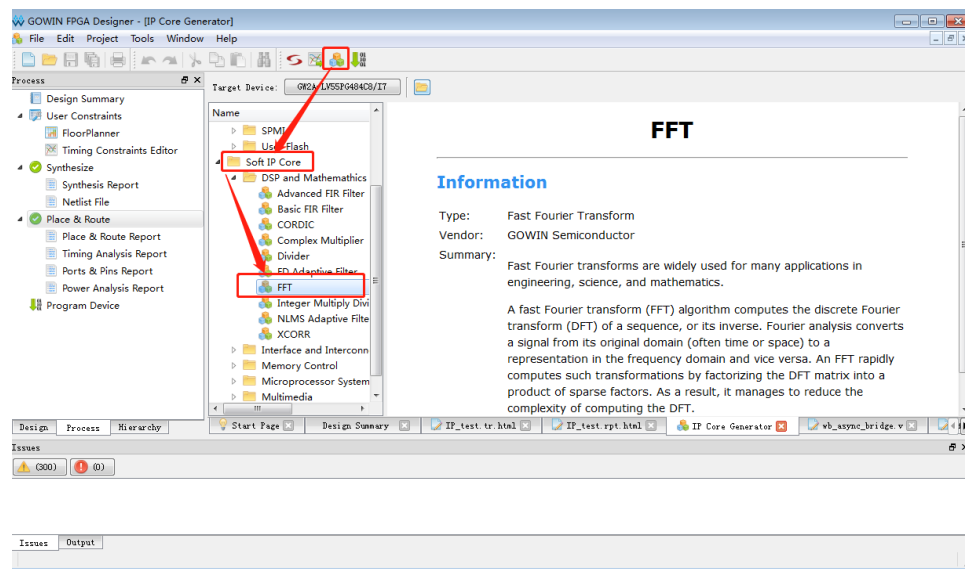
Figure 7-1 Open the Project



7.2 Call Gowin FFT IP

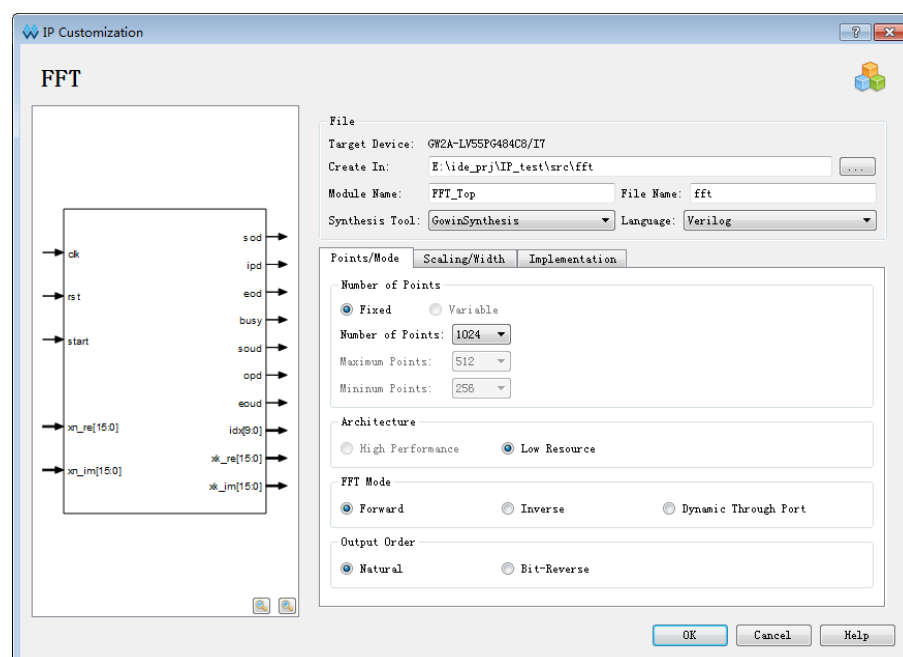
In the Gowin Software menu bar, click "Tool > IP Core Generator > Soft IP Core > DSP and Mathematics"; the interface shown in Figure 7-2 will pop up. This interface can also be opened according to the path shown in Figure 7-2.

Figure 7-2 IP Core Generator Interface



Select device, such as GOWIN2A-55-PBGA484; double-click on "FFT", and the interface shown in Figure 7-3 will pop up. Take the defaults and click "OK" to generate FFT_Top Module.

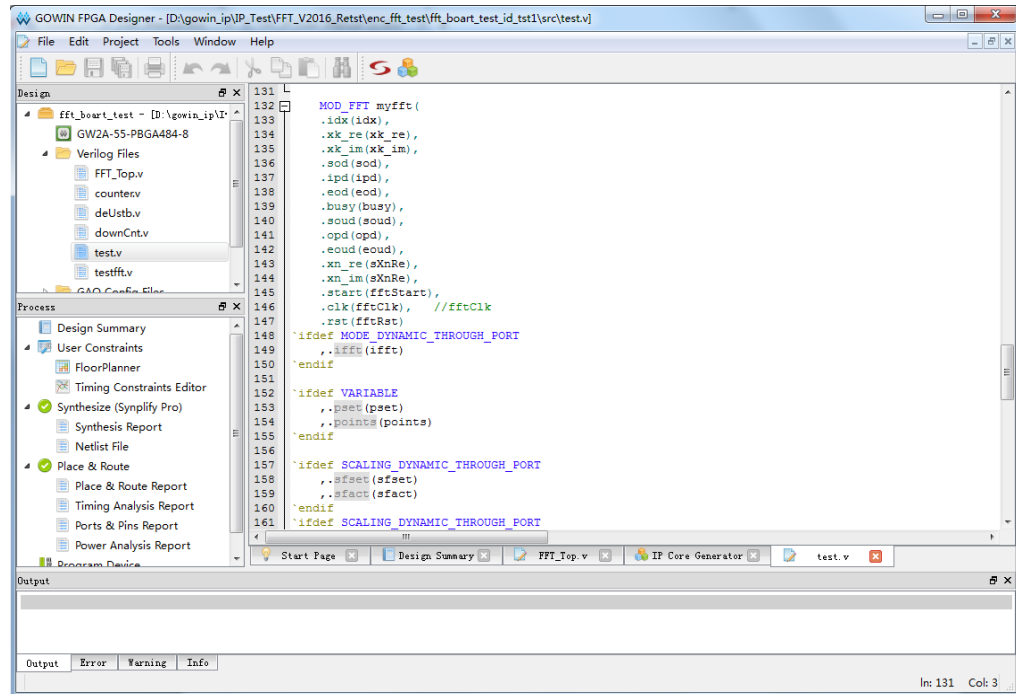
Figure 7-3 Gowin FFT IP Interface



7.3 Instantiate Gowin FFT IP

The FFT_Top is instantiated in the project, as shown in Figure 7-4.

Figure 7-4 Instantiate Gowin FFT IP



7.4 Generate Bitstream File

After making the necessary constraints, the bitstream file is generated after synthesis, placement and routing. Download the bitstream file to the development board or beta via the Gowin USB cable and observe the FFT transformation result via the test interface.

