



Gowin Basic FIR Filter User Guide

IPUG542-1.0E,2/25/2019

Copyright©2019 Guangdong Gowin Semiconductor Corporation. All Rights Reserved.

No part of this document may be reproduced or transmitted in any form or by any denotes, electronic, mechanical, photocopying, recording or otherwise, without the prior written consent of GOWINSEMI.

Disclaimer

GOWINSEMI[®], LittleBee[®], Arora[™], and the GOWINSEMI logos are trademarks of GOWINSEMI and are registered in China, the U.S. Patent and Trademark Office, and other countries. All other words and logos identified as trademarks or service marks are the property of their respective holders, as described at www.gowinsemi.com. GOWINSEMI assumes no liability and provides no warranty (either expressed or implied) and is not responsible for any damage incurred to your hardware, software, data, or property resulting from usage of the materials or intellectual property except as outlined in the GOWINSEMI Terms and Conditions of Sale. All information in this document should be treated as preliminary. GOWINSEMI may make changes to this document at any time without prior notice. Anyone relying on this documentation should contact GOWINSEMI for the current documentation and errata.

Revision History

Date	Version	Description
2/25/2019	1.0E	Initial version published.

Content

Content	i
List of Figures	iii
List of Tables	iv
1 About This Guide	1
1.1 Purpose	1
1.2 Supported Products	1
1.3 Related Documents	1
1.4 Terminology and Abbreviation	2
1.5 Support and Feedback	2
2 Overview	3
2.1 Basic FIR Filter IP Introduction	3
2.2 Key Features	3
2.3 Max. Frequency	4
2.4 Resource Utilization	4
3 Port Description	5
4 GUI Parameters	6
4.1 Overview	6
5 Principle	7
5.1 Algorithm Introduction	7
5.2 Gowin Basic FIR Filter IP Implementation	7
6 Timing Description	9
6.1 Coefficient Input Timing	9
6.2 Data Input Timing	10
6.3 Data Output Timing	11
6.4 ini	11
6.5 Input Interval	11
7 Configuration and Call	12

8 Reference Design	15
---------------------------------	-----------

List of Figures

Figure 3-1 Basic FIR FilterInterface Diagram	5
Figure 5-1 Gowin Basic FIR Filter IP Implementation Diagram	7
Figure 6-1 Coefficient Input Timing	9
Figure 6-2 Data Input Timing	10
Figure 6-3 Data Output Timing.....	11
Figure 7-1 Open Basic FIR Filter IP Core	12
Figure 7-2 Basic FIR Filter IP Core Configuration Interface	13
Figure 7-3 Help Document.....	14

List of Tables

Table 1-1 Abbreviations and Terminologies	2
Table 2-1 Basic FIR Filter IP	3
Table 2-2 Basic FIR Filter Resource Utilization	4
Table 3-1 Basic FIR Filter I/O Ports List.....	5
Table 4-1 GUI Paramrters	6

1 About This Guide

1.1 Purpose

Gowin Basic FIR Filter user guide provides an introduction of the functions, signals, ports, timing, configuration call, and reference design, etc. The guide helps users to quickly learn the feature and usage of Gowin Basic FIR Filter IP.

1.2 Supported Products

The information presented in this guide applies to the following products:

1. GW1N series of FPGA products: GW1N-2, GW1N-2B, GW1N-4, GW1N-4B, GW1N-6, GW1N-9
2. GW1NR series of FPGA Products
3. GW2A series of FPGA Products
4. GW2AR series of FPGA Products

1.3 Related Documents

The user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. GW1N series FPGA Products Data Sheet
2. GW1NR series FPGA Products Data Sheet
3. GW2A series FPGA Products Data Sheet
4. GW2AR series FPGA Products Data Sheet
5. Gowin YunYuan Software User Guide

1.4 Terminology and Abbreviation

The terminology and abbreviations used in this manual are as shown in Table 1-1 below.

Table 1-1 Abbreviations and Terminologies

Terminology and Abbreviations	Full Name
FPGA	Field Programmable Gate Array
FIR	Finite Impulse Response
IP	Intellectual Property
DSP	Digital Signal Processing
BSRAM	Block SRAM

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

+Tel: +86 755 8262 0391

2Overview

2.1 Basic FIR Filter IP Introduction

Gowin Basic FIR Filter IP is a basic structure FIR Filter which is realized by multiplication and cumulative calculation. It is simple to control timing by this IP. The order can be configured to a wide range. The user can configure the length of the internal multiplication array according to the DSP resource. When the tapsize is large, BSRAM is used to store the data and coefficient, which saves a lot of logical resources.

Table 2-1 Basic FIR Filter IP

Basic FIR Filter IP	
IP Core Application	
Supported Devices	● GW1N Series: GW1N-2, GW1N-2B, GW1N-4, GW1N-4B, GW1N-6, GW1N-9 ● GW1NR Series ● GW2A Series ● GW2A Series
Logic Resource	Please refer to Table 2-2.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	Synplify_Pro
Application Software	GoWinYunYuan

2.2 Key Features

- Input data bit width is configurable
- Coefficient bit width is configurable
- Tapsize supporting 16-2048 is configurable

- The multiplier array length is configurable

2.3 Max. Frequency

The maximum frequency of Basic FIR Filter IP is mainly determined by the speed grade of the devices, and it can reach 100M.

2.4 Resource Utilization

Basic FIR Filter is implemented by Verilog language. Due to different IP configuration, its resource utilization varies greatly accordingly. In addition, its performance and resource utilization may vary when the design is employed in different devices, or at different density, speed, or grade.

The following table shows the resource utilization of Basic FIR Filter IP under some typical configurations when the input data bit width and coefficient bit width are both selected 18bits.

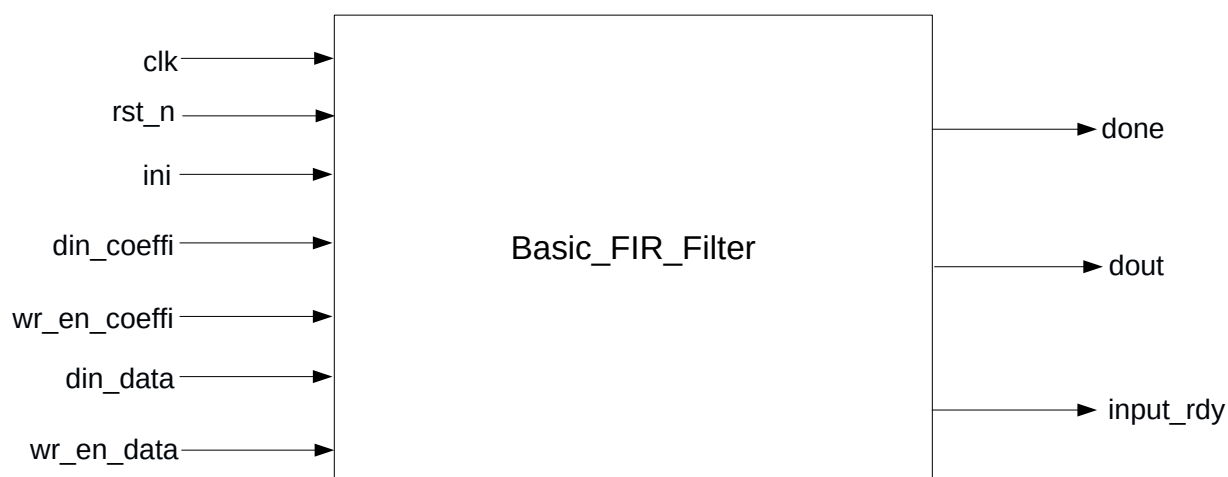
Table 2-2 Basic FIR Filter Resource Utilization

Device	Speed Level	Mult Array length	Tapsize	LOGICS	REGS	DSP Macros	BSRAMS
GW2A-55	C8/I7	2	32	327	395	1	0
			1024	337	373	1	4
		4	32	629	570	3	0
			1024	603	511	3	8
		8	32	1973	1254	6	0
			1024	1789	1107	6	16

3Port Description

I/O Ports diagram is shown in Figure 3-1.

Figure 3-1 Basic FIR Filter Interface Diagram



I/O ports list is shown in Table 3-1.

Table 3-1 Basic FIR Filter I/O Ports List

Signal	I/O	Data Width	Description
rst_n	Input	1	Reset signal, active - low
clk	Input	1	Clock signal
ini	Input	1	Initialization signal for zeroing data memory
wr_en_data	Input	1	Input data write enable signal
din_data	Input	12-24	Input data
wr_en_coeffi	Input	1	Input coefficient write enable signal
din_coeffi	Input	12-24	Input coefficient
dout	Output	54	Output signal, namely filtered result
done	Output	1	High level, output indication signal means the filter is completed, and the output is effective.
input_rdy	Output	1	Indicate that one calculation cycle is completed and data can be input again

4GUI Parameters

4.1 Overview

Basic FIR Filter provides relevant parameters for users to configure according to their actual requirements, as shown in Table 4-1.

Table 4-1 GUI Parameters

No.	Name	Options	Description
1	Mult Array Length	2/4/8	The multiplier array length
2	Tapsize	16-2048	The tapsize must be an integer multiple of the multiplier array length
3	Input data width	12-24	Input data width
4	Input coefficient width	12-24	Input coefficient width

5 Principle

5.1 Algorithm Introduction

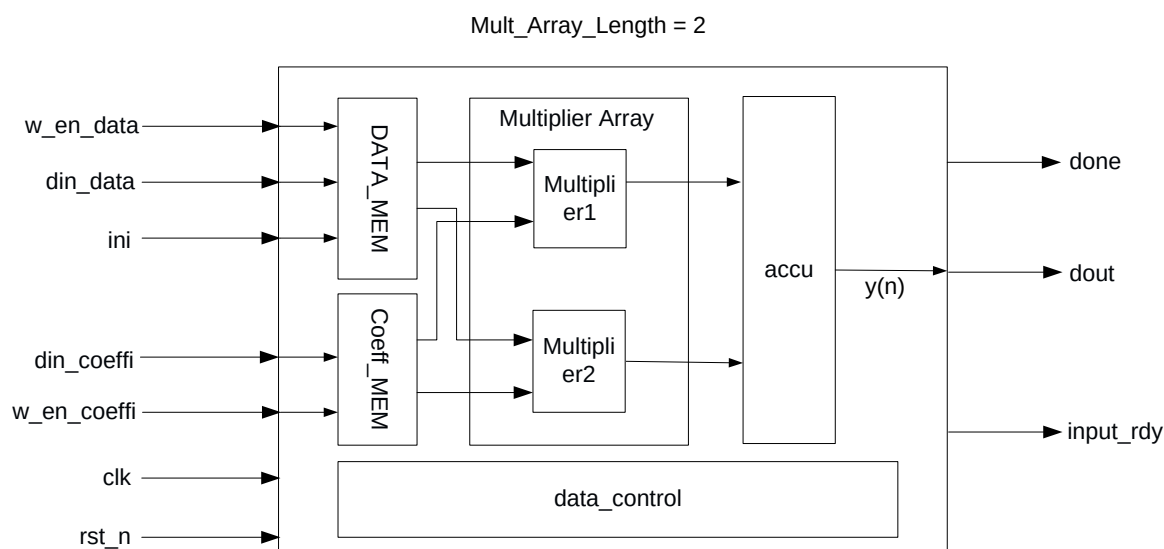
Basic FIR(Finite Impulse Response) Filter, its calculation formula is as follows:

$$y[n] = b_0x[n] + b_1x[n - 1] + \cdots + b_Nx[n - N]$$

$$= \sum_{i=0}^N b_i \cdot x[n - i]$$

5.2 Gowin Basic FIR Filter IP Implementation

Figure 5-1 Gowin Basic FIR Filter IP Implementation Diagram



When Mult Array Length = 2, the basic FIR Filter IP implementation diagram is shown in Figure 5-1. The internal is mainly composed of DATA_MEM, Coeff_MEM, Multiplier Array, accumulator and data control. When the multiplier array length is configured differently, the number of

multiplier in the multiplier array will change accordingly. When tapsize is large, DATA_MEM and Coeff_MEM are implemented by BSRAM, which can save other logic resources to a great extent.

6Timing Description

Basic FIR Filter IP input timing control signals are listed as follows:

1. rst_n: Reset signal, active - low
2. ini: Initialization signal for zeroing data memory
3. wr_en_data: Input data write enable signal
4. wr_en_coeffi: Input coefficient write enable signal

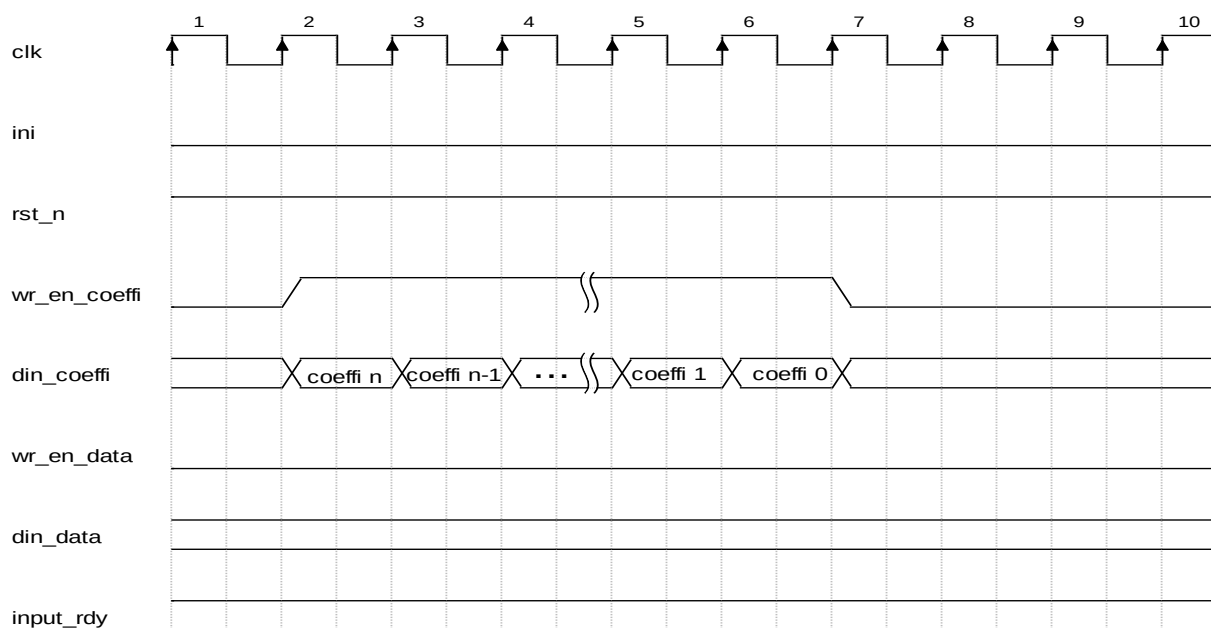
Note!

Do not do multiple timing controls at the same time, otherwise the calculation results will be wrong.

Each timing is described respectively in the below.

6.1 Coefficient Input Timing

Figure 6-1 Coefficient Input Timing



Coefficient input timing is shown in the Figure 6-1 above. The input coefficient write enable signal should be pulled up when inputting

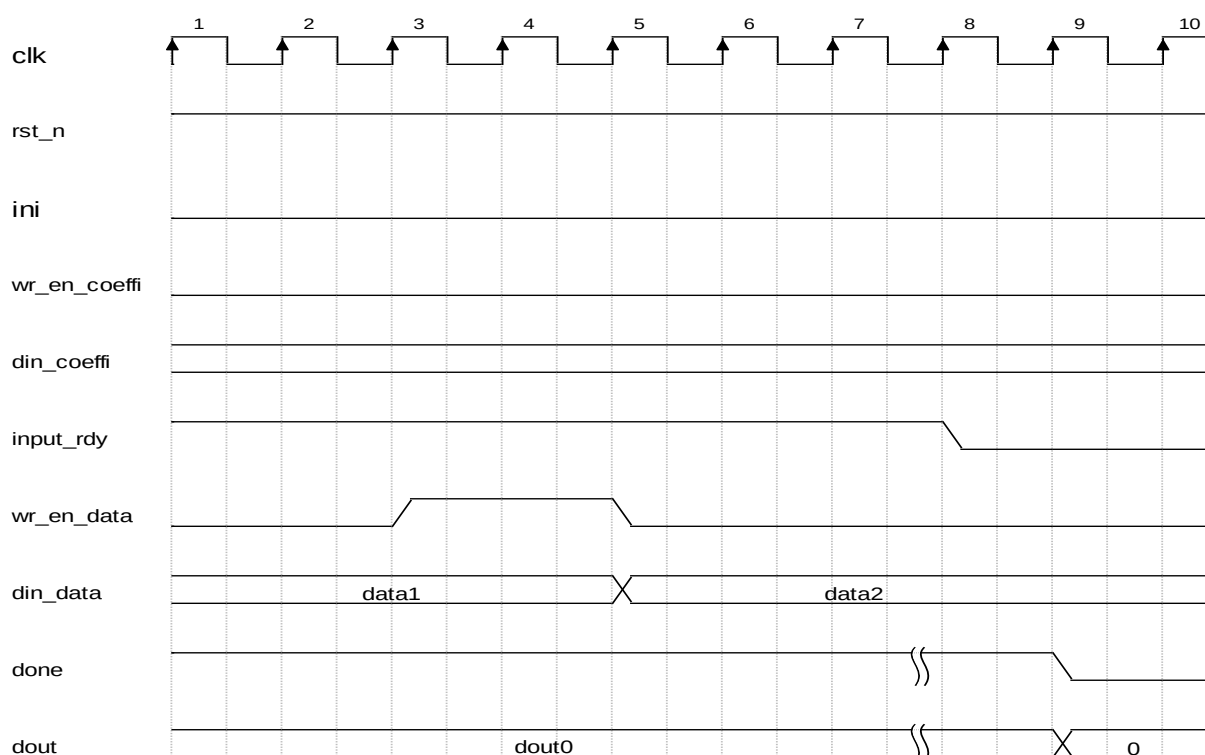
coefficient. When the rising edge of the clock arrives, if the input coefficient write enable signal is high level, then the coefficient will be written. The number of written coefficient should be the same as the number of IP configuration tapsize, if exceeded, the written coefficient before will be covered. It should be noted that if the filter is as follows:

$$y[n] = b_0x[n] + b_1x[n - 1] + \dots + b_Nx[n - N]$$

When inputting coefficient , it should be input in the order of $b_N, b_{N-1}, b_{N-2} \dots b_1, b_0$.

6.2 Data Input Timing

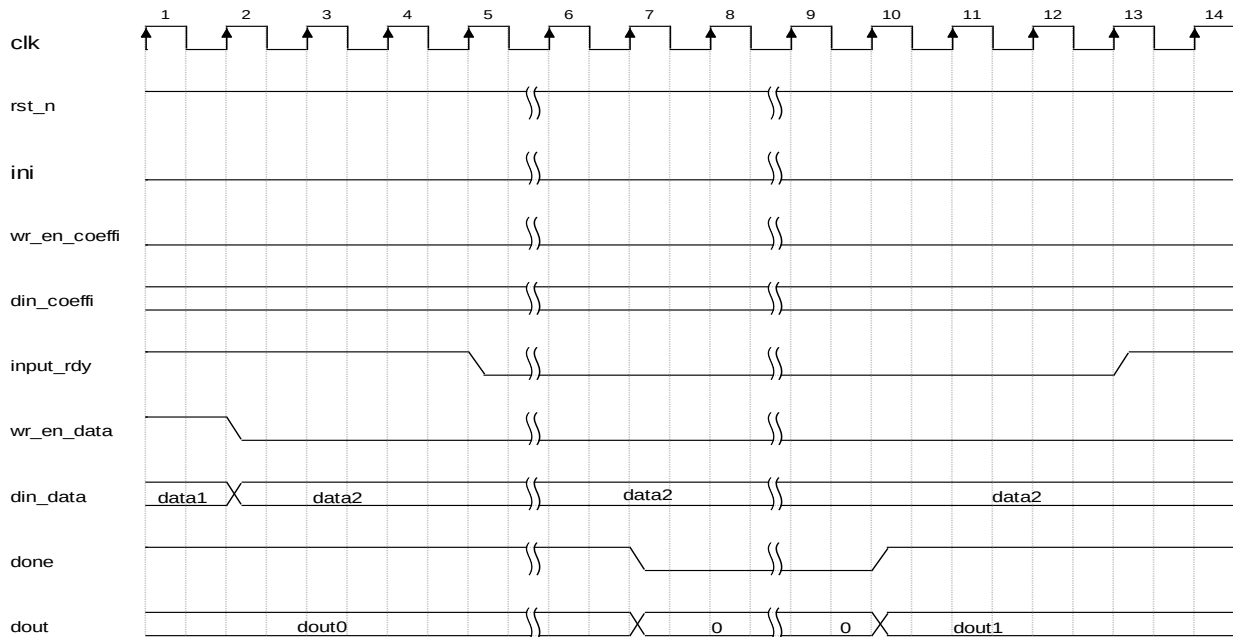
Figure 6-2 Data Input Timing



Data input timing is shown in the Figure 6-2. When input_rdy signal is high, it indicates that IP can input data. When it needs to input data, the wr_en_data signal is pulled up. Basic FIR Filter IP will input din_data at last high level of wr_en_data. (As shown in the Figure 6-2, when the fifth clock rises, IP will input data1 and calculate. After three cycles of delay, the input_rdy signal is set to zero. Please wait for the input_rdy signal to be pulled up again then input next data.

6.3 Data Output Timing

Figure 6-3 Data Output Timing



Data output timing is shown in the Figure 6-3. After finishing one data write, the done and dout signal will be set to zero after several cycles of delay. Wait for a while , the done signal will be pulled up to indicate that the calculation has been completed, and dout will output. After three more clock cycles of delay, the input_rdy signal will be pulled up to indicate that the data can be input again.

6.4 ini

Ini signal is used to initialize the input data in the data memory. The number of initialization clock cycle should be greater than the number of filter tapsize.

6.5 Input Interval

Because Basic FIR Filter IP involves a lot of mathematical calculation, the calculation process takes much time. If a calculation is not completed (input_rdy signal is not pullded up), the new data is input again, and an unexpected error will occur. In the use process, data can be input after input_rdy is pulled up or at a fixed rate. The following provides a simple algorithm for data input interval as a reference.

Assuming that the input clk frequency is f_c HZ, the tap size is n , the multiplier array length is m , and $f_{w\max}$ means the maximum frequency of input data, then:

$$f_{w\max} = \frac{f_c}{n/m + 50}$$

7 Configuration and Call

Start "IP Core Generator" from the "Tools" menu in the Gowin YunYuan software, complete the call and configure Basic FIR Filter.

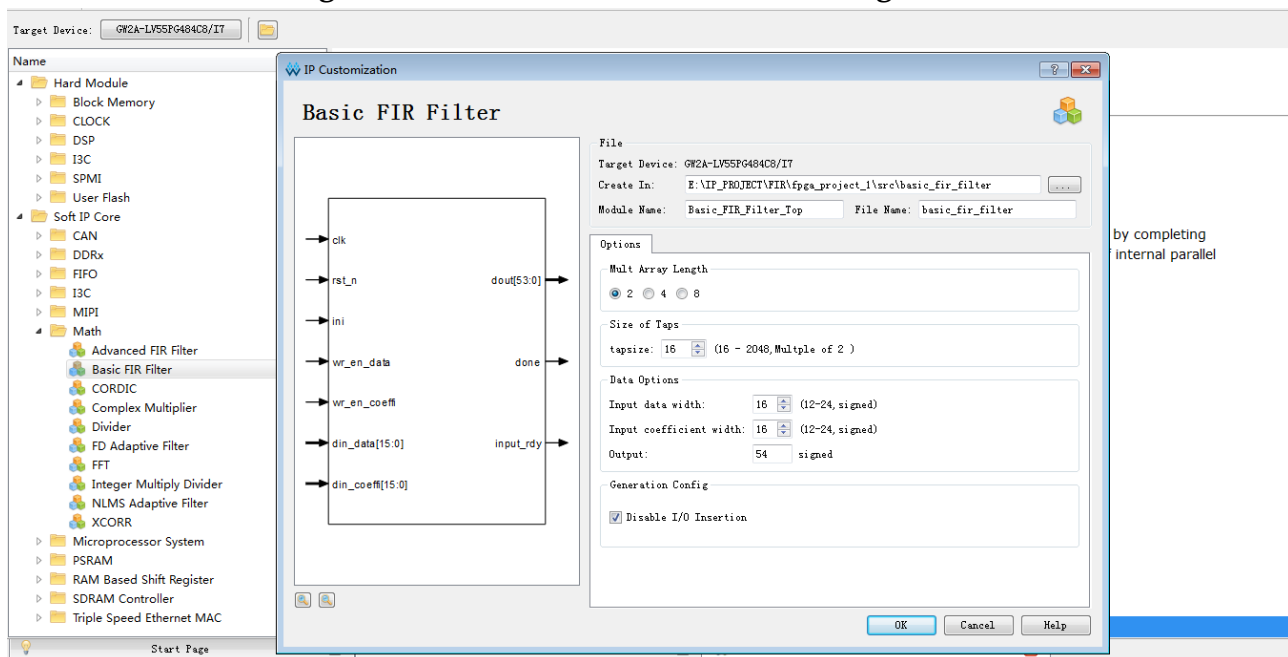
1. Open IP Core Generator
After creating a project, you can click the "Tools" tab in the upper left. Click on the IP Core Generator option via the drop-down list to open GOWIN IP Core Generator tool.
2. Open Basic FIR Filter IP Core.
Basic FIR Filter IP Core is located in Math of Soft IP Core. Double click to open the Basic FIR Filter IP Core, as shown in Figure 7-1.

Figure 7-1 Open Basic FIR Filter IP Core



3. Basic FIR Filter ConfigurationInterface.
Basic FIR Filter configuration interface is shown in Figure 7-2.

Figure 7-2 Basic FIR Filter IP Core Configuration Interface



Basic FIR Filter IP core interface diagram is on the left of the configuration interface; On the right are some configurable options to do the following:

- a). Basic FIR Filter can be configured to generate the file name by modifying the File Name.
- b). The generated Basic FIR Filter top-level module name can be configured by modifying the Module Name.
- c). The user can configure Mult Array Length, filter tapsize, Input data bitwidth, Input data width and Input coefficient width (the output data is 54 bits) by Options.
4. Open Help document

You can click the Help button in the lower left of Figure 7-2 to check the English brief introduction of each option so as to facilitate users to quickly complete the configuration of IP core, as shown in Figure 7-3.

Figure 7-3 Help Document

Basic FIR Filter**Information**

Type:	Basic FIR Filter
Vendor:	GOWIN Semiconductor
Summary:	The Gowin Basic FIR Filter IP is a basic version of FIR filter. It realizes FIR filter function by completing multiplication and accumulation operation. Mult Array Length determines the number of internal parallel multipliers, and the larger the number, the faster the calculation speed.

Options

Option	Description
Mult Array Length	
Mult Array Length	Select the number of internal parallel multipliers.
Size of Taps	
Size of Taps	Specify the number of taps in Basic FIR Filter.
Data Options	
Input data width	Specify the input data width.
Input coefficient width	Specify the input coefficient data width.

8Reference Design

Please refer to the related test cases in RefDesign.

