



Gowin Fixed Point Divider

User Guide

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Revision

Date	Revision	Description
2018/12/11	1.0E	Initial version released.
2020/02/10	1.1E	• Supported devices updated; • IP name updated; • Some figures updated; • Data interpretation added.

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1 About This Manual

1.1 Purpose

Gowin Fixed Point Divider includes features, port descriptions, timing descriptions, call and configuration , reference designs, etc, mainly used to help users quickly understand the features and usage of Gowin Fixed Point Divider IP.

1.2 Supported Products

The information described in this guide applies to Gowin all devices.

1.3 Related Documents

The latest user guides are available on the Gowin website:

www.gowinsemi.com

1.4 Terms and Abbreviations

The abbreviations and terminology used in this manual are as shown in Table 1-1 below.

Table 1-1 Terms and Abbreviations

Abbreviation and Terminology	Meaning
IP	Intellectual Property

1.5 Technical Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

URL: www.gowinsemi.com

E-mail: support@gowinsemi.com

Tel: +86 755 8262 0391

2 Overview

2.1 Introduction

Gowin Fixed Point Divider IP is available for all Gowin FPGA chips and is designed to perform division operations.

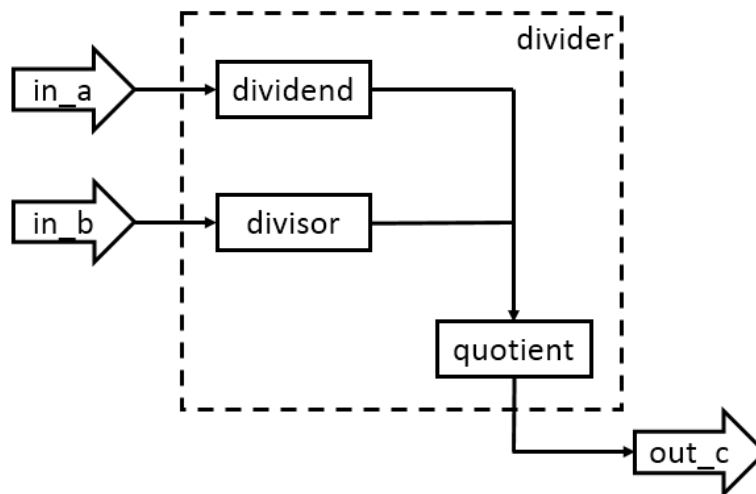
Table 2-1 Gowin Fixed Point Divider IP

Gowin Fixed Point IP	
IP core application	
Chip supported	Gowin all devices
Logical resource	See Table 3-1
Delivery document	
Design documents	Verilog (Encrypted)
Reference design	Verilog
TestBench	Verilog
Test design flow	
Integrated software	Synplify_Pro
Application	Gowin YunYuan

2.2 Introduction to Gowin Fixed Point Divider

The Fixed Point Divider IP is designed to implement a signed decimal division module with fixed point. The structure diagram is shown in Figure 2-1.

Figure 2-1 Gowin Fixed Point Divider Structure Diagram



3 Features and Performance

3.1 Main Features

- Can achieve division of signed decimals with fixed pointed;
- Can configure input data width;
- Can configure decimal precision;
- The output latency is related to the parameters configuration (data width and decimal precision).

3.2 Data Interpretation

The input and output data of Gowin Fixed Point Divider IP (dividend, divisor, quotient) is calculated using fixed point source code; It is different from the commonly used complement to represent data, so special attention should be paid when the data is negative.

The interpretation of input and output data depends on bit width (Q) and decimal precision (N). Take the inputs of Q=32 and N=3 as an example:

Dividend =32 'd 12345, divisor =32' d 345, Quotient_out =32'd 286; The actual value of the quotient is $\text{quotient_out}/(2^N)=35.75$.

Because of the precision, it is normal for the calculation result of IP to have some error with the accurate result.

Note:

- The source code means that the highest bit is the sign bit, and the remaining bits represent the value.
- Source code example (3bit data; source code -> decimal value):
- 101 - > 1; 001 - > + 1; 111 - > - 3; 011 - > + 3.
- When the input or output is negative, the highest bit is regarded as the sign bit, and the interpretation of the remaining bits is the same as the one in the above example.

3.3 Maximum Frequency

The maximum frequency of Gowin Fixed Point Divider IP is primarily determined by the speed grade of the devices.

3.4 Latency

The output latency of Gowin Fixed Point Divider IP is primarily determined by the configuration parameters (data width and decimal precision).

3.5 Resource Utilization

Implement Gowin Fixed Point Divider IP in Verilog. Performance and resource utilization may vary depending on the density, speed, and grade of the device being used.

Taking Gowin GW2A-55 series FPGA as an example, the resource utilization of Gowin Fixed Point Divider IP is shown in Table 3-1. For application verification on other Gowin FPGAs, please pay attention to the post-release information.

Table 3-1 The Resource Utilization of Gowin Fixed Point Divider

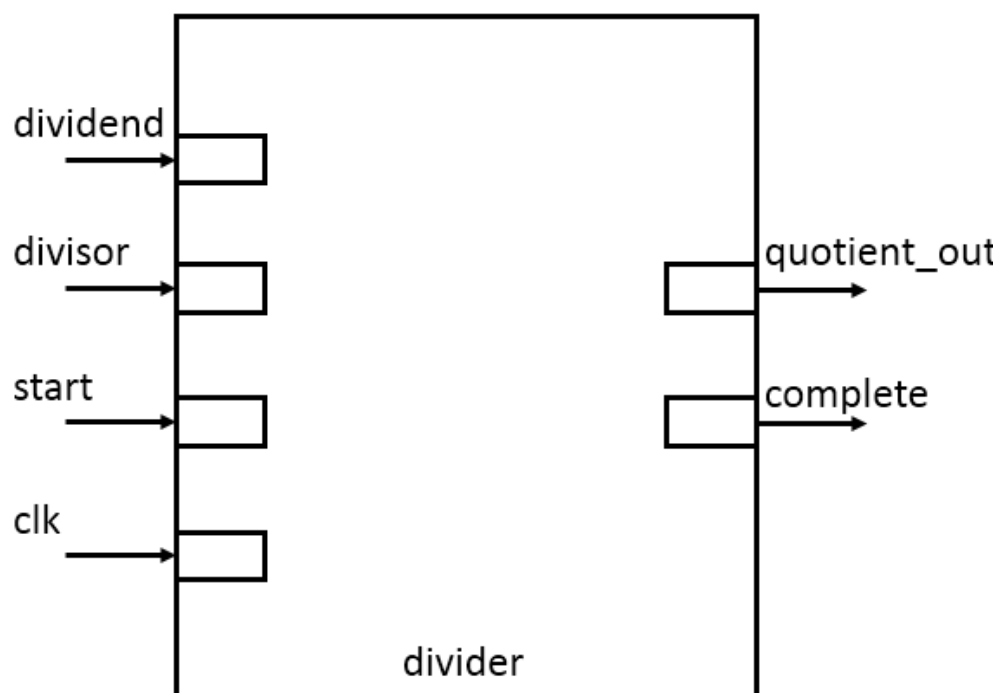
Device series	Speed grade	Device name	Resource utilization	Remarks
GW2A-55	C8/I7	Logic	318	Input data width=32 Decimal precision=3
		Register	132	

4 Functional Description

4.1 Structure and Function

Gowin Fixed Point Divider IP can realize the division of signed decimals with fixed point. When generating the module, users can configure the data width and decimal precision according to their needs. Its structural block diagram is shown in Figure 4-1.

Figure 4-1 Interface Implementation of Gowin Fixed Point Divider



The user enters the dividend and divisor, and the IP calculates quotient_out.

4.2 Data Bit Width Setting

The data bit width can be configured through the GUI interface. The divider supports signed bit data. The most significant bit is the sign bit, the maximum bit width is 32 bits, and the minimum bit width is 8 bits.

4.3 Decimal Precision Setting

The decimal precision can be configured through the GUI interface. By changing the demical precision, decimals of different precision can be achieved.

5 Port Description

5.1 Port

Details on the I/O ports of Gowin Fixed Point Divider are shown in Table 5-1. Please refer to Figure 4-1 for the interface block diagram.

Table 5-1 List of I/O Ports for Gowin Fixed Point Divider

Signal	Direction	Description
dividend	Input	Input dividend
divisor	Input	Input divisor
start	Input	Start signal
clk	Input	Clock signal
quotient_out	Output	Output quotient_out
complete	Output	End signal

Note!

Dividend, divisor and quotient are represented by source code. Special attention should be paid when the data is negative.

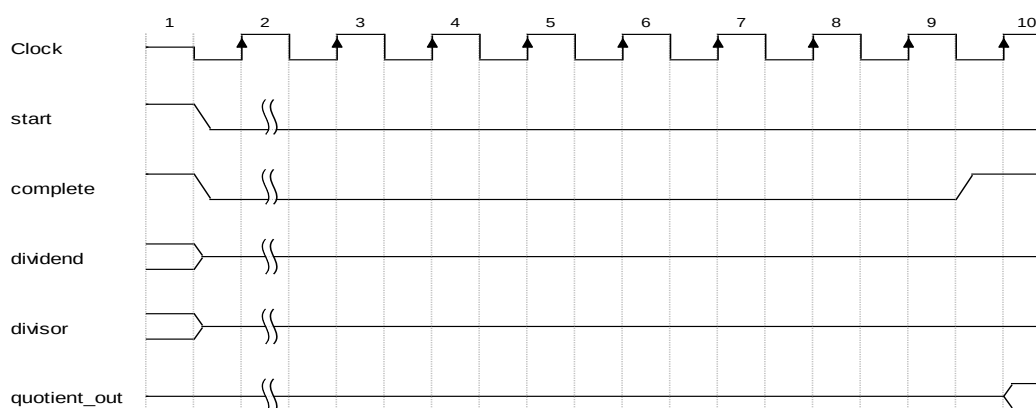
6 Timing Description

This chapter is intended to introduce the timing of Gowin Fixed Point Divider IP.

6.1 Gowin Fixed Point Divider Signal Timing

Signal timing diagram of Gowin Fixed Point Divider IP is shown in Figure 6-1.

Figure 6-1 Signal Timing of Gowin Fixed Point Divider IP



As shown in Figure 6-1, when the start and complete signals both are at high level, the dividend and divisor are input and start to run, after a certain period (the latency period is determined by the configuration parameter, data width, decimal precision), the output quotient_out is got when the rising edge of the complete signal .

7 GUI Configuration

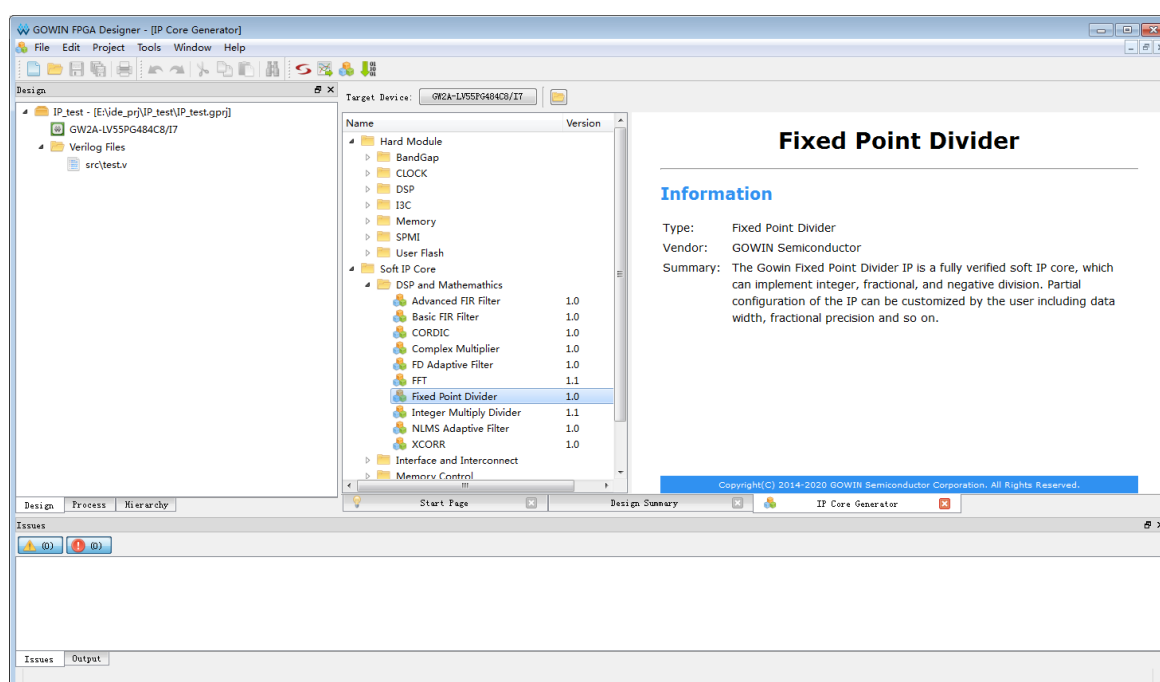
In the "Tools" of Gowin YunYuan software interface, you can start the IP Core Generator tool, call and configure Gowin Fixed Point Divider IP.

7.1 Configuration

The Gowin Fixed Point Divider IP configuration is as follows.

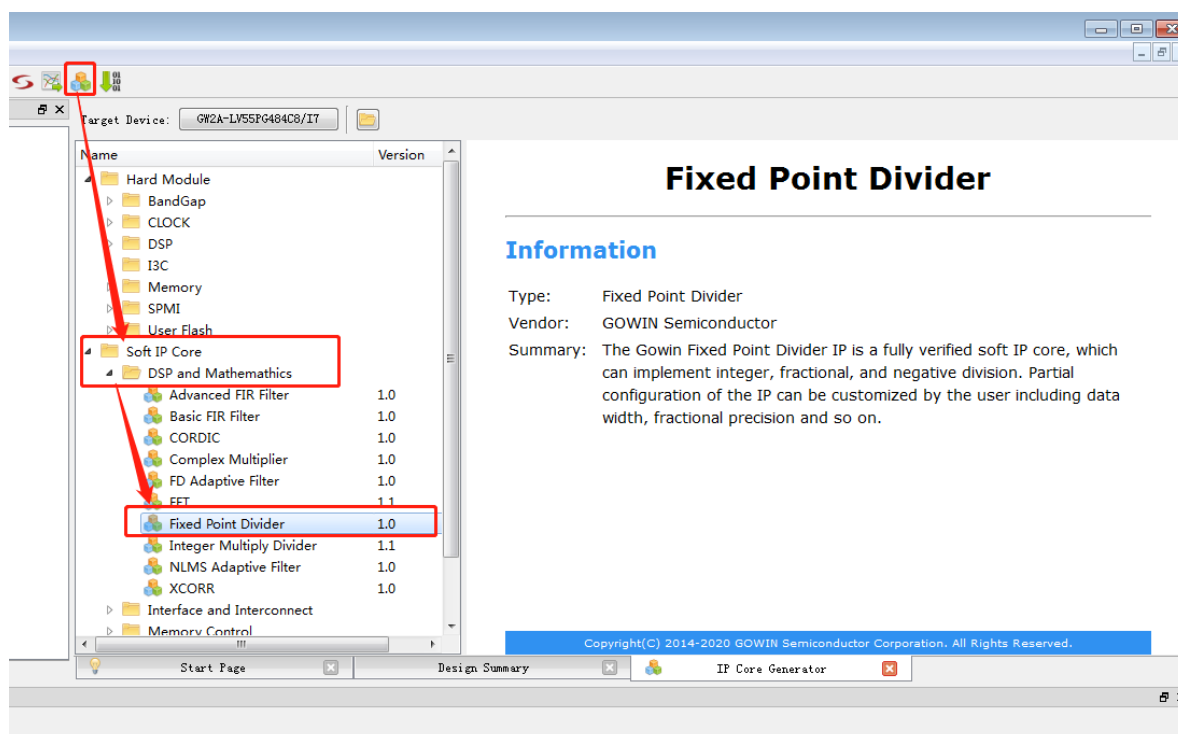
1. Create a project, as shown in Figure 7-1.

Figure 7-1 Project Interface



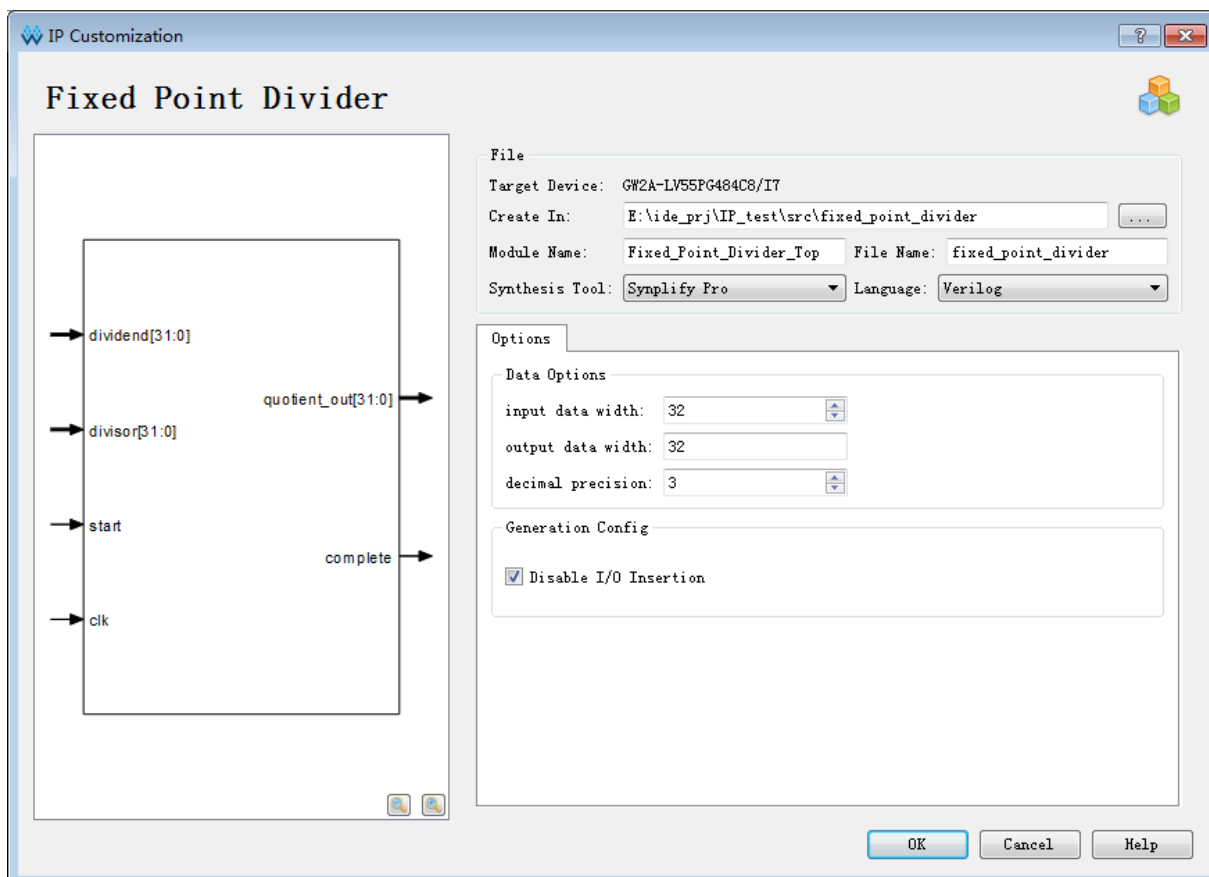
2. After creating a project, click "Tools > IP Core Generator > Soft IP Core > DSP and Mathematics > Fixed Point Divider" to call Gowin Fixed Point Divider IP, as shown in Figure 7-2.

Figure 7-2 Open Gowin Fixed Point Divider IP



3. Open Gowin Fixed Point Divider IP interface as shown in Figure 7-3.

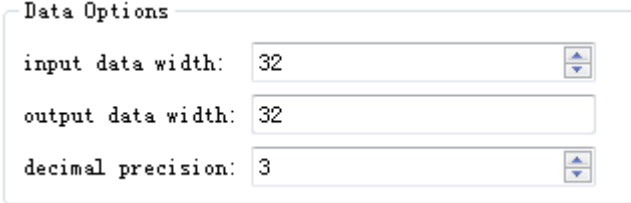
Figure 7-3 Gowin Fixed Point Divider IP Interface



7.2 Configuring Gowin Fixed Point Divider IP

Open the GUI configuration interface, as shown in Figure7-4.

Figure7-4 Parameter Configuration Interface



Data Options	
input data width:	32
output data width:	32
decimal precision:	3

Here you can configure the data width and decimal precision. The range of input data width is 8-32. The size of output data width is the same as the input data width and changes accordingly. The range of demical precision is from 1 to input data width-2.

Users can configure the above parameters according to their own needs and click "ok" to generate Gowin Fixed Point Divider IP.

8 Reference Design

Refer to the relevant test case in ref_design.

9 Document Delivery

Gowin Fixed Point Divider IP includes two parts: document and reference design.

9.1 Document

The folder mainly contains the user guide PDF document.

Table 9-1 List of Documents

Name	Description
Gowin Fixed Point Divider IP User Guide	Gowin Fixed Point Divider IP User Guide

