



Gowin DDS IP

Release Note

RN941-1.2E,08/19/2022

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Revision History

Date	Version	Description
06/30/2020	1.0E	Initial version published.
08/19/2022	1.2E	● Triangle and square waveforms added. ● Taylor correction added.

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1 About This Guide

This release includes Gowin DDS IP reference design and user guide.

Gowin DDS IP and reference design are available at www.gowinsemi.com. The reference design has been configured with parameters that can be used for testing after simulation, synthesis, placement and routing.

2 Overview

Gowin DDS IP is a direct digital frequency synthesizer that enables direct synthesis of the desired waveform from the phase concepts. The IP can be configured with multiple independent time-division multiplexing channel, output data bit width, frequency, and phase offset, thus providing flexibility and ease of use.

Table 2-1 Gowin DDS IP Overview

Gowin DDS IP	
IP Core Application	
Supported Devices	● GW1N series of FPGA products: GW1N-9 ● GW1NR series of FPGA products: GW1NR-9 ● GW2A series of FPGA products ● GW2AR series of FPGA products ● GW1NZ series of FPGA Products
Delivered Doc.	
Design File	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.6Beta and above)

3 Documents

This software release contains Gowin DDS IP documents as listed below:

Documents	Usage
Gowin DDS IP User Guide. pdf	PDF
Gowin DDS IP Release Note.pdf	PDF

4 IP Support

Since the requirements of user design and the highest frequency are different, the reference design does not include associated FPGA specific location (.cst) and timing constraints (.sdc) documents, which user can determine on his own as required.

For the customized IP design and support, please contact Gowin sales and support line.

Website: www.gowinsemi.com

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