Gowin USB 2.0 SoftPHY IP

User Guide

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Revision History

Date	Version	Description
07/23/2021	1.0E	Initial version published.
08/13/2021	1.1E	The property configuration of IO ports modified.
10/12/2021	1.2E	Chapter 2.3 "Using 5V Host Supply to Power USB Device Solution" added.
12/23/2021	1.3E	● The configuration method of peripheral circuit modified. ● IO configuration constraints added.
03/29/2022	1.4E	The description of resource utilization added.
06/20/2022	1.5E	● The speed grade modified. ● The description of pin constraints updated.
07/20/2022	1.5.1E	A note added in Table 2-1.

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1 About This Guide

1.1 Purpose

The purpose of Gowin USB 2.0 SoftPHY IP User Guide is to help you learn the features and usage of this IP by providing the descriptions of functions, signals, and interface configuration.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at: www.gowinsemi.com.

- DS100, GW1N series of FPGA Products Data Sheet
- DS117, GW1NR series of FPGA Products Data Sheet
- DS821, GW1NS series of FPGA Products Data Sheet
- DS871, GW1NSE series of FPGA Products Data Sheet
- DS861, GW1NSR series of FPGA Products Data Sheet
- DS891, GW1NRF series of FPGA Products Data Sheet
- DS881, GW1NSER series of Bluetooth FPGA Products Data Sheet
- DS102, GW2A series of FPGA Products Data Sheet
- DS226, GW2AR series of FPGA Products Data Sheet
- DS961, GW2ANR series of FPGA Products Data Sheet
- DS976, GW2AN-55 Data Sheet
- DS971, GW2AN-18X & 9X Data Sheet
- SUG100, Gowin Software User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
IP	Intellectual Property
USB	Universal Serial Bus
UTMI	USB 2.0 Transceiver Macrocell Interface
HS	High Speed
FS	Full Speed
LS	Low Speed
NRZI	Non Return Zero Inverted

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Introduction

2.1 Overview

Gowin USB 2.0 SoftPHY IP is a USB physical layer transceiver that can support data reception and transmission at high speed (480Mbps), full speed (12Mbps), and low speed (1.5Mbps).

Table 2-1 Gowin USB 2.0 SoftPHY IP Overview

Gowin USB 2.0 SoftPHY IP	
IP Core Application	
Supported Devices[1]	● Arora family ● LittleBee family, excluding GW1N-1/GW1N-1S/GW1NZ-1/GW1N-1P5 devices..
Logic Resource	Please refer to Table 2-3 and Table 2-4.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.8.05 and above)

Note!

[1] Only part number with speed grade C7 and above support USB 2.0 SoftPHY IP

2.2 Features

The features of GowinUSB 2.0 SoftPHY IP include:

- Supports HS (480 Mbps), FS (12 Mbps), and LS (1.5 Mbps).
- Supports data serial and parallel conversion.
- Supports bit stuffer and unstuffer.
- Supports NRZI encoder and decoder.
- Supports UTMI interface.

2.3 Using 5V Host Supply to Power USB Device Solution

Many solutions may to provide power to a USB device using the 5V provided over the cable from the Host without providing a separate power supply. To support cable powered USB device use cases, designers must be careful to ensure the total PCB BOM of the device does not exceed the current limitations of the USB Host as well as voltage drops over the cable.

The USB v2.0 specification, sections 7.1.2 and 7.3.2 provides information on current and voltage drop requirements expected to be supplied by a USB Host. If the total PCB BOM cannot meet the current and minimum voltage requirements of the specified host, the board can be powered with a separate power supply.

Table 2-2 DC Electrical Characteristics

Parameter	Symbol	Condition	Min.	Max.	Unit
Supply voltage					
High-power Port	V_{BUS}	Note 2, Section 7.2.1	4.75	5.25	V
Low-power Port	V_{BUS}	Note 2, Section 7.2.1	4.40	5.25	V
Supply Current					
High-power Hub Port (out)	I_{CCPRT}	Section 7.2.1	500		mA
Low-power Hub Port (out)	I_{CCUPT}	Section 7.2.1	100		mA
High-Power Function (in)	I_{CCHPF}	Section 7.2.1		500	mA
Low-power Function (in)	I_{CCLPF}	Section 7.2.1		100	mA
Unconfigured Function/Hub (in)	I_{CCINIT}	Section 7.2.1.4		100	mA
Suspended High-power	I_{CCSH}	Note 15, Section		2.5	mA

Device		7.2.3			
Suspended Low-power Device	I_{CCSL}	Section 7.2.3		500	μA

2.4 Resource Utilization

Gowin USB 2.0 SoftPHY IP can be implemented by Verilog. Its resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Taking Gowin GW1NSR-4 and GW2AR-18 series of FPGA ptoducts as an instance, the resource utilization is as shown in Table 2-3 and Table 2-4.

Table 2-3 Resource Utilization (I)

Device	Speed Grade	Resource	Utilization	Notes
GW1NSR-4	C7/I6	LUT	384	-
		REG	1109	
		ALU	13	
		BSRAM	1	
		SSRAM	0	
		IO	7	

Table 2-4 Resource Utilization (Ⅱ)

Device	Speed Grade	Resource	Utilization	Notes
GW2AR-18	C7/I6	LUT	384	-
		REG	1109	
		ALU	13	
		BSRAM	1	
		SSRAM	4	
		IO	7	

Note!

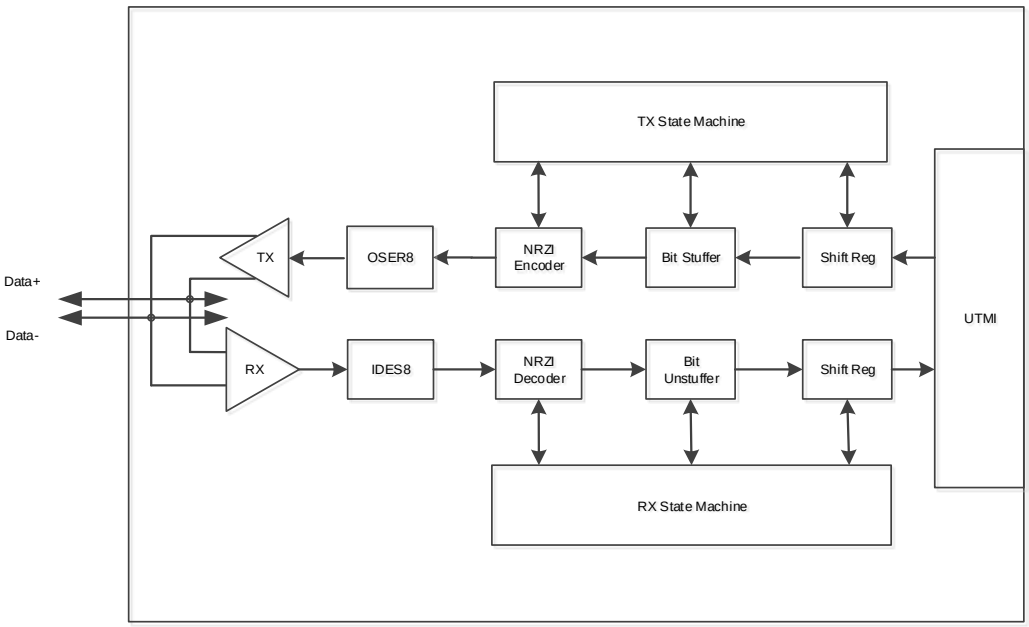
GW2A series and GW1NSR-4 can choose the chip with speed grade C6/I5; for other part numbers, please choose the chip with speed grade C7/I6.

3 Functional Description

3.1 USB 2.0 SoftPHY Block Diagram

In the RX, after USB serial data goes through IDES8, NRZI decoder, bit unstuffer, shift Reg modules in turn, USB RX data is received, and then the data transmits to the upper module through UTMI interface. In the TX, after receiving the data transmitted by UTMI and then going through shift Reg, bit stuffer, NRZI encoder to generate the serial TX data stream, which then is sent to the USB interface via OSER8.

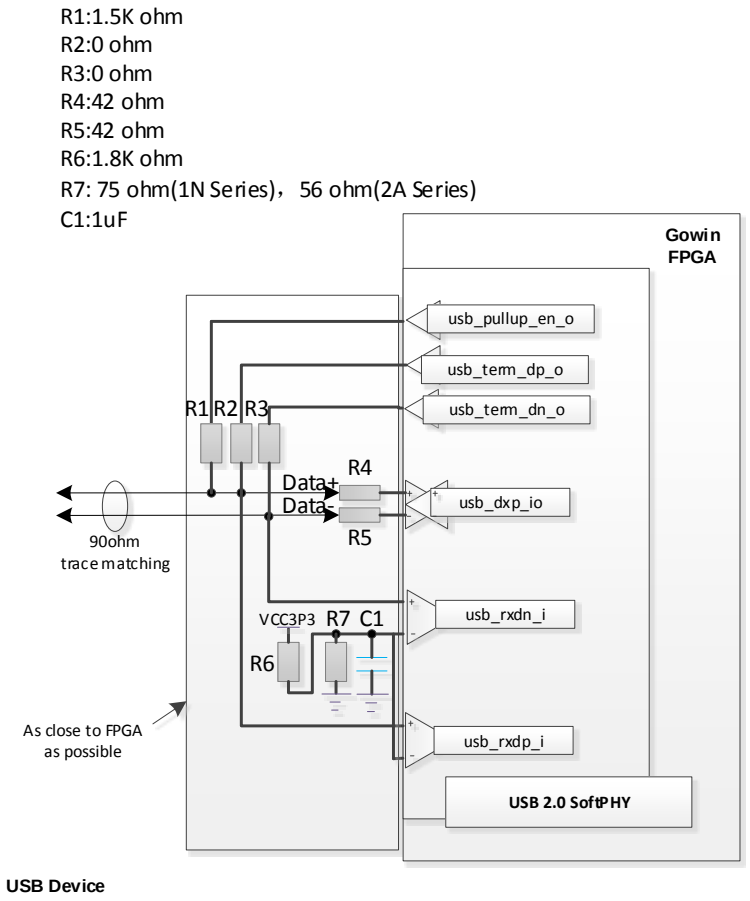
Figure 3-1 USB 2.0 SoftPHY Block Diagram



3.2 USB 2.0 SoftPHY External Circuit Connection

USB 2.0 SoftPHY supports high speed mode (480Mbps) . When the USB 2.0 SoftPHY is used as a USB slave device, the external circuit connection is as follows.

Figure 3-2 USB Slave Device Interface Implementation



Note!

1. You can see the followings for the IO port attribute constraints of GW2A series of FPGA.
   - usb_dxp_io: IO_TYPE= LVCMOS33D PULL_MODE= NONE DRIVE=4;
   - usb_term_dn_o: IO_TYPE=LVCMOS33 PULL_MODE= NONE DRIVE=8;
   - usb_term_dp_o: IO_TYPE=LVCMOS33 PULL_MODE=NONE DRIVE=8;
   - usb_pullup_en_o: IO_TYPE=LVCMOS33 PULL_MODE=NONE DRIVE=8;
   - usb_rxdn_i: IO_TYPE=LVDS25 PULL_MODE=NONE;
   - usb_rxdp_i: IO_TYPE=LVDS25 PULL_MODE=NONE.

2. You can see the followings for the IO port attribute constraints of GW1N series of FPGA.
   - usb_dxp_io: IO_TYPE= LVCMOS33D PULL_MODE= NONE DRIVE=8;
   - usb_term_dn_o: IO_TYPE=LVCMOS33 PULL_MODE= NONE DRIVE=16;
   - usb_term_dp_o: IO_TYPE=LVCMOS33 PULL_MODE= NONE DRIVE=16;
   - usb_pullup_en_o: IO_TYPE=LVCMOS33 PULL_MODE= NONE DRIVE=8;
   - usb_rxdn_i: IO_TYPE=LVDS25 PULL_MODE=NONE;
   - usb_rxdp_i: IO_TYPE=LVDS25 PULL_MODE=NONE.
3. All signals related to the USB interface on the FPGA are recommended to be placed in one Bank, using adjacent assignment, and powering the I/O Bank at 3.3V
4. It is required that the adjacent differential pair pins in the same Bank where the usb_dxp_io differential pair is located exist and are not used. Taking GW1NSR-4 as an example, Figure 3-3 shows the GW1NSR-4 Pinout. If the usb_dxp_io differential pair is located at G5, H5 (i.e. IOR11A/IOR11B) in the diagram, it will cause the project to report an error when implementing synthesis and placement with Gowin Software, as the adjacent differential pair pins IOR10A/IOR10B do not exist. If usb_dxp_io differential pair is located at G6/H6 (i.e. IOR13A/IOR13B), the project will synthesize and place successfully with Gowin Software, as the adjacent differential pair pins IOR12A/IOR12B exists.

Figure 3-3 GW1NSR-4 Pinout

GW1NSR Series of FPGA Products
GW1NSR-4 Pinout
Pin List

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	X16	MG64P
IOB13A	I/O	3		True_of_IOB13B	NONE	NONE	
IOB13B	I/O	3		Comp_of_IOB13A	NONE	NONE	
IOB14A	I/O	3		True_of_IOB14B	NONE	NONE	
IOB14B	I/O	3		Comp_of_IOB14A	NONE	NONE	
IOB15A	I/O	3		True_of_IOB15B	NONE	NONE	
IOB15B	I/O	3		Comp_of_IOB15A	NONE	NONE	
IOB16A/GCLKT_5	I/O	3	GCLKT_5	True_of_IOB16B	NONE	NONE	
IOB16B/GCLKC_5	I/O	3	GCLKC_5	Comp_of_IOB16A	NONE	NONE	
IOB22A/GCLKT_4	I/O	3	GCLKT_4	True_of_IOB22B	NONE	NONE	
IOB22B/GCLKC_4	I/O	3	GCLKC_4	Comp_of_IOB22A	NONE	NONE	
IOB23A	I/O	3		True_of_IOB23B	NONE	NONE	
IOB23B	I/O	3		Comp_of_IOB23A	NONE	NONE	
IOB24A	I/O	3		True_of_IOB24B	NONE	NONE	
IOB24B	I/O	3		Comp_of_IOB24A	NONE	NONE	
IOB25A	I/O	3		True_of_IOB25B	NONE	NONE	
IOB25B	I/O	3		Comp_of_IOB25A	NONE	NONE	
IOB29A	I/O	3		True_of_IOB29B	NONE	NONE	
IOB29B	I/O	3		Comp_of_IOB29A	NONE	NONE	
IOB4A	I/O	3		True_of_IOB4B	NONE	NONE	
IOB4B	I/O	3		Comp_of_IOB4A	NONE	NONE	
IOB5A	I/O	3		True_of_IOB5B	NONE	NONE	
IOB5B	I/O	3		Comp_of_IOB5A	NONE	NONE	
IOB6A	I/O	3		True_of_IOB6B	NONE	NONE	
IOB6B	I/O	3		Comp_of_IOB6A	NONE	NONE	
IOB7A	I/O	3		True_of_IOB7B	NONE	NONE	
IOB7B	I/O	3		Comp_of_IOB7A	NONE	NONE	
IOR11A/GCLKT_3	I/O	2	GCLKT_3	True_of_IOR11B	TRUE	x16	G5
IOR11B/GCLKC_3	I/O	2	GCLKC_3	Comp_of_IOR11A	TRUE	NONE	H5
IOR12A	I/O	2		True_of_IOR12B	NONE	NONE	
IOR12B	I/O	2		Comp_of_IOR12A	NONE	NONE	
IOR13A	I/O	2		True_of_IOR13B	TRUE	x16	G6
IOR13B	I/O	2		Comp_of_IOR13A	TRUE	NONE	H6
IOR14A	I/O	2		True_of_IOR14B	NONE	NONE	

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4 Signal Description

A description of Gowin USB 2.0 SoftPHY IP signals is as shown in Table 4-1.

Table 4-1 Signal Description

No.	Signal Name	I/O	Data Width	Description
1	clk_i	I	1	Input clock signal (60MHz)
2	fclk_i	I	1	Input clock signal (480MHz)
3	rst_i	I	1	Asynchronous reset signal resets the state machine inside of PHY.
4	pll_locked_i	I	1	pll lock signal generating fclk_i
5	utmi_data_out_i	I	8	Data input, 8-bit parallel data transmit bus.
6	utmi_txvalid_i	I	1	Transmit data valid indicator, active-high.
7	utmi_txready_o	O	1	Transmit data ready signal, indicating that PHY can receive the data to be transmitted from the controller end.
8	utmi_data_in_o	O	8	Data output, 8-bit parallel data receive bus.
9	utmi_rxactive_o	O	1	Rx data active, indicating that PHY detects the SYNC signal and then starts receiving data.
10	utmi_rxvalid_o	O	1	Rx data valid, active-high.
11	utmi_rxerror_o	O	1	Receive data error, active high indicates receive error.

No.	Signal Name	I/O	Data Width	Description
12	utmi_linestate_o	O	2	Line status of receive end: DM DP 2'b00：SE0 2'b01："J" 2'b10："K" 2'b11：SE1
13	utmi_opmode_i	I	2	Operation mode selection signal: 2'b00: Normal 2'b01: No driver 2'b10: Disable bit stuffing and NRZI encoding 2'B11: Reserved
14	utmi_xcvrselect_i	I	2	Transfer mode selection signal: 2'b00: HS Transfer 2'b01: FS Transfer 2'b10: LS Transfer 2'B11: Reserved
15	utmi_termselect_i	I	1	Termination Selection: 1' b0: HS termination enable 1' b1: FS / LS termination enable
16	usb_dxp_io	I/O	1	USB data signal Data+
17	usb_dxn_io	I/O	1	USB data signal Data-
18	usb_rxdp_i	I	1	USB data signal Data+ input
19	usb_rxdn_i	I	1	USB data signal Data- input
20	usb_pullup_en_o	O	1	1.5K resistor pull-up control on USB data signal Data+
21	usb_term_dp_o	I/O	1	Termination resistor control of USB data signal Data+
22	usb_term_dn_o	I/O	1	Termination resistor control of USB data signal Data-

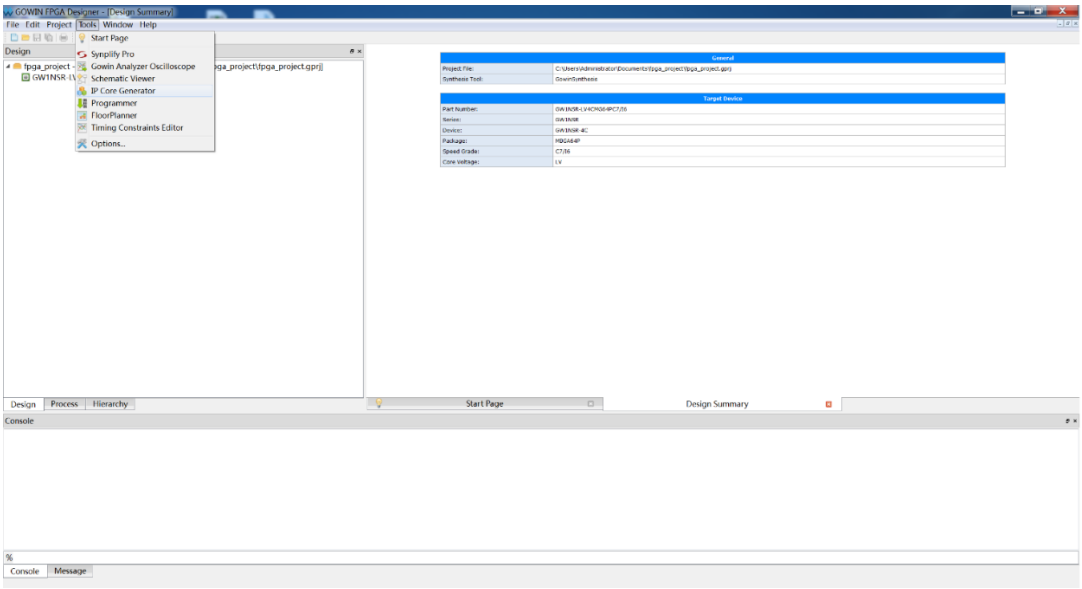
5 Interface Configuration

Selecting "Tools > IP Core Generator" in Gowin Software, you call and configure USB 2.0 SoftPHY.

1. Open IP Core Generator

After creating the project, you can click the "Tools" tab in the upper left, select and open the IP Core Generator via the drop-down list, as shown in Figure 5-1.

Figure 5-1 IP Core Generator



2. Open USB 2.0 SoftPHY IP Core

Select "Soft IP Core > Interface and Interconnect > USB 2.0 IP", as shown in Figure 5-2. Double-click to open the configuration interface.

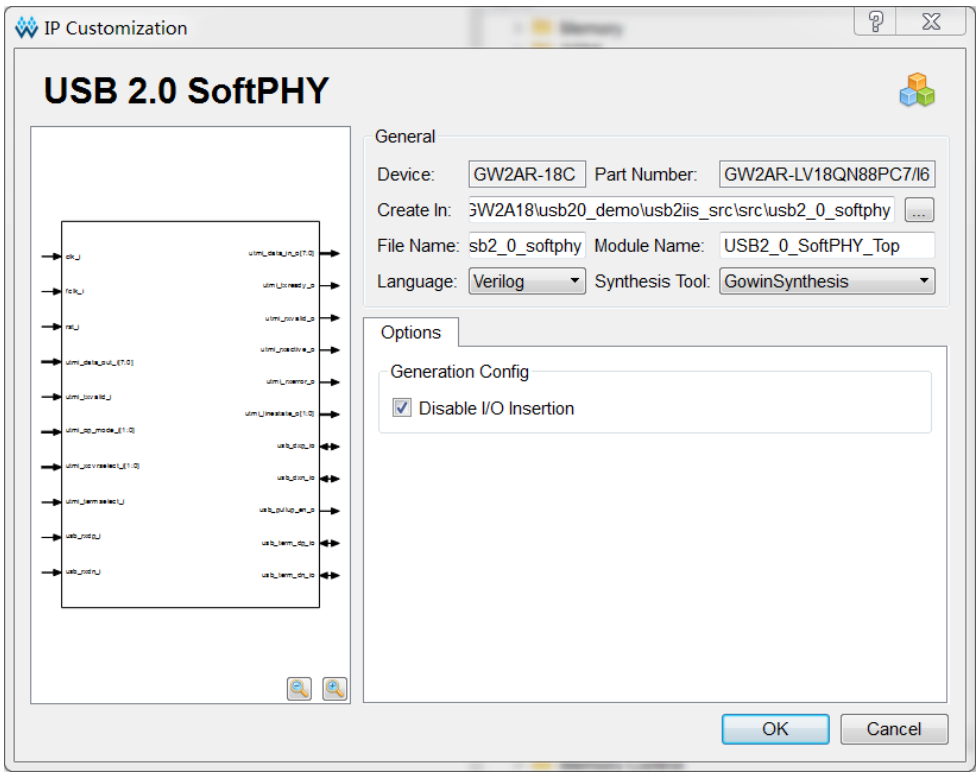
Figure 5-2 Open USB 2.0 SoftPHY IP Core

3. USB 2.0 SoftPHY IP Core Configuration Interface

Figure 5-3 shows the USB 2.0 SoftPHY IP core configuration interface. The ports diagram is on the left of the configuration interface. Options are on the right.

- You can configure the file name in File Name.
- You can configure the top module name in Module Name.

Figure 5-3 USB 2.0 SoftPHY IP Configuration Interface

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