Gowin USB 1.1 SoftPHY IP

User Guide

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Revision History

Date	Version	Description
01/06/2021	1.0E	Initial version published.
04/09/2021	1.1E	Chapter 3 Functional Description modified.
09/02/2022	1.2E	● The description of resource utilization added. ● Clock parameter configuration modified.
11/16/2023	1.2.1E	The descriptions of Figure 3-3 USB Slave Device Interface Implementation and Figure 3-4 USB Slave Device Interface Implementation updated.

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1 About This Guide

1.1 Purpose

The purpose of Gowin USB 1.1 SoftPHY IP User Guide is to help you learn the features and usage of Gowin USB 1.1 SoftPHY IP by providing descriptions of signals, functions and interface configuration.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- DS100, GW1N series of FPGA Products Data Sheet
- DS117, GW1NR series of FPGA Products Data Sheet
- DS891, GW1NRF series of FPGA Products Data Sheet
- DS821, GW1NS series of FPGA Products Data Sheet
- DS871, GW1NSE series of FPGA Products Data Sheet
- DS881, GW1NSER series of FPGA Products Data Sheet
- DS861, GW1NSR series of FPGA Products Data Sheet
- DS102, GW2A series of FPGA Products Data Sheet
- DS226, GW2AR series of FPGA Products Data Sheet
- SUG100, Gowin Software User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FS	Full Speed
HS	High Speed
IP	Intellectual Property
LS	Low Speed
USB	General Serial Bus
UTMI	USB 2.0 Transceiver Macrocell Interface

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Introduction

2.1 Overview

Gowin USB 1.1 SoftPHY IP is a USB physical layer transceiver that can support data receiving and transmitting at full speed (12 Mbps) or low speed (1.5 Mbps).

2.2 Features

The features of USB 1.1 SoftPHY IP include:

- Supports Full Speed Mode (12 Mbps) and Low Speed Mode (1.5 Mbps)
- Supports data serial and parallel conversion
- Supports bit stuffing and extraction
- Supports NRZI encoding and decoding
- Supports UTMI interface

2.3 Resource Utilization

Gowin USB 1.1 SoftPHY IP can be implemented by Verilog language. Its resource utilization may vary when the design is employed in different devices, or at different densities, speed grades. Taking Gowin GW1N-2 series of products for an instance, the resource utilization of USB 1.1 SoftPHY is shown in Table 2-1.

Table 2-1 Resource Utilization

Device Series	Speed Grade	Name	Resource Utilization	Note
GW1N-2	-5	LUT	133	–
		REG	47	

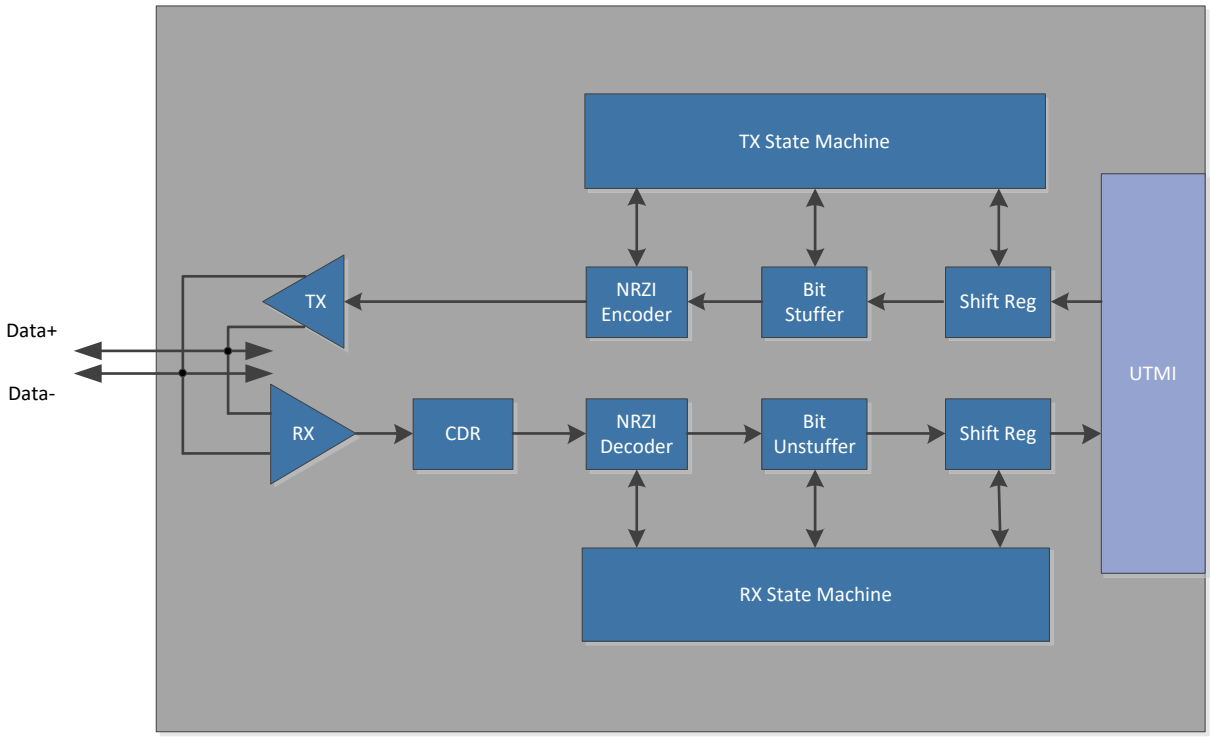
Device Series	Speed Grade	Name	Resource Utilization	Note
		ALU	0	
		BSRAM	0	
		IO	2	

3 Functional Description

3.1 USB 1.1 SoftPHY

In the RX direction, after USB serial data goes through the modules including CDR, NRZI decoding, bit extraction, data shifting, the realized USB RX data is received, and the received data is sent to the upper module through the UTMI interface. In the TX direction, after receiving the transmit data, the USB serial data goes through the modules including data shifting, bit filling, NRZI encoding to generate the serial TX data stream.

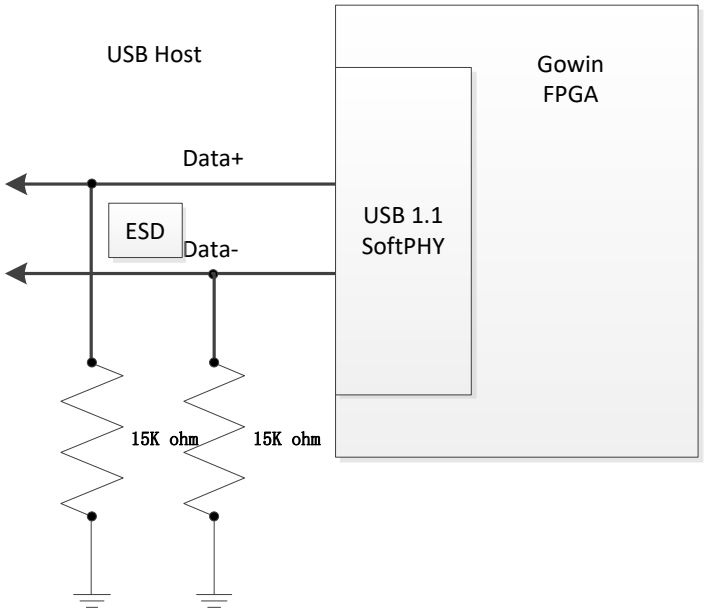
Figure 3-1 SoftPHY Block Diagram



USB 1.1 SoftPHY supports Full Speed Mode (12Mbps) and Low Speed

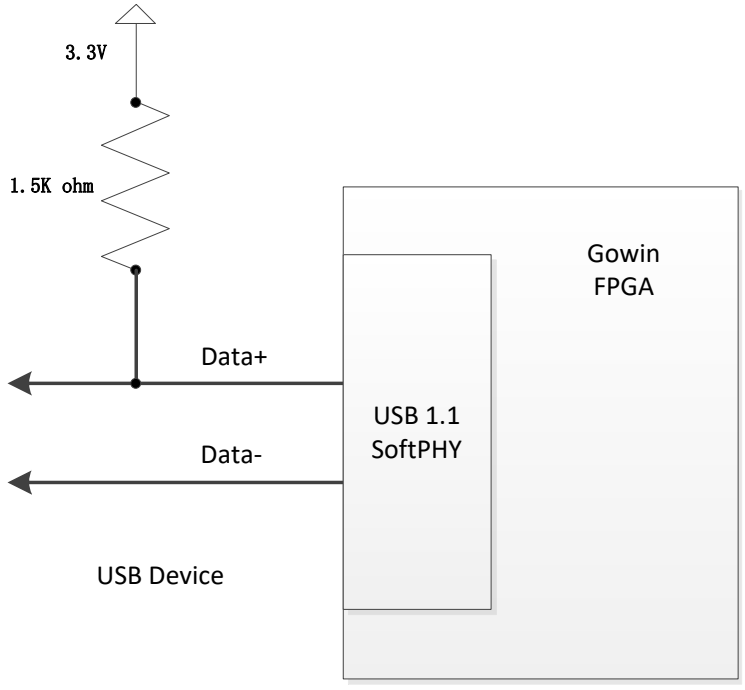
Mode (1.5Mbps); When USB 1.1 SoftPHY is used as the master device, a 15K pull-down resistor needs to be connected to Data+ and Data-.

Figure 3-2 USB Master Device Interface Implementation



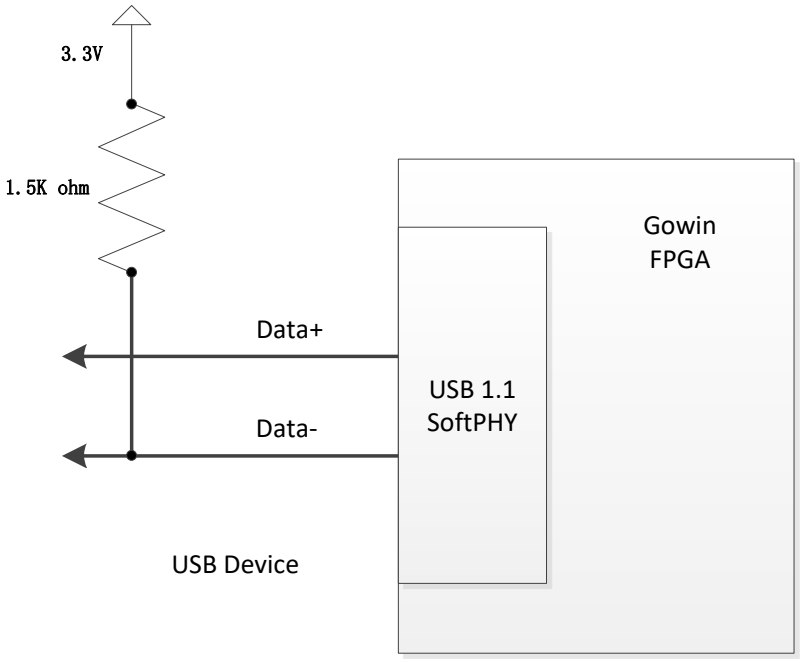
When USB 1.1 SoftPHY is used as the slave device in full speed, a 1.5K pull-up resistor needs to be connected to Data+.

Figure 3-3 USB Slave Device Interface Implementation



When USB 1.1 SoftPHY is used as the slave device in low speed, a 1.5K pull-up resistor needs to be connected to Data-.

Figure 3-4 USB Slave Device Interface Implementation



4 Signal Description

4.1 Signal Description

The descriptions of signals are as shown in Table 4-1.

Table 4-1 Signals Description

No.	Signal Name	I/O	Data Width	Description	Note
1	clk_i	I	1	Input clock signal (36MHz/48MHz/60MHz)	
2	rst_i	I	1	Asynchronous reset signal; reset the state machine inside of PHY	
3	utmi_data_out_i	I	8	Data input, 8-bit parallel TX data bus	
4	utmi_txvalid_i	I	1	TX data valid, active-high	
5	utmi_opmode_i	I	2	Operation mode selection signal: ● 2'b00: Normal ● 2'b01: No driver ● 2'b10: Disable bit stuffing and NRZI encoding ● 2'b11: Operation of not automatically generating start and end signals	–
6	utmi_xcvrselect_i	I	2	Transmit mode selection signal: ● 2'b00: HS transmission (Not supported) ● 2'b01: FS transmission ● 2'b10: LS transmission ● 2'b11: Reserved	
7	utmi_termselect_i	I	1	Termination selection:	

No.	Signal Name	I/O	Data Width	Description	Note
				● 1’ b0: HS termination enable (Not supported) ● 1’ b1: FS/LS termination enable	
8	utmi_data_in_o	O	8	Data Output, 8-bit parallel RX data bus	
9	utmi_txready_o	O	1	TX data ready signal, indicating that PHY can receive this data	
10	utmi_rxactive_o	O	1	RX data activation, indicating that the receive state machines detects the SYNC signal and starts receiving data	
11	utmi_rxvalid_o	O	1	RX data valid, active-high	
12	utmi_rxerror_o	O	1	RX data error; active-high indicates receive error	
13	utmi_linestate_o	O	2	Line status of receive: DM DP ● 2’b00: SE0 ● 2’b01: "J" status ● 2’b10: "K" status ● 2’b11: SE1	
14	usb_dp_io	I/O	1	USB data signal Data+	
15	usb_dn_io	I/O	1	USB data signal Data-	

4.2 Parameter Configuration Option

Gowin USB 1.1 SoftPHY IP parameter configuration is shown in Table 4-2.

Table 4-2 Configuration Option

Option	Description
Clock Frequency	Working clock frequency includes 36MHz, 48MHz and 60MHz

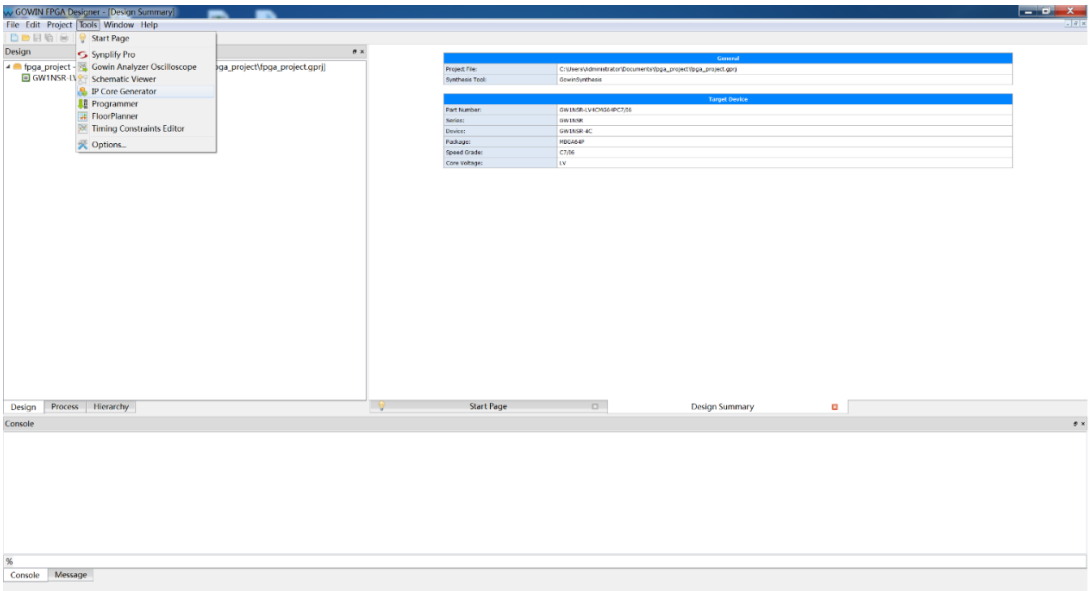
5 Interface Configuration

Select "Tools" in the Gowin Software interface, and you can start the IP Core Generator tool, call and configure USB 1.1 SoftPHY.

1. Open IP Core Generator

After creating the project, you can click the "Tools" tab in the upper left, select and open the IP Core Generator via the drop-down list, as shown in Figure 5-1.

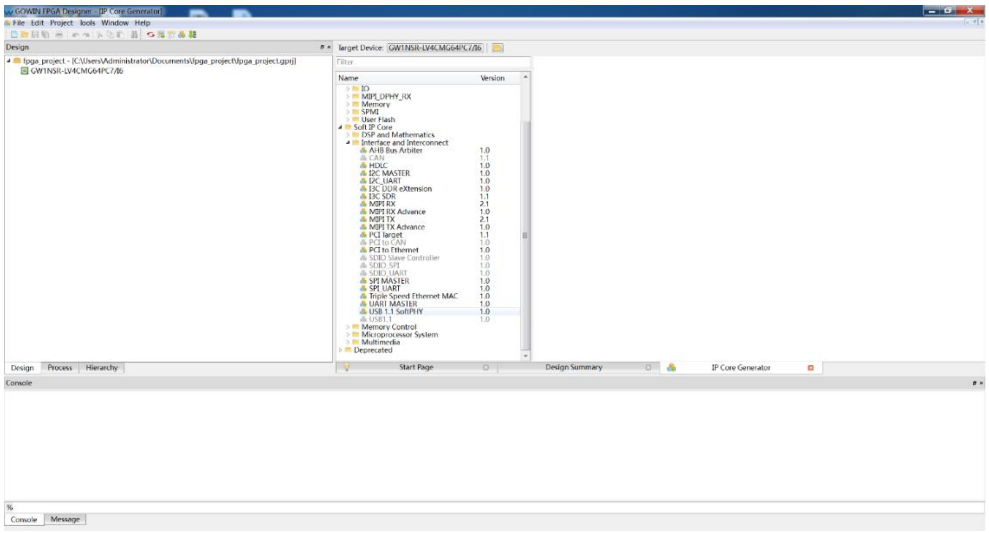
Figure 5-1 IP Core Generator



2. Open USB 1.1 SoftPHY IP Core

Select "Soft IP Core > Interface and Interconnect > USB 1.1 IP", as shown in Figure 5-2. Double click to open the configuration interface.

Figure 5-2 Open USB 1.1 SoftPHY IP Core

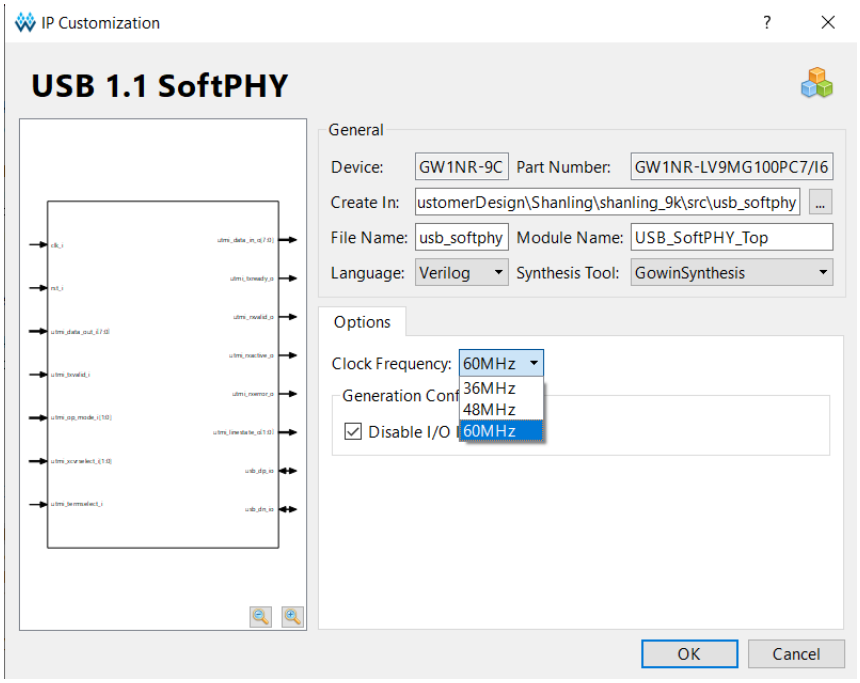


3. USB 1.1 SoftPHY IP Core Configuration Interface

Figure 5-3 shows the USB 1.1 SoftPHY IP core configuration interface. The interface diagram is on the left. Options are on the right.

- You can configure the file name in "File Name"
- You can configure the top module name in "Module Name"
- You can configure the speed mode, power supply mode, endpoint transmission type in "Options".

Figure 5-3 USB 1.1 SoftPHY IP Configuration Interface

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