



# Gowin UHS PSRAM Memory Interface IP

## User Guide

IPUG767-1.2E, 05/30/2025

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## Revision History

| Date       | Version | Description                                                                                                                                                                                                                                                                                 |
|------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 01/14/2021 | 1.0E    | Initial version published.                                                                                                                                                                                                                                                                  |
| 09/08/2023 | 1.1E    | <ul style="list-style-type: none"><li>● The descriptions of GW5AST-138 devices added.</li><li>● The descriptions of Chapter 7 Interface Configuration updated.</li><li>● Design source code (encrypted) removed.</li></ul>                                                                  |
| 05/30/2025 | 1.2E    | <ul style="list-style-type: none"><li>● UHS PSRAM Memory Interface V1.0 IP, UHS PSRAM Memory Interface V2.0 IP, UHS PSRAM Memory Interface 2CH V1.0 IP, and UHS PSRAM Memory Interface 2CH V2.0 IP merged into a single IP.</li><li>● All content related to 64M devices removed.</li></ul> |

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# 1 About This Guide

## 1.1 Purpose

The purpose of Gowin UHS PSRAM Memory Interface IP User Guide is to help you quickly learn the features and usage of Gowin UHS PSRAM Memory Interface IP by providing the descriptions of the functions, ports, timing, GUI, and reference design. The software screenshots in this manual are based on 1.9.11.02. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

The usage of 256 Mbit PSRAM (APS256XXN-OBR) and 32 Mbit PSRAM (APS3208K-OK) is basically the same, and this manual will use 32 Mbit PSRAM to introduce the usage of Gowin UHS PSRAM Memory Interface IP, and it is universal if not otherwise specified.

## 1.2 Related Documents

You can find the related documents at [www.gowinsemi.com](http://www.gowinsemi.com):

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS821, GW1NS series of FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS841, GW1NZ series of FPGA Products Data Sheet](#)
- [DS861, GW1NSR series of FPGA Products Data Sheet](#)
- [DS881, GW1NSER series of SecureFPGA products Data Sheet](#)
- [DS891, GW1NRF series of Bluetooth FPGA Products Data Sheet](#)
- [DS961, GW2ANR series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

## 1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

**Table 1-1 Terminology and Abbreviations**

| Terminology and Abbreviations | Meaning                            |
|-------------------------------|------------------------------------|
| 2CH                           | 2 Channels                         |
| GSR                           | Global System Reset                |
| IP                            | Intellectual Property              |
| LUT                           | Look-up Tables                     |
| PSRAM                         | Pseudo Static Random Access Memory |
| RAM                           | Random Access Memory               |
| UHS                           | Ultra High Speed                   |

## 1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: [www.gowinsemi.com](http://www.gowinsemi.com)

E-mail: [support@gowinsemi.com](mailto:support@gowinsemi.com)

# 2 Overview

Gowin UHS PSRAM Memory Interface IP is a common used PSRAM interface IP, in compliance with PSRAM standard protocol. The IP includes the PSRAM MCL (Memory Controller Logic) and the corresponding PHY (Physical Interface) design. Gowin UHS PSRAM Memory Interface IP provides you a generic command interface to connect with the PSRAM chip for data access and storage.

**Table 2-1 Gowin UHS PSRAM Memory Interface IP**

| Gowin UHS PSRAM Memory Interface IP |                                         |
|-------------------------------------|-----------------------------------------|
| Logic Resource                      | Please refer to Table 3-1               |
| Delivered Doc.                      |                                         |
| Design Files                        | Verilog (encrypted)                     |
| Reference Design                    | Verilog                                 |
| TestBench                           | Verilog                                 |
| Test and Design Flow                |                                         |
| Synthesis Software                  | GowinSynthesis                          |
| Application Software                | Gowin Software (1.9.9 Beta-3 and above) |

**Note!**

For the devices supported, you can click [here](#) to get the information.

# 3 Feature and Performance

## 3.1 Features

- Compatible with interfaces of standard PSRAM devices
- Supports memory data path width of 8 bits, 16 bits, 24 bits, and 32 bits
- Supports memory chip of x8/x16 data width
- Programs burst lengths 16, 32, 64 or 2048 bytes
- Supports linear continuous burst mode
- Supports clock rate 1:2
- Supports the initial latency 5/6/7
- Supports the fixed latency mode
- Supports the power off option
- Configurable drive strength
- Configurable self-refresh area
- Configurable refresh rate
- Single channel or two-channel operation mode to be chosen

## 3.2 Operating Frequency and Bandwidth Efficiency

The data rate and efficiency of Gowin UHS PSRAM Memory Interface IP supports:

- Maximum 400 Mbps
- In linear continuous burst mode, the longer the burst data, the higher the efficiency, which can be up to 90%

## 3.3 Resource Utilization

Gowin UHSPSRAM Memory Interface IP employs the Verilog language, which is used in the GW1N-4 and GW1NR-4 FPGA devices. Table 3-1 presents an overview of the resource utilization. For the applications on the other GOWINSEMI FPGA devices, please see the associated post-release information.

**Table 3-1 Resource Utilization**

| DQ_WIDTH | LOGICs | REGs | I/O | f <sub>MAX</sub> | Throughout                         | Device Series     | Speed Grade    |
|----------|--------|------|-----|------------------|------------------------------------|-------------------|----------------|
| 8(x8)    | 615    | 541  | 16  | 400Mbps          | f <sub>MAX</sub> x DQ x Efficiency | GW1N-4<br>GW1NR-4 | C6/I5<br>C5/I4 |
| 16(x8)   | 947    | 898  | 29  |                  |                                    |                   |                |

**Note!**

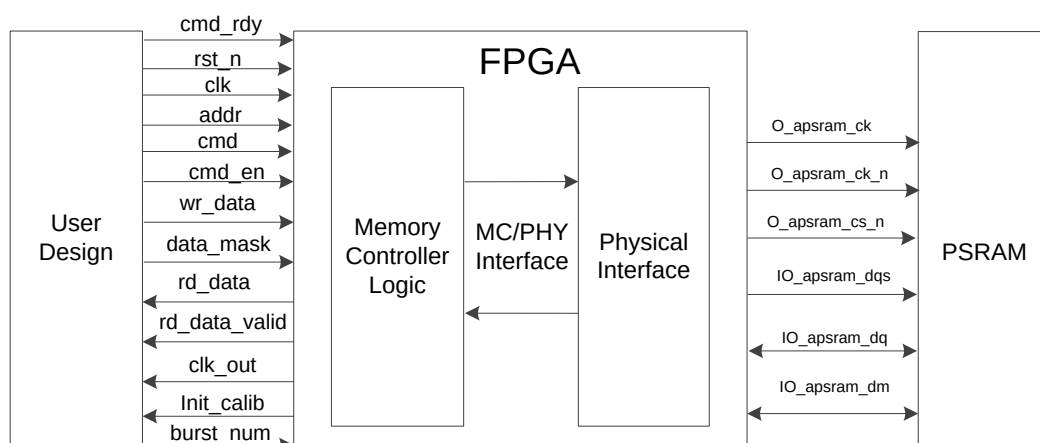
In Table 3-1, the user address width of Gowin UHS PSRAM Memory Interface IP is 22 bits, and PSRAM WIDTH is x8. The two-channel PSRAM IP will also increase the resource utilization.

# 4 Functional Description

## 4.1 Architecture

As shown in Figure 4-1, Gowin UHS PSRAM Memory Interface IP mainly includes Memory Controller Logic, Physical Interface, etc. The User Design module in Figure 4-1 is the module connected to the external PSRAM chip in FPGA.

**Figure 4-1 Gowin UHS PSRAM Memory Interface IP Structure**



## 4.2 Memory Controller Logic

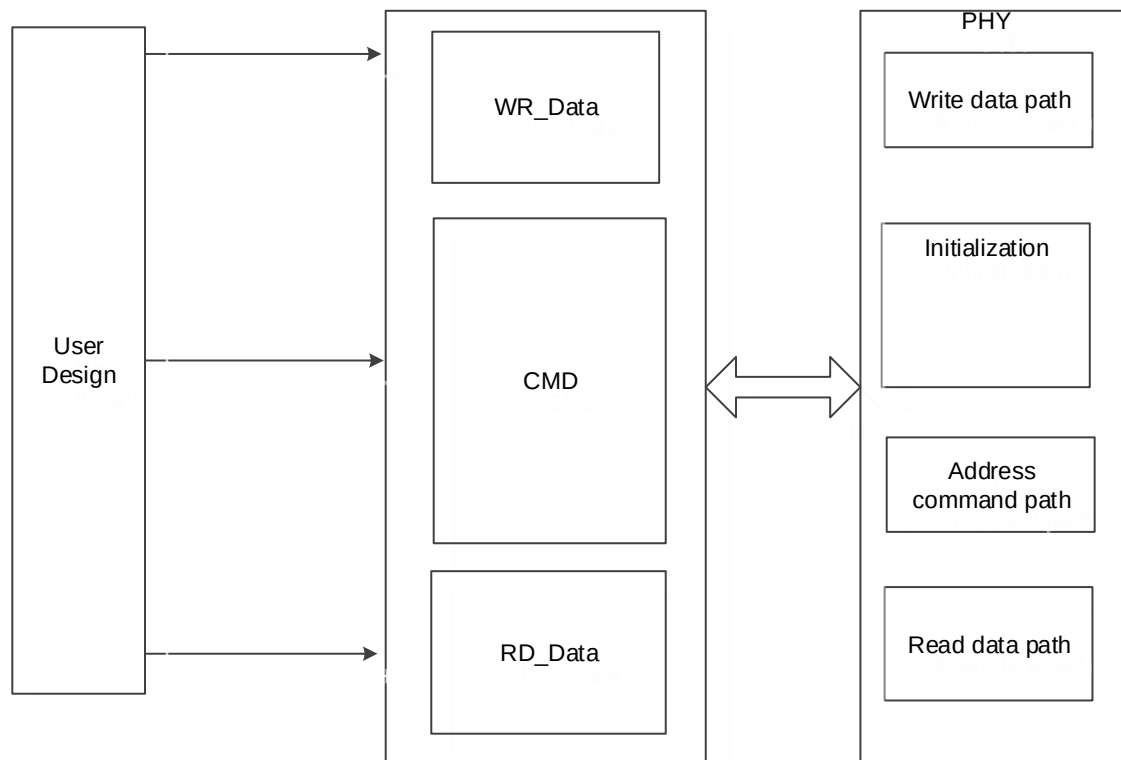
Memory Controller Logic is the logic module of Gowin PSRAM Interface IP, which locates between User Design and PHY. The Memory Controller Logic receives the command, address, and data from the user interface and stores them in logical order.

The write, read and other commands sent by the user are sorted and reorganized in Memory Controller Logic to combine a data format that complies with the PSRAM protocol. Meanwhile, when the Memory Controller Logic writes data, the data will be reorganized and cached to meet the initial delay value between the command and the data. When the Memory Controller Logic reads the data, the data will be sampled and reorganized to be the correct one.

UHS PSRAM Memory Controller includes the CMD unit, the WR\_Data

unit, the RD\_Data unit, etc. The main structure is shown in Figure 4-2.

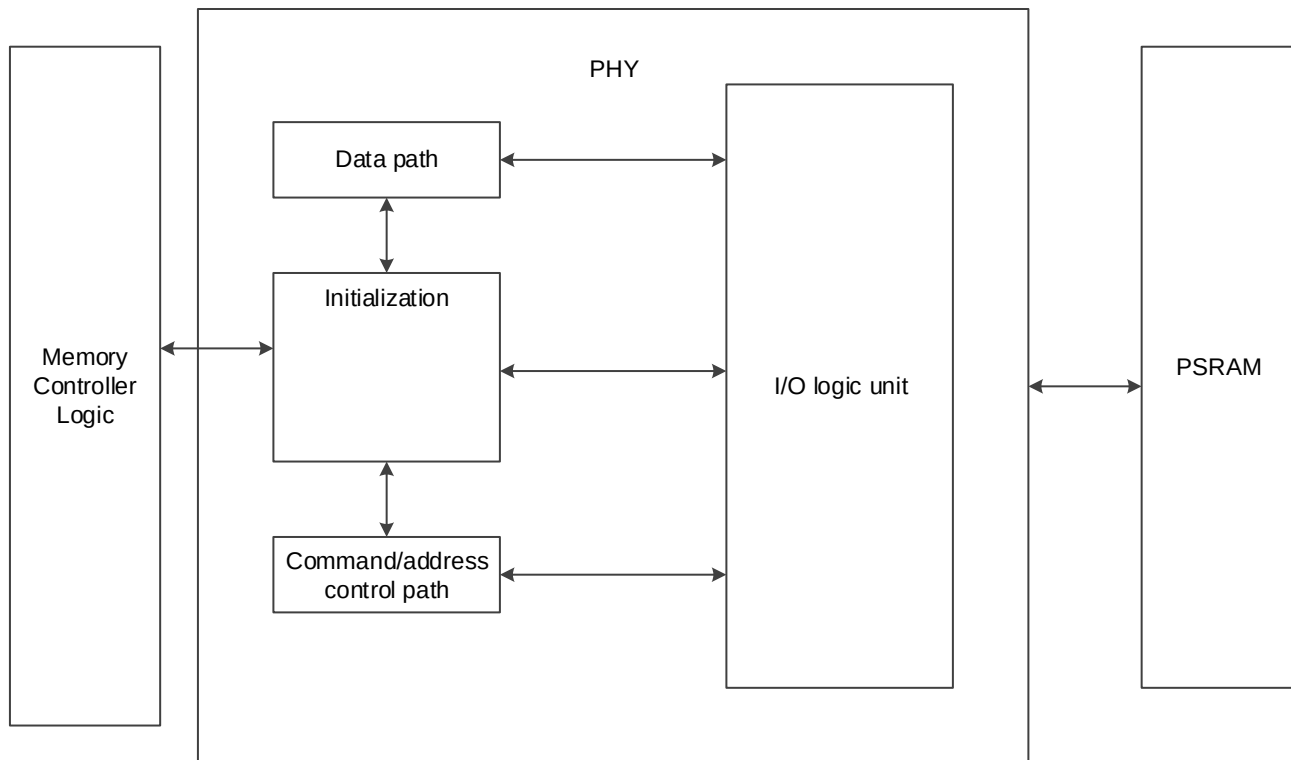
**Figure 4-2 UHS PSRAM Memory Controller Logic Structure**



## 4.3 PHY

The PHY provides the physical layer definition and interface between Memory Controller Logic and the external PSRAM. It receives the commands and data from the Memory Controller Logic and provides the PSRAM interface with signals that meet the timing and sequence requirements.

The basic structure of the PHY includes four modules: initialization module, data path, command/address control path and I/O logic module, as shown in Figure 4-3.

**Figure 4-3 PSRAM PHY Structure**

### 4.3.1 Initialization Unit

The initialization module is mainly used for the initialization and read-calibration after power on. After all initialization and read-calibration are finished, the signal "init\_calib" will become high to indicate the completion of the entire initialization.

#### Power-on Initialization

According to the PSRAM protocol standard, it needs to initialize the PSRAM after power on. This includes the reset, mode register configuration, and read calibration.

### 4.3.2 Data Path Unit

Data path includes write data path and read data path.

### 4.3.3 Control Path Unit

The command/address control path is a single pass that receives the command and address signal sent by the Memory Controller Logic and cooperates with the data path to process the write and read data delay parameters and sends the commands to the I/O logic module.

### 4.3.4 I/O Logic Unit

The Logic I/O module is mainly used to convert the clock domain of the data, command, and address signals received from the data path and command/address path.

## 4.4 Primary Function

The functions of UHS PSRAM Memory Interface IP are as follows:

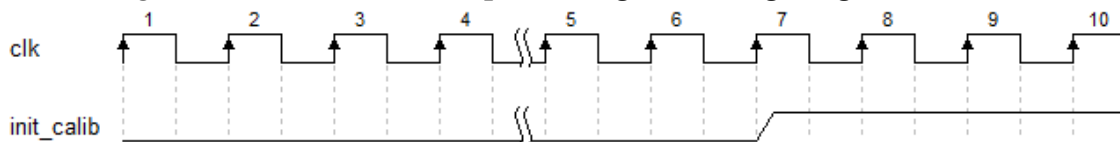
- Initializes the PSRAM
- Sends the addresses and commands
- Writes data
- Reads data

### 4.4.1 Initialization

PSRAM must be read calibrated to perform normal write and read operations. Therefore, after power on, PHY performs initialization read calibration operation on PSRAM and returns to `init_calib` after initialization completion. Single-channel PSRAM IP initializes two PSRAM particles at the same time, while two-channel IP initializes two PSRAM particles respectively and sends two initialization completion signals to the user respectively.

The completion signal is returned to the user after the initialization is completed, as shown in Figure 4-4.

Figure 4-4 Initialization Completion Signal Timing Diagram



### 4.4.2 Send Addresses and Commands

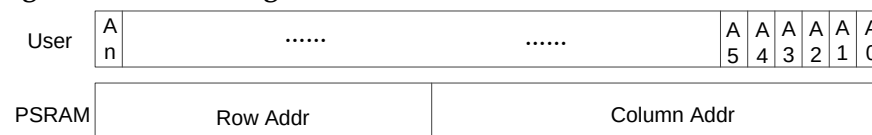
You can send operation commands and addresses through the `addr`, `cmd`, and `cmd_en` user interfaces.

- The `addr` serves as the address data port. The IP design adopts bit-width extension to increase bandwidth. When multiple PSRAM chips are used, the IP treats them as a single PSRAM for access. Users do not need to consider address bit width changes when selecting one or multiple PSRAM chips. The address is a byte address. With 1 PSRAM chip, one byte is stored per address. With 2 PSRAM chips, two bytes are stored per address, and so on. For continuous address write operations, the address increments by  $(burst\_num + 1) \times 4$  between adjacent operations. The same rule applies to continuous address read operations.
- The `cmd` is the command data port.
- `cmd_en` is the address and command enable signal, which is active-high.

**Note!**

The dual-channel PSRAM IP operates in the same manner as the single-channel PSRAM IP. However, the two channels of the dual-channel IP have independent command and address signals, requiring separate control signals for each channel.

In the application, a mapping relationship exists between the address bus of user interface and the physical memory ROW, Upper Column, and Lower Column. In this design, it is in ROW-Column-Lower Column order. The addressing scheme is as shown Figure 4-5. In the application, you need to give the address as needed, and the mapping relationship is no concerned.

**Figure 4-5 Addressing Scheme in Row-Column Order**

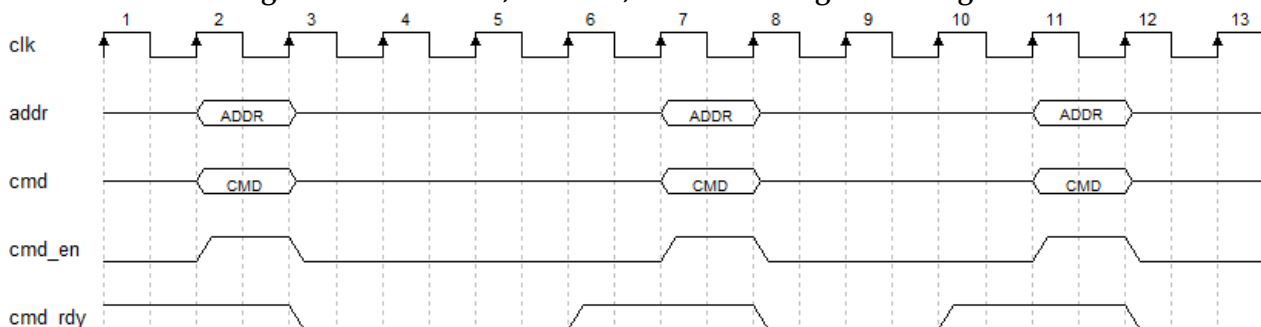
The commands sent by users through the cmd interface are as shown in Table 4-1:

**Table 4-1 cmd Command**

| Command | cmd  |
|---------|------|
| Read    | 1'b0 |
| Write   | 1'b1 |

At the user interface, the timing between the command, address, and enable signals is as shown in Figure 4-6.

When cmd\_en is high, the cmd and addr are valid at this time, and you need to wait for cmd\_rdy to be pulled high before sending the command. cmd\_rdy is pulled high to indicate that the controller is in idle state to accept the user commands.

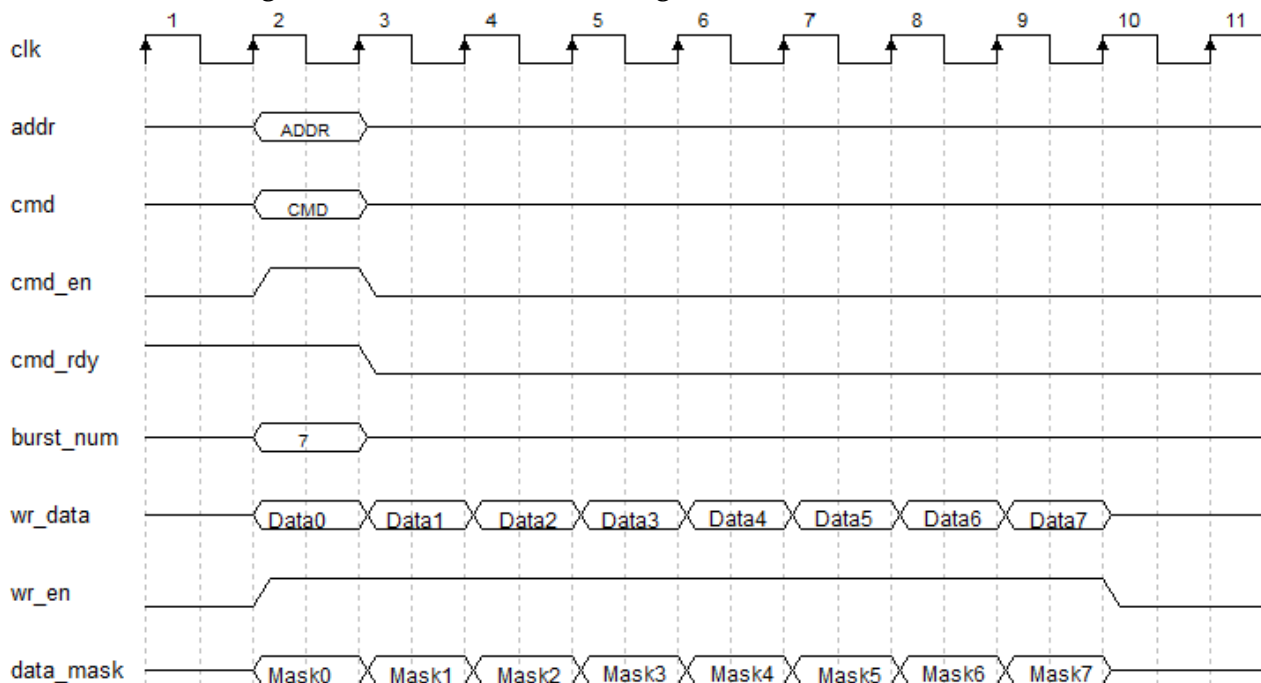
**Figure 4-6 Command, Address, and Enable Signal Timing****4.4.3 Write Data**

You can send the data to Gowin UHS PSRAM Memory Interface IP through wr\_data, wr\_en, burst\_num, data\_mask ports. The write data will be sent to the PSRAM after being processed.

- wr\_data is a write data port.

- `wr_en` is a write enable signal.
- `burst_num` is the data number of this burst.
- `data_mask` is a write mask port.
- There are multiple timing relations between the data channel and the command channel. Take `Burst_num` 8 equal to as an example as shown in Figure 4-7.
- The write operation mode of two-channel PSRAM IP and single channel PSRAM IP is the same, but the command and address of the two-channel PSRAM IP are independent, and write data need to be given respectively.

Figure 4-7 Write Data Port Timing



- `burst_num` is the number of linear continuous burst, the minimum is 1, that is, 2 user data. In the above figure, 7 means it writes 8 data continuously. The maximum value of `burst_num` with different frequencies as shown in Table 4-2.
- You need to calculate the address if there are continuous operations. In the above figure, burst 8 user data, for the next write operation, the address is  $(\text{burst\_num} + 1) \times 4$ , that is, 32.
- If the mask function is not used, the `data_mask` can be 0.

Table 4-2 `Burst_num` Maximum Value and Frequency

| Burst_num Max. | Memory_clk Frequency | WL |
|----------------|----------------------|----|
| 163            | 133MHz               | 0  |
| 191            | 166MHz               | 0  |
| 191            | 200MHz               | 0  |
| 245            | 200MHz               | 2  |

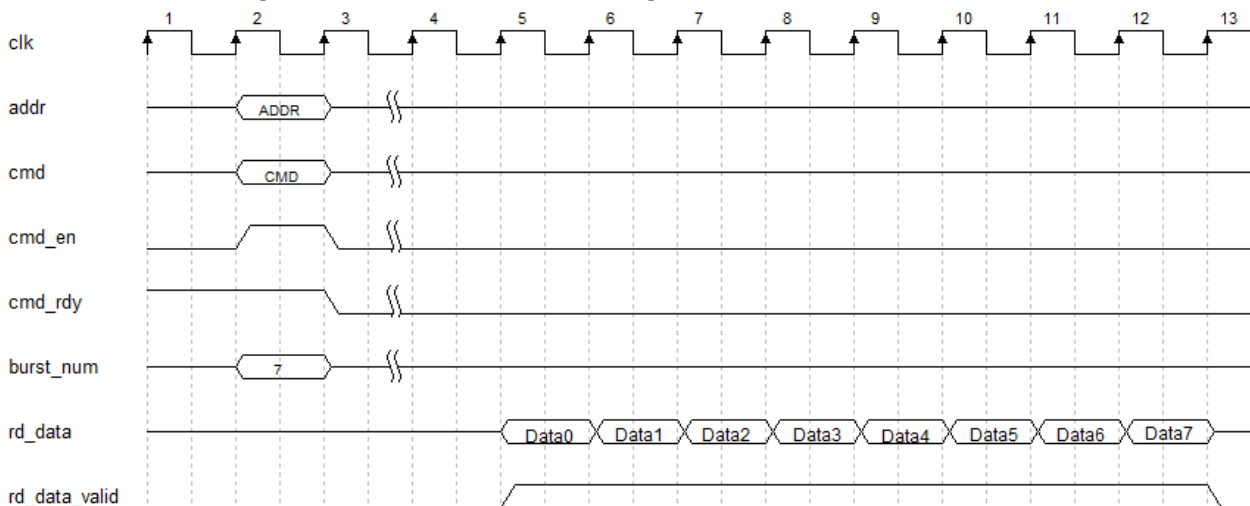
| Burst_num Max. | Memory_clk Frequency | WL |
|----------------|----------------------|----|
| 255            | 233MHz               | 2  |

#### 4.4.4 Read Data

You can read the data returned by PSRAM through rd\_data, rd\_data\_valid ports.

- rd\_data is the returned read data port.
- rd\_data\_valid is the read data valid port. When it is high, the returned rd\_data is valid at this time.
- There are multiple timing relations between read data channel and the command channel. Take Burst\_num equal to 8 as an example as shown in Figure 4-8.
- The read operation mode of two-channel PSRAM IP and single-channel PSRAM IP is the same, but the command and address of the two-channel PSRAM IP are independent, and The rd\_data\_valid signal and rd\_data data need to be received respectively.

Figure 4-8 Read Data Port Timing



- You need to calculate the address if there are continuous operations. In the above figure, burst 8 user data, for the next operation, the address is  $(burst\_num + 1) \times 4$ , that is, 32.
- For read, the burst\_num max. value is 1023.

# 5 Port List

The I/O ports of Gowin UHS PSRAM Memory Interface IP are shown in Table 5-1 and Table 5-2.

**Table 5-1 I/O Port List of Gowin UHS PSRAM Memory Interface IP (1 Channel)**

| Signal         | Data Width | I/O    | Description                                                                             |
|----------------|------------|--------|-----------------------------------------------------------------------------------------|
| User Interface |            |        |                                                                                         |
| addr           | ADDR_WIDTH | Input  | Address input                                                                           |
| cmd            | 1          | Input  | Command channel                                                                         |
| cmd_en         | 1          | Input  | Command and address enable signals<br>0: invalid<br>1: valid                            |
| cmd_rdy        | 1          | output | Ready to write command<br>0: No<br>1: Yes                                               |
| rd_data        | 4*DQ_WIDTH | Output | Read data channel                                                                       |
| rd_data_valid  | 1          | Output | rd_data valid signal<br>0: invalid<br>1: valid                                          |
| wr_data        | 4*DQ_WIDTH | Input  | Write data channel                                                                      |
| wr_en          | 1          | Input  | Write data enable signal<br>0: Invalid<br>1: Valid                                      |
| data_mask      | MASK_WIDTH | Input  | Provides the mask signals for wr_data                                                   |
| clk_d          | 1          | Input  | clkoutd pin using the same PLL with memory_clk, generally divided-by-four of memory_clk |
| init_calib     | 1          | Output | Initialization completed signal                                                         |
| clk_out        | 1          | Output | The clock with a frequency of 1/2 Memory Clk for user design                            |
| rst_n          | 1          | Input  | User input reset signal<br>0: valid<br>1: invalid                                       |

| Signal          | Data Width | I/O         | Description                                                                                                                                       |
|-----------------|------------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| memory_clk      | 1          | Input       | The PSRAM operating clock, which is generally a high-speed clock multiplied by PLL, or you can also choose not to use PLL                         |
| memory_clk_p    | 1          | Input       | 90° shift clock of memory_clk, generally the clkoutp pin using the same PLL                                                                       |
| pll_lock        | 1          | Input       | If memory_clk is multiplied by PLL, this port is connected to pll_lock pin of PLL<br>If the user does not use PLL, this port is connected to 1'b1 |
| PSRAM Interface |            |             |                                                                                                                                                   |
| O_apsram_cs_n   | CS_WIDTH   | Output      | Chip selected, active-low.                                                                                                                        |
| O_apsram_ck     | CS_WIDTH   | Output      | A clock signal provided to PSRAM                                                                                                                  |
| O_apsram_ck_n   | CS_WIDTH   | Output      | Composes the differential signal with the O_apsram_ck                                                                                             |
| O_apsram_dm     | CS_WIDTH   | Output      | PSRAM mask signal                                                                                                                                 |
| IO_apsram_dq    | DQ_WIDTH   | Bidirection | PSRAM data                                                                                                                                        |
| IO_apsram_dqs   | CS_WIDTH   | Bidirection | PSRAM data strobe signal                                                                                                                          |

**Table 5-2 I/O Port List of Gowin UHS PSRAM Memory Interface IP (2 Channels)**

| Signal         | Data Width | I/O    | Description                                                            |
|----------------|------------|--------|------------------------------------------------------------------------|
| User Interface |            |        |                                                                        |
| addr0          | ADDR_WIDTH | Input  | Channel 0 address input                                                |
| addr1          | ADDR_WIDTH | Input  | Channel 1 address input                                                |
| cmd0           | 1          | Input  | Channel 0 command channel                                              |
| cmd1           | 1          | Input  | Channel 1 command channel                                              |
| cmd_en0        | 1          | Input  | Channel 0 command and address enable signal:<br>0: invalid<br>1: valid |
| cmd_en1        | 1          | Input  | Channel 1 command and address enable signal:<br>0: invalid<br>1: valid |
| cmd_rdy0       | 1          | output | Ready to write channel 0 command<br>0: No<br>1: Yes                    |
| cmd_rdy1       | 1          | output | Ready to write channel 1 command<br>0: No<br>1: Yes                    |

| Signal          | Data Width | I/O    | Description                                                                                                                                   |
|-----------------|------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| rd_data0        | 4*DQ_WIDTH | Output | Read data channel 0                                                                                                                           |
| rd_data1        | 4*DQ_WIDTH | Output | Read data channel 1                                                                                                                           |
| rd_data_valid0  | 1          | Output | Channel 0rd_data valid signal<br>0: invalid<br>1: valid                                                                                       |
| rd_data_valid1  | 1          | Output | Channel 1rd_data valid signal:<br>0: invalid<br>1: valid                                                                                      |
| wr_data0        | 4*DQ_WIDTH | Input  | Write data channel 0                                                                                                                          |
| wr_data1        | 4*DQ_WIDTH | Input  | Write data channel 1                                                                                                                          |
| wr_en0          | 1          | Input  | Channel 0 write data enable signal<br>0: Invalid<br>1: Valid                                                                                  |
| wr_en1          | 1          | Input  | Channel 1 write data enable signal<br>0: Invalid<br>1: Valid                                                                                  |
| data_mask0      | MASK_WIDTH | Input  | Provides the mask signals for channel 0wr_data                                                                                                |
| data_mask1      | MASK_WIDTH | Input  | Provides the mask signals for channel 1wr_data                                                                                                |
| init_calib0     | 1          | Output | Channel 0 initialization completed signal                                                                                                     |
| init_calib1     | 1          | Output | Channel 1 initialization completed signal                                                                                                     |
| clk_d           | 1          | Input  | clkoutd pin using the same PLL with memory_clk, generally divided-by-four of memory_clk.                                                      |
| clk_out         | 1          | Output | The clock with a frequency of 1/2 Memory Clk for user design                                                                                  |
| rst_n           | 1          | Input  | User input reset signal<br>0: valid<br>1: invalid                                                                                             |
| memory_clk      | 1          | Input  | The PSRAM operating clock, which is generally a high-speed clock multiplied by PLL, or you can also choose not to use PLL                     |
| memory_clk_p    | 1          | Input  | 90° shift clock of memory_clk, generally the clkoutp pin using the same PLL                                                                   |
| pll_lock        | 1          | Input  | If memory_clk is multiplied by PLL, this port is connected to pll_lock pin of PLL<br>If user does not use PLL, this port is connected to 1'b1 |
| PSRAM Interface |            |        |                                                                                                                                               |

| Signal        | Data Width | I/O         | Description                                           |
|---------------|------------|-------------|-------------------------------------------------------|
| O_apsram_cs_n | 2*CS_WIDTH | Output      | Chip selected, active-low.                            |
| O_apsram_ck   | 2*CS_WIDTH | Output      | A clock signal provided to PSRAM                      |
| O_apsram_ck_n | 2*CS_WIDTH | Output      | Composes the differential signal with the O_apsram_ck |
| O_apsram_dm   | 2*CS_WIDTH | Output      | PSRAM mask signal                                     |
| IO_apsram_dq  | 2*DQ_WIDTH | Bidirection | PSRAM data                                            |
| IO_apsram_dqs | 2*CS_WIDTH | Bidirection | PSRAM data strobe signal                              |

# 6 Parameter Configuration

Gowin UHS PSRAM Memory Interface IP supports PSRAM devices. You need to configure static parameters and timing parameters of the Gowin UHS PSRAM Memory Interface IP according to the design requirements. The specific parameters are as shown in Table 6-1.

**Table 6-1 Static Parameter Options**

| Name           | Description                                                                           | Options                                                                                                                                                                                                                                                                                    |
|----------------|---------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Memory TYPE    | PSRAM part number                                                                     | You can select APS3208K-OK or APS256XXN-OBR. APS3208K-OK is a PSRAM device with a capacity of 32 Mbit, and APS256XXN-OBR is a PSRAM device with a capacity of 256 Mbit.                                                                                                                    |
| CLk Ratio      | The CLK ratio of the PSRAM PHY and internal logic clock, cannot be operated by users. | 1:2                                                                                                                                                                                                                                                                                        |
| Channel Number | Number of channels                                                                    | 1 channel/2 channel                                                                                                                                                                                                                                                                        |
| PSRAM Width    | DQ Width of one PSRAM                                                                 | 8                                                                                                                                                                                                                                                                                          |
| DQ Width       | The total data width required by the user.                                            | The values include 8,16, 24,32. For example, when 16 is selected, the IP will interface with two PSRAM chips. When the user selects an FPGA with embedded PSRAM, the maximum selectable data width for this option must not exceed the total data width of the embedded PSRAM in the FPGA. |
| ADDR Width     | Address width, filled by users according to the specific chip.                        | <ul style="list-style-type: none"> <li>For 32 Mbit PSRAM, you can choose 22.</li> <li>For 256 Mbit PSRAM, you can choose 25.</li> </ul>                                                                                                                                                    |
| Data Width     | User data bit width                                                                   | 4*DQ Width                                                                                                                                                                                                                                                                                 |
| CS Width       | Chip selection width                                                                  | DQ Width/PSRAM Width                                                                                                                                                                                                                                                                       |
| Mask Width     | Mask Width                                                                            | Data Width/PSRAM Width                                                                                                                                                                                                                                                                     |
| Simulation     | Simulation acceleration button                                                        | <ul style="list-style-type: none"> <li>You can click this button to</li> </ul>                                                                                                                                                                                                             |

| Name                 | Description                                                  | Options                                                                                                               |
|----------------------|--------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------|
|                      |                                                              | accelerate simulation<br>● Not checked for the board test                                                             |
| Buffer Type          | The hardware resource used for data buffering within the IP. | BSRAM, SSRAM or REG                                                                                                   |
| Burst Type           | Burst Type                                                   | ● For 256 Mbit, you can select 16/32/64/2048<br>● For 32 Mbit, this option is grayed out                              |
| Burst Length         | Burst Length                                                 | ● For 256 Mbit, you can select Word/Hybrid<br>● For 32 Mbit, this option is grayed out.                               |
| Fixed Latency Enable | Fixed Latency Enable                                         | Fixed                                                                                                                 |
| Initial Latency      | Initial Latency                                              | ● For 32 Mbit, you can select 5/6<br>● For 256 Mbit, this option is grayed out                                        |
| RL                   | Read latency                                                 | ● For 256 Mbit, you can select 6/7, and it needs to be consistent with WL<br>● For 32 Mbit, this option is grayed out |
| WL                   | Write latency                                                | ● For 256 Mbit, you can select 6/7, and it needs to be consistent with RL<br>● For 32Mbit, you can select 0/2         |
| Drive Strength       | Drive strength                                               | 1/2, 1/4, 1/8, 1/16                                                                                                   |
| Deep Power Down      | Deep Power Down                                              | ● For 256 Mbit, you can select None/Half_Sleep/Deep_Power_Down<br>● For 32 Mbit, this option is grayed out            |
| Refresh Rate         | Refresh Rate                                                 | ● For 256 Mbit, you can select 4X/1X/0.5X<br>● For 32 Mbit, this option is grayed out                                 |
| DQ Mode              | DQ Mode                                                      | ● For 256 Mbit, you can select X8/X16<br>● For 32 Mbit, this option is grayed out                                     |
| RBX                  | Cross-row read and write                                     | ● For 256 Mbit, you can select ON/OFF<br>● For 32 Mbit, this option is grayed out                                     |
| PASR                 | Self Refresh Area                                            | full, bottom_1/2, bottom_1/4, bottom_1/8, top_1/2, top_1/4, top_1/8                                                   |

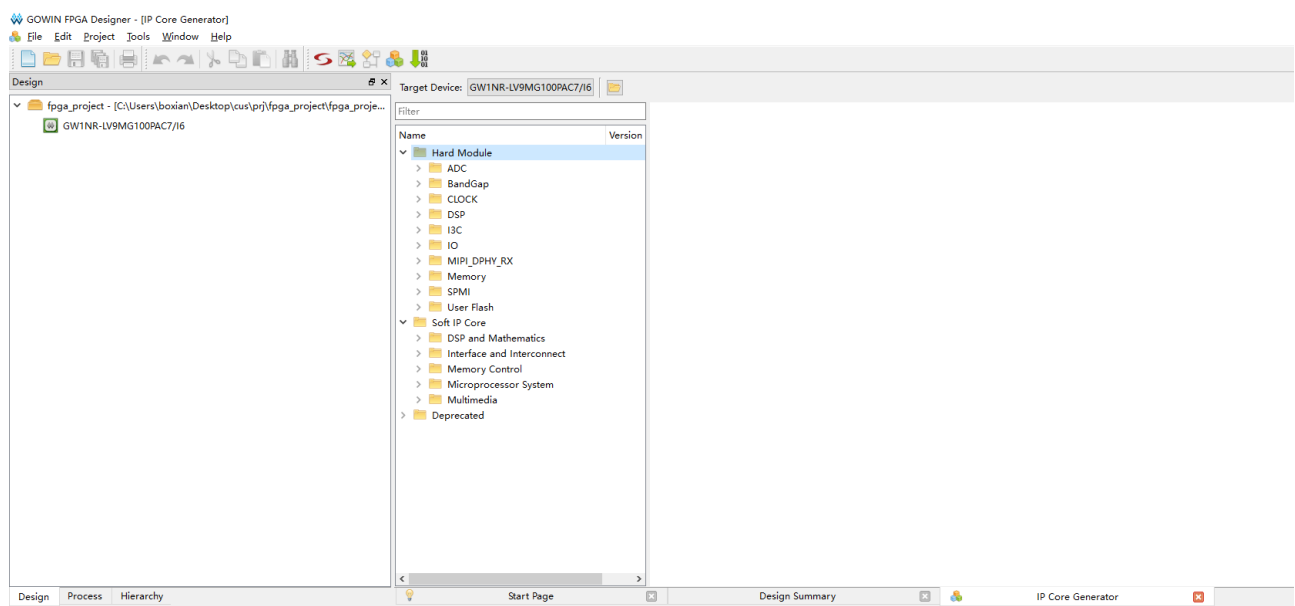
# 7 Interface Configuration

You can call and configure Gowin UHS PSRAM Memory Interface IP using the IP Core tool in the IDE. This section will introduce the GUI and configuration options.

## 1. Open IP Core Generator

After creating the project, you can click the "Tools" tab in the upper left, select and open the IP Core Generator via the drop-down list, as shown in Figure 7-1.

**Figure 7-1 Open IP Core Generator**

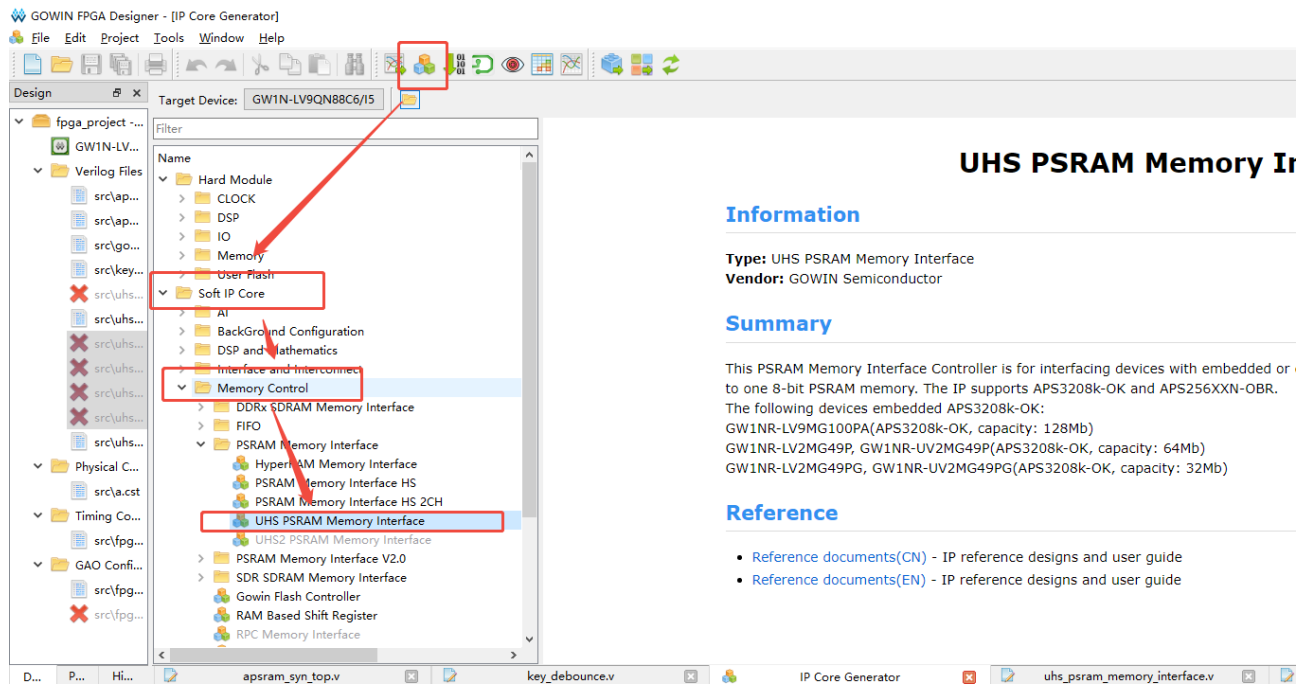


## 2. Open UHS PSRAM Memory Interface IP core

Click "Soft IP Core > Memory Control > PSRAM Memory Interface", double-click UHS PSRAM Memory Interface to open UHS PSRAM Memory Interface IP core open, as shown in Figure 7-2.

A brief introduction of the IP can be found by clicking the link under "References".

Figure 7-2 Open UHS PSRAM Memory Interface V1.0 IP Core

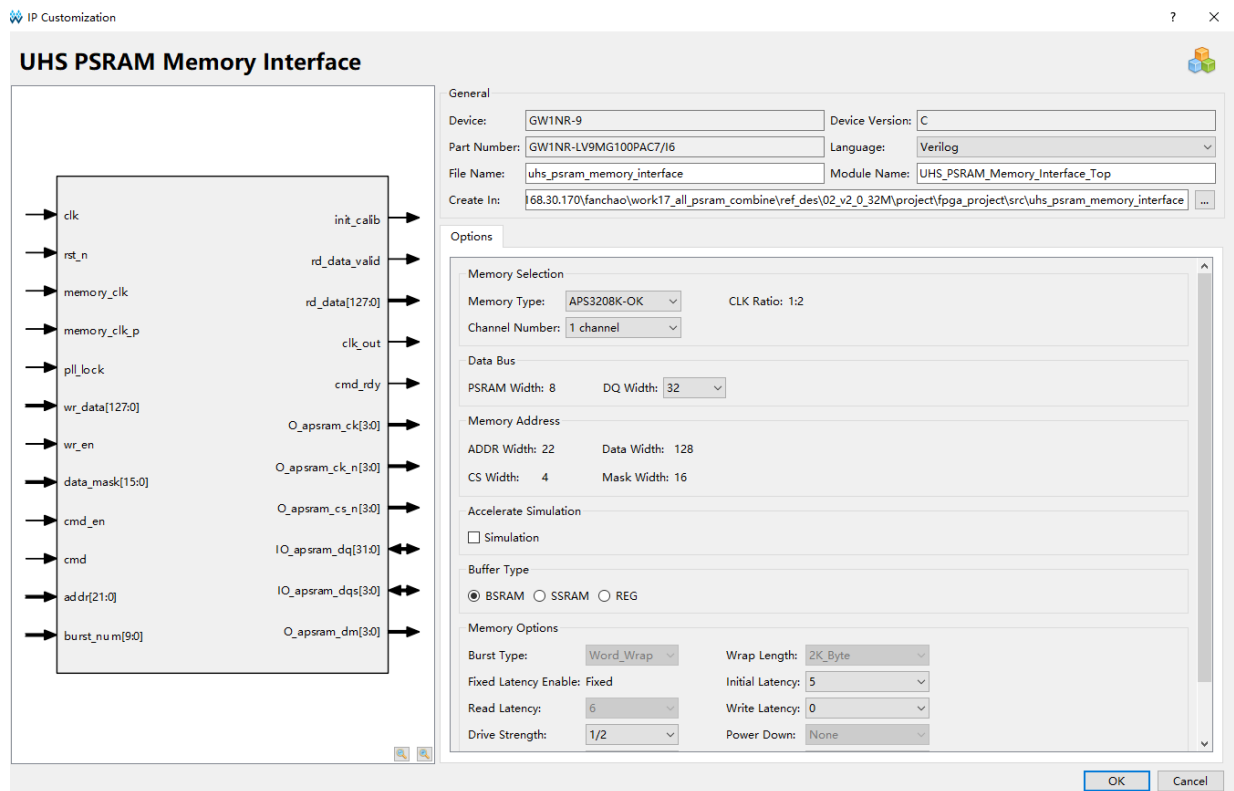


### 3. UHS PSRAM Memory Interface IP Core Ports

The ports of UHS PSRAM Interface IP core is on the left, as shown in Figure 7-3.

The right side of the view is the interfaces between the UHS PSRAM Memory Controller and users. You can send/receive the commands and data through connecting your design to the UHS PSRAM Memory Interface IP. The left side of the view is the interfaces between the physical interface (PHY) and the memory. You can access the data through connecting the UHS PSRAM Memory Interface IP core to your required memory. With different configurations, the signal bit width and the signal number will change accordingly.

Figure 7-3 IP Core Ports

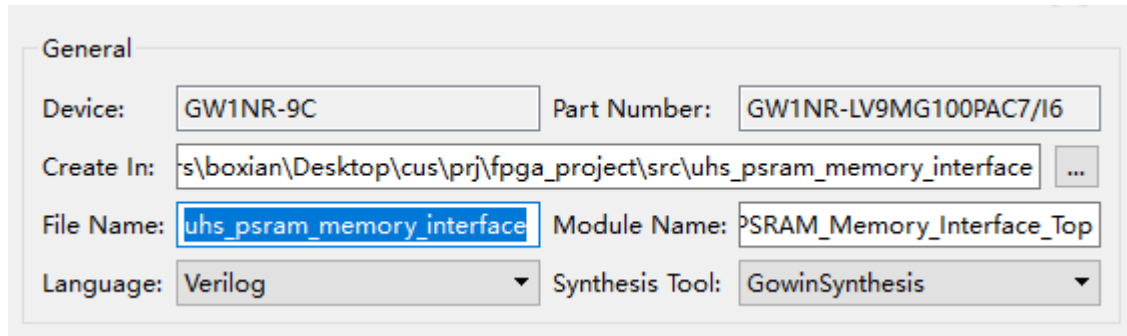


#### 4. Configure General Information

See the general information in the upper part of the configuration interface. Take the GW1NR-9C as an example, and select the MBGA100PA package.

- The "Module Name" option displays the top-level file name of the generated project, and the default is "UHS\_PSRAM\_Memory\_Interface\_Top". You can modify the name.
- The "File Name" option displays the folder generated by the IP core, which contains the files required by UHS PSRAM Memory Interface IP core, and the default is "uhs\_psrasm\_memory\_interface". You can modify the path.
- The "Create In" option displays the path of IP core folder. The default is "\project path\src\ uhs\_psrasm\_memory\_interface". You can modify the path.

Figure 7-4 General Information Configuration Interface



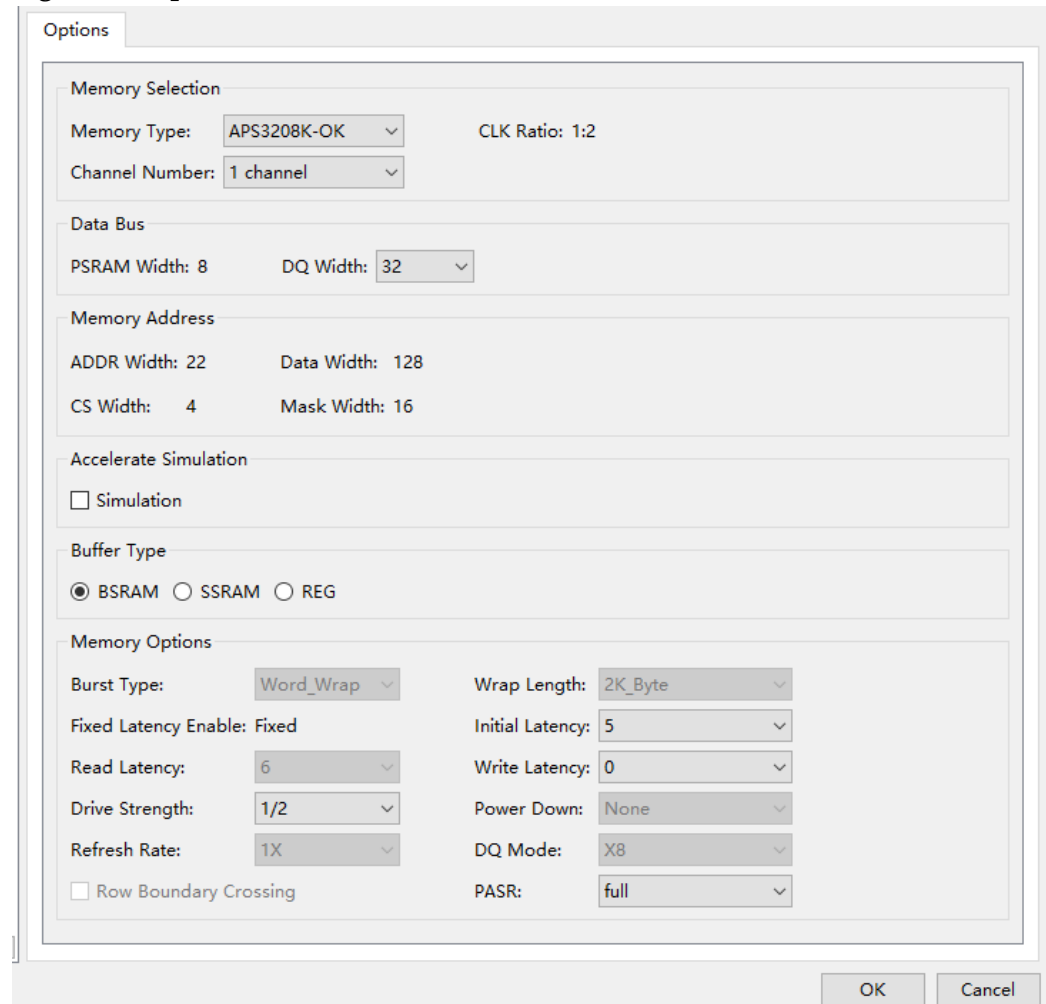
The General Information Configuration Interface dialog box contains the following fields:

- Device:** GW1NR-9C
- Part Number:** GW1NR-LV9MG100PAC7/I6
- Create In:** s:\boxian\Desktop\cus\prj\fpga\_project\src\uhs\_psram\_memory\_interface ...
- File Name:** uhs\_psram\_memory\_interface
- Module Name:** PSRAM\_Memory\_Interface\_Top
- Language:** Verilog
- Synthesis Tool:** GowinSynthesis

## 5. Options Tab

For the parameter descriptions in options tab, you can see Chapter [6](#) *Parameter Configuration*.

Figure 7-5 Options Tab



The Options Tab configuration interface includes the following sections and parameters:

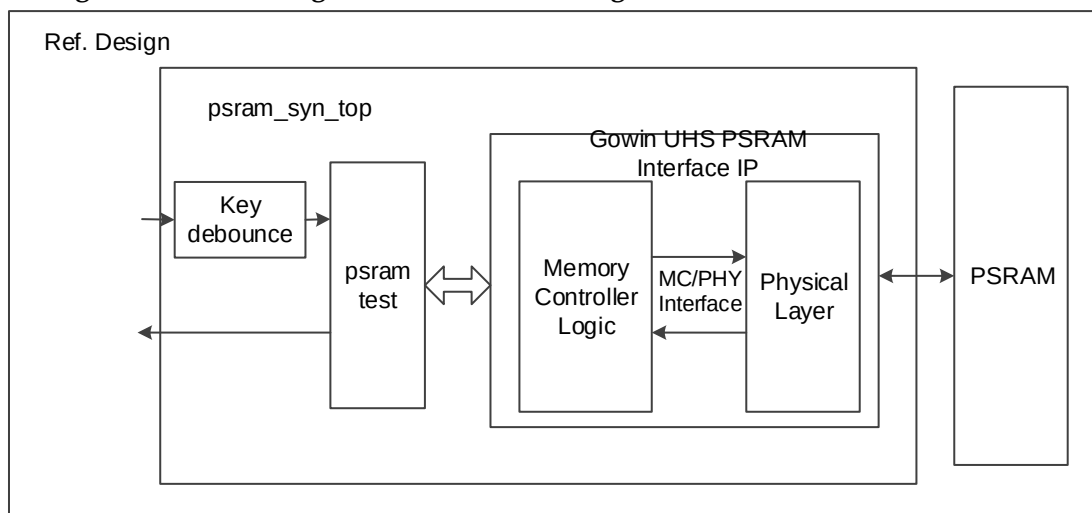
- Memory Selection**
  - Memory Type: APS3208K-OK
  - Channel Number: 1 channel
  - CLK Ratio: 1:2
- Data Bus**
  - PSRAM Width: 8
  - DQ Width: 32
- Memory Address**
  - ADDR Width: 22
  - Data Width: 128
  - CS Width: 4
  - Mask Width: 16
- Accelerate Simulation**
  - ☐ Simulation
- Buffer Type**
  - ☒ BSRAM ☐ SSRAM ☐ REG
- Memory Options**
  - Burst Type: Word\_Wrap
  - Wrap Length: 2K\_Byte
  - Fixed Latency Enable: Fixed
  - Initial Latency: 5
  - Read Latency: 6
  - Write Latency: 0
  - Drive Strength: 1/2
  - Power Down: None
  - Refresh Rate: 1X
  - DQ Mode: X8
  - ☐ Row Boundary Crossing
  - PASR: full

Buttons: OK, Cancel

# 8 Reference Design

To quickly familiar with and use Gowin UHS PSRAM Memory Interface IP, a simple [reference design](#) is provided for you. The basic structure of reference is shown in Figure 8-1.

**Figure 8-1 Block Diagram of Reference Design**



In the reference design, the `psram_syn_top` module is the top-level module, and its ports are connected to the input reference clocks, external reset signals, etc. as shown in Figure 8-1. The `psram_test` is used to generate the address, data, and read/write commands required by Gowin PSRAM Interface IP, and the module can be synthesized. The `Key_debounce` module is a jitter elimination module that is used to eliminate the signal jitter generated by the key or dial switch when it controls the external stimulation.

**Table 8-1 psram\_syn\_top Module Input Ports List**

| Name  | Description                              |
|-------|------------------------------------------|
| clk   | Input reference clock, 50 MHz by default |
| rst_n | Input reset signal                       |

After IP initialization completed, PSRAM\_test automatically cycles read and write operations for different addresses, and each burst length is increased by itself, traversing all burst cases. It analyzes and verifies the read data returned by UHS PSRAM Memory Interface IP, and outputs the error signal. When the error signal is pulled high, it indicates that there is an error code, and vice versa.

# 9 File Delivery

The delivery files for the Gowin UHS PSRAM Memory Interface IP include the document, the design source code, and the reference design.

## 9.1 Document

The document folder contains the user guide in PDF version.

**Table 9-1 Document List**

| Name                                                    | Description                                |
|---------------------------------------------------------|--------------------------------------------|
| IPUG767, Gowin UHS PSRAM Memory Interface IP User Guide | Gowin PSRAM Memory Interface IP User Guide |

## 9.2 Reference Design

The Ref. Design folder contains the netlist file for Gowin UHS PSRAM Memory Interface IP, the user reference design, the constraint file, the jitter elimination module, the top file, the project file folder, etc.

**Table 9-2 Ref. Design Folder**

| Name                          | Description                                      |
|-------------------------------|--------------------------------------------------|
| psram_syn_top.v               | The top module of reference design               |
| key_debounce.v                | Key jitter elimination module                    |
| psram_test.v                  | Test stimulation generation module               |
| UHS_PSRAM_Memory_Interface.vo | Gowin UHS PSRAM Memory Interface IP netlist file |
| psram.cst                     | PSRAM physical constraints file                  |
| psram.sdc                     | PSRAM timing constraints file                    |
| psram.gao                     | Capture PSRAM data                               |
| UHS_PSRAM_Memory_Interface    | PSRAM IP project folder                          |

