Gowin MIPI D-PHY RX TX Advance IP

User Guide

IPUG948-2.3E, 10/15/2026

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Revision History

Date	Version	Description
09/01/2020	1.0E	Initial version published.
04/27/2021	1.1E	The description of D-PHY RX Ports revised.
07/09/2021	1.11E	● The supported device info. improved. ● The Appendix A MIPI D-PHY Data Rates added.
05/16/2023	1.12E	● 3.4 Resource Utilization updated. ● 3.5 Devices Supported updated.
06/08/2023	1.13E	The range of single lane TX line rate modified.
05/22/2024	2.0E	● Supported highest rate updated. ● TX port descriptions updated. ● Supported devices updated.
07/18/2024	2.0.1E	● Descriptions of MIPI IO updated. ● 1.2 Related Documents updated.
10/25/2024	2.0.2E	3.5 Devices Supported updated.
12/13/2024	2.0.3E	3.5 Devices Supported updated.
02/28/2025	2.1E	● 3.5 Devices Supported updated. ● MIPI D-PHY RX Advance IP I/O ports updated. ● 1.2 Related Documents updated.
07/04/2025	2.2E	● int_pll_lock and init_clk added in MIPI D-PHY TX Advance IP. ● PLL Reference Clock parameter added in MIPI D-PHY TX Advance IP. ● Descriptions of "Generation Config" option added. ● The line rate range of the single lane TX/RX updated.
08/08/2025	2.2.1E	Notes have been added below the Table 3-4 D-PHY RX Advance Mode Devices Supported and Table 3-6 D-PHY TX Advance Mode Devices Supported to indicate that some packages do not support MIPI soft IP RX/TX.
10/30/2025	2.2.2E	● Removed the notes below the Table 3-4 D-PHY RX Advance Mode Devices Supported and Table 3-6 D-PHY TX Advance Mode Devices Supported to indicate that some packages do not support MIPI soft IP RX/TX. ● Added the notes below the Table 3-5 D-PHY RX IO Type Devices Supported and Table 3-7 D-PHY TX IO Type Devices Supported to indicate that some packages can not support MIPI IO RX/TX.
03/13/2026	2.2.3E	Added the notes describing the line rate in sections 3.1 Features and 3.2 Max. Frequency.
08/11/2026	2.2.4E	Updated the description of the init_clk port.

Date	Version	Description
10/15/2026	2.3E	● Updated the block diagrams of the MIPI D-PHY RX Advance and TX Advance IPs. ● Updated the port descriptions of the MIPI D-PHY RX Advance and TX Advance IPs. ● Updated chapter 6 Timing Description. ● Updated the GUI screenshots and option descriptions.

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1 About This Guide

1.1 Purpose

The purpose of Gowin MIPI D-PHY RX TX Advance IP User Guide is to help you to quickly learn the features and usage of Gowin MIPI D-PHY RX TX Advance IP by providing the descriptions of the functions, features, ports, timing, configuration, and reference design, etc.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- DS100, GW1N series of FPGA Products Data Sheet
- DS117, GW1NR series of FPGA Products Data Sheet
- DS891, GW1NRF series of FPGA Products Data Sheet
- DS821, GW1NS series of FPGA Products Data Sheet
- DS881, GW1NER series of FPGA Products Data Sheet
- DS861, GW1NSR series of FPGA Products Data Sheet
- DS102, GW2A series of FPGA Products Data Sheet
- DS226, GW2AR series of FPGA Products Data Sheet
- DS961, GW2ANR series of FPGA Products Data Sheet
- DS971, GW2AN-18X and GW2AN-9X Data Sheet
- DS976, GW2AN-55 Data Sheet
- DS981, GW5AT series of FPGA Products Data Sheet
- DS1103, GW5A series of FPGA Products Data Sheet
- DS1239, GW5AST series of FPGA Products Data Sheet
- DS1105, GW5AS series of FPGA Products Data Sheet

- DS1108, GW5AR series of FPGA Products Data Sheet
- DS1118, GW5ART series of FPGA Products Data Sheet
- SUG100, Gowin Software User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
CSI	Camera Serial Interface
DSI	Display Serial Interface
GSR	Global System Reset
IP	Intellectual Property
LUT	Look-up Table
RAM	Random Access Memory

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Introduction to Gowin MIPI D-PHY RX TX Advance IP

Gowin MIPI D-PHY TX RX Advance IP applies to the display serial interface (DSI) and the camera serial interface (CSI). It aims to receive and send images or video data. MIPI D-PHY provides a physical layer definition.

Table 2-1 Gowin MIPI D-PHY RX Advance and TX Advance IP

Gowin MIPI D-PHY RX Advance and TX Advance IP	
Logic Resource	Please refer to Table 3-2 and Table 3-3.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.7.05 Beta and above)

2.2 MIPI D-PHY

The Mobile Industry Processor Interface (MIPI) is an interface standard for mobile devices. MIPI D-PHY provides a physical definition for DSI and CSI and describes the physical layer interface protocols of source synchronous, high speed, and low power. In accordance with applications, MIPI D-PHY Advance includes RX and TX, which are used for receiving or transmitting the data in line with MIPI D-PHY. Figure 2-1 shows the diagram.

MIPI D-HPY typically includes one clock lane and 1~ 4 data lanes. You can configure the number of data lanes using IDE. The clock and data

lanes can switch between 1.2V LVCMOS signal and SLVS-200 differential signal.

MIPI D-PHY supports the following two data modes:

- High-speed (HS) mode
- Low-power (LP) mode

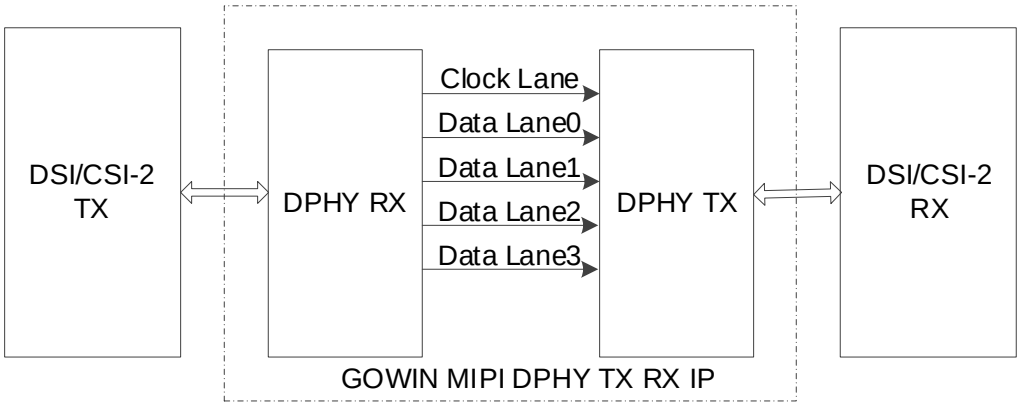
In HS mode, video data is transmitted through differential pair. Depending on the applications, the HS mode can be utilized at all times, or the D-PHY can be switched from HS differential lanes to signal ended signals.

When D-PHY is transmitting single ended signals, it enters to the LP mode.

Note!

- In camera and display applications, the device enters to the LP mode, which reduces power during the blanking period.
- In display applications, LP mode is used for screen configuration.

Figure 2-1 MIPI D-PHY Structure Diagram



3 Features and Performance

3.1 Features

- Compliant with MIPI Alliance Standard for D-PHY Specification, version 1.1
- Supports MIPI DSI and CSI-2 interfaces for TX and RX
- Supports unidirectional high-speed (HS) mode and bidirectional low-power (LP) operation mode for both TX and RX
- Supports 8:1 and 16:1 modes for both TX and RX
- Supports ELVDS, TLVDS, and MIPI I/O types for both TX and RX
- Supports manual IO Delay configuration and automatic IO Delay scanning for RX
- The line rate of the single lane TX ranges from 80 Mb/s to 2000 Mb/s[1]
- The line rate of the single lane RX ranges from 80 Mb/s to 1600 Mb/s[1]
- Supports control data transmission in LP mode at a data rate of 10 Mb/s

Note!

[1]For the line rates supported by different devices, please refer to the device datasheets and *WP1153, Gowin MIPI Solution Capability White Paper*.

3.2 Max. Frequency

The max. frequency of MIPI D-PHY is mainly determined by the line rate[1] and the speed grade of the devices.

Note!

[1]For the line rates supported by different devices, please refer to the device datasheets and *WP1153, Gowin MIPI Solution Capability White Paper*.

3.3 Latency

D-PHY TX Latency is the time from inputting the data_in (8-bit/16-bit parallel data) to outputting HS_DATA.

D-PHY RX Latency is the time from inputting the HS_DATA SOT (start-of-transmission) to outputting data_out (8-bit/16-bit parallel data).

See Table 3-1 for the detailed Latency.

Table 3-1 D-PHY TX RX Advance Latency

Module	Line Rate（Mb/s）	Lane	Latency
D-PHY TX	1200	1	3
D-PHY RX	1200	1	11

3.4 Resource Utilization

MIPI D-PHY RX and TX are implemented via Verilog language. Their performance and resource utilization may vary when the design is employed in a different device, or at a different density, speed, or grade.

Take the GW1N-2 series of FPGA device as an example. See Table 3-2 and Table 3-3 for the MIPI D-PHY RX and TX resource utilization. For the applications on other GOWINSEMI devices, please refer to the later release.

Table 3-2 MIPI D-PHY RX Advance Resource Utilization

Device Series	Speed Grade	Name	Resource Utilization	Remarks
GW1N-2	-6	LUT	477	● 1:8 Mode ● Four HS data lanes included ● Word alignment and lane alignment modules included
		IODELAY	4	
		REG	505	
		BSRAM	0	
		IDES8	4	
		CLKDIV	1	
		DHCEN	1	

Table 3-3 MIPI D-PHY TX Advance Resource Utilization

Device Series	Speed Grade	Name	Resource Utilization	Remarks
GW1N-2	-6	LUT	3	1:8 Mode Internal PLL configured
		REG	0	
		CLKDIV	1	

Device Series	Speed Grade	Name	Resource Utilization	Remarks
		OSER8	5	

3.5 Devices Supported

Table 3-4 D-PHY RX Advance Mode Devices Supported

D-PHY RX Mode	Devices Supported
1:8 Mode	GW1N series, GW1NR series, GW1NS series, GW1NSR series, GW1NSER series, GW1NRF series, GW1AN series, GW2A series, GW2AR series, GW2ANR series, GW2AN series, GW5A series, GW5AT series, GW5AST series, GW5AS series, GW5AR series, GW5ART series, GW3A series, GW1NZ-2B, GW1NZ-2C
1:16 Mode	GW1NS series, GW1NSR series, GW1NSER series, GW5AT series, GW5AST series, GW5A series, GW5AS series, GW5AR series, GW5ART series, GW3A series, GW1N-1S, GW1N-2, GW1N-2B, GW1N-2C, GW1NR-2, GW1NR-2B, GW1NR-2C, GW1N-1P5, GW1N-1P5B, GW1N-1P5C, GW1NR-9, GW1NR-9C, GW1N-9, GW1N-9C, GW1NZ-2B, GW1NZ-2C

Table 3-5 D-PHY RX IO Type Devices Supported

D-PHY RX IO Type	Devices Supported
MIPI IO[1]	GW1NS series, GW1NSR series, GW1NSER series, GW5AT series, GW5A series, GW5AS series, GW5AST series, GW5AR series, GW5ART series, GW3A series, GW1N-9, GW1N-9C, GW1NR-9, GW1NR-9C, GW1N-1P5, GW1N-1P5B, GW1N-1P5C, GW1N-2, GW1N-2B, GW1NR-2, GW1NR-2B, GW1N-2C, GW1NR-2C, GW1NZ-2B, GW1NZ-2C, GW1NR-9, GW1NR-9C, GW1AN-9A, GW2AN-18X, GW2AN-9X
TLVDS IO	All Gowin devices except GW1N-1S, GW1NZ-1, and GW1NZ-1C
ELVDS IO	All Gowin devices

Note!

- [1]MIPI CLK requires GCLK IO when MIPI IO mode is used for GW2AN-18X and GW2AN-9X.
- GW5AT-LV15CS130 can not support MIPI IO RX.

- GW5A-LV25UG324S, GW5A-LV25PG256C, GW5A-LV25UG256C, GW5A-LV25LQ100, GW5A-LV25MG196S, GW5A-LV25PG256S, GW5A-LV25LQ144, GW5A-LV25PG196S can not support MIPI IO RX.
- GW5A-LV60UG324A can not support MIPI IO RX.
- GW5ART-LV15CM90P and GW5ART-LV15CM90PF can not support MIPI IO RX.

Table 3-6 D-PHY TX Advance Mode Devices Supported

D-PHY TX Mode	Devices Supported
8:1 Mode	GW1N series, GW1NR series, GW1NZ series, GW1NS series, GW1NSR series, GW1NSER series, GW1NRF series, GW1AN series, GW2A series, GW2AR series, GW2ANR series, GW2AN series, GW5AT series, GW5A series, GW5AST series, GW5AS series, GW5AR series, GW5ART series, GW3A series
16:1 Mode	GW1NS series, GW1NSR series, GW1NSER series, GW5AT series, GW5ART series, GW5AS series, GW5AST series, GW5A series, GW5AR series, GW3A series, GW1N-1S, GW1N-2, GW1N-2C, GW1N-2B, GW1NR-2, GW1NR-2C, GW1NR-2B, GW1N-1P5, GW1N-1P5B, GW1N-1P5C, GW1NZ-2B, GW1NZ-2C, GW1N-9, GW1N-9C, GW1NR-9, GW1NR-9C

Table 3-7 D-PHY TX IO Type Devices Supported

D-PHY TX IO Type	Devices Supported
MIPI IO	GW1NS series, GW1NSR series, GW1NSER series, GW5AR series, GW5ART series, GW3A series, GW1N-1P5, GW1N-1P5B, GW1N-1P5C, GW1N-2, GW1N-2B, GW1N-2C, GW1NR-2, GW1NR-2B, GW1NR-2C, GW1NR-9, GW1NR-9C, GW1N-9, GW1N-9C, GW1NZ-2B, GW1NZ-2C, GW5A-25A, GW5A-25B, GW5AS-25A, GW5AS-25B, GW5AT-60ES, GW5AT-60B, GW5A-60B, GW5AT-15A
TLVDS IO	All Gowin devices except GW1N-1S, GW1NZ-1, and GW1NZ-1C
ELVDS IO	All Gowin devices

Note！

- GW5AT-LV15CS130 can not support MIPI IO TX.
- GW5A-LV25UG324S, GW5A-LV25PG256C, GW5A-LV25UG256C, GW5A-LV25LQ100, GW5A-LV25MG196S, GW5A-LV25PG256S, GW5A-LV25LQ144, GW5A-LV25PG196S can not support MIPI IO TX.
- GW5A-LV60UG324A can not support MIPI IO TX.
- GW5ART-LV15CM90P and GW5ART-LV15CM90PF can not support MIPI IO TX.

4 Functional Description

MIPI D-PHY contains the following two D-PHY IP modules:

- D-PHY RX Advance
- D-PHY TX Advance

In D-PHY RX Advance and D-PHY TX Advance, HS data is converted to serial-parallel/parallel-serial respectively. The data in LP mode can be transmitted bi-directionally on any data lane or clock lane.

Note!

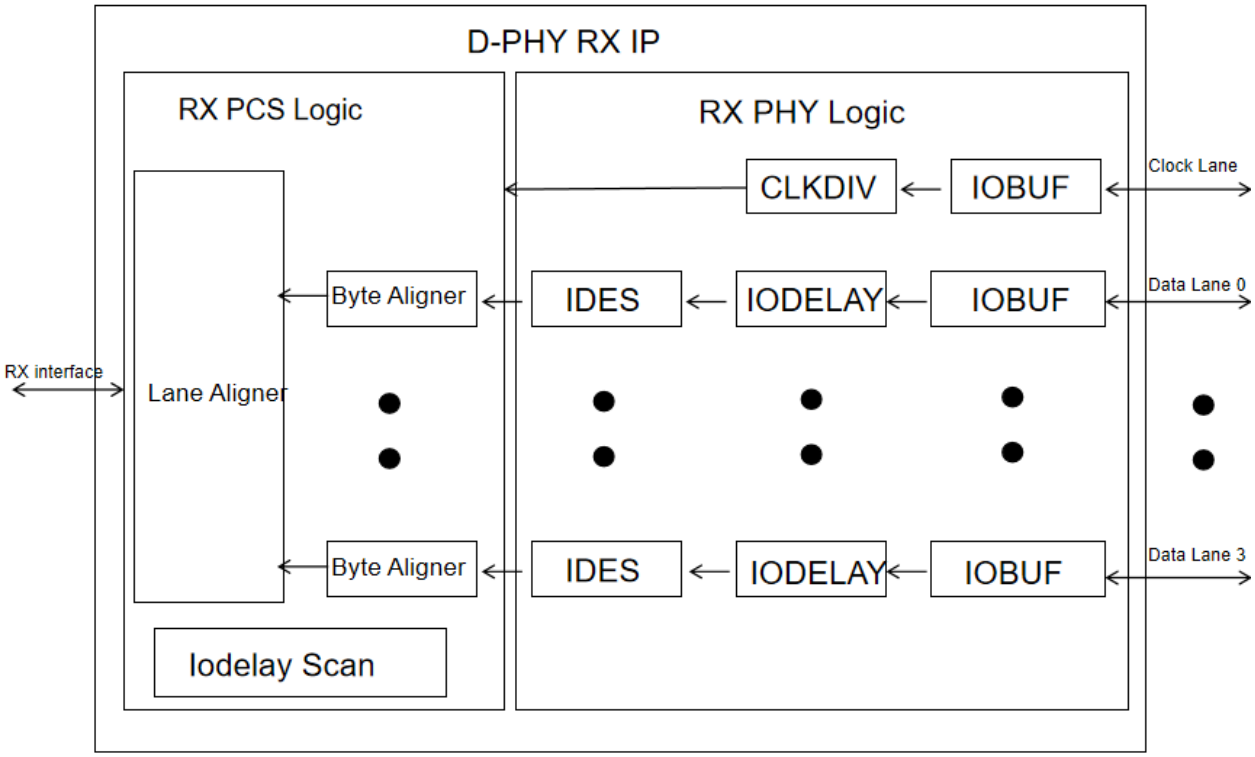
D- PHY RX Advance and D-PHY TX have different resister networks; However, both modules support bi-directional LP communication and unidirectional HS communication.

4.1 MIPI D-PHY RX Advance IP Structure and Function

Figure 4-1 shows the block diagram of the MIPI D-PHY RX Advance IP with the I/O type configured as MIPI, TLVDS, or ELVDS. The design consists of two main modules:

- RX PCS Logic: Provides the RX user interface; performs B8 alignment and lane-to-lane alignment; controls HS/LP switching and ODT enable/disable; and implements IO Delay scanning.
- RX PHY Logic: Performs clock recovery and data deserialization; adjusts the clock-to-data phase; and supports bidirectional LP operation.

Figure 4-1 Block Diagram of the MIPI D-PHY RX Advance IP



When the I/O type is configured as MIPI I/O, each clock or data lane uses one pair of I/Os, and no external resistor network is required. When the I/O type is configured as ELVDS/TLVDS I/O, each clock or data lane uses two pairs of I/Os: one pair for HS operation and the other for LP operation. An external resistor network is also required. For details, refer to *TN100, MIPI Interface Matching Solutions Based on GOWINSEMI FPGA*.

Note!

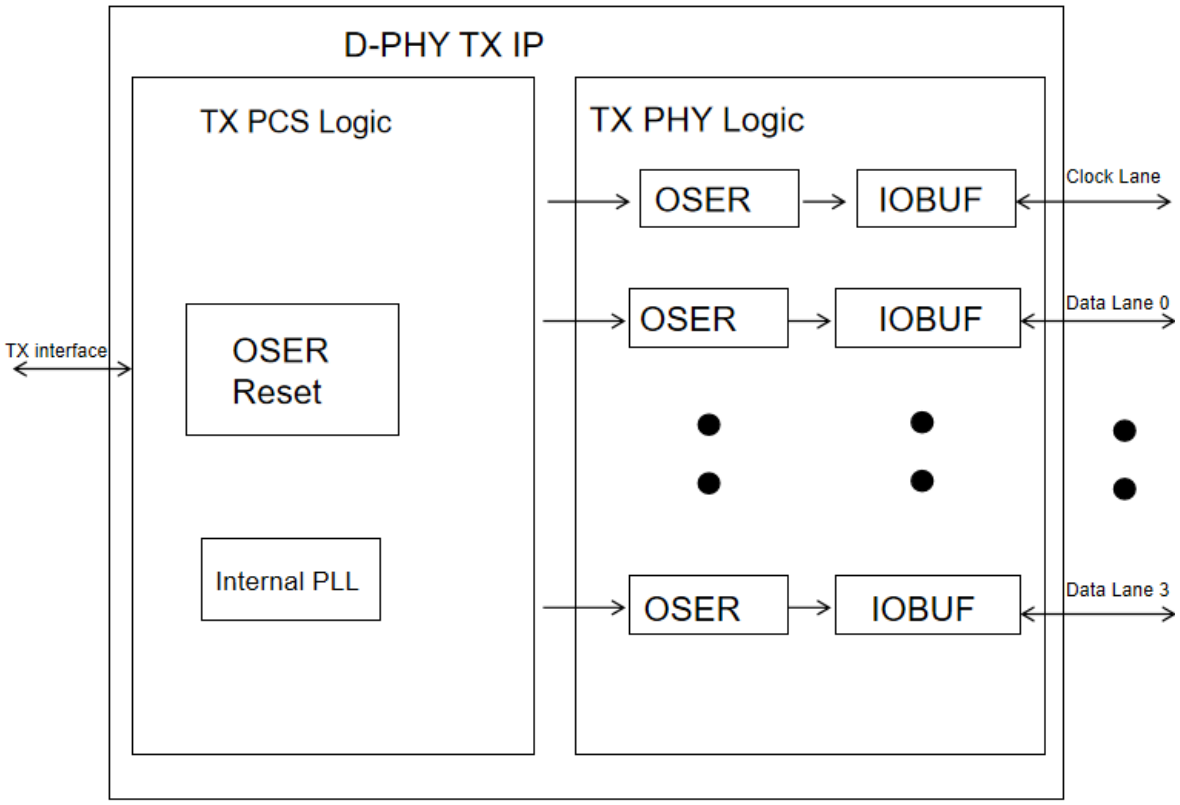
When using 9K and 4K devices, if the bank voltage of the bank containing the D-PHY RX MIPI I/Os is 1.2 V, a 100 Ω matching resistor must be connected between the P and N terminals of MIPI I/O.

4.2 MIPI D-PHY TX Advance IP Structure and Function

Figure 4-2 shows the block diagram of the MIPI D-PHY TX Advance IP with the I/O type configured as MIPI, TLVDS, or ELVDS. The design consists of two main modules:

- TX PCS Logic: Provides the TX user interface, controls HS/LP switching and OSER reset timing, and implements the internal PLL.
- TX PHY Logic: Performs clock and data serialization and supports bidirectional LP operation.

Figure 4-2 Block Diagram of the MIPI D-PHY TX Advance IP



When the I/O type is configured as MIPI I/O, each clock or data lane uses one pair of I/Os, and no external resistor network is required. When the I/O type is configured as ELVDS/TLVDS I/O, each clock or data lane uses two pairs of I/Os: one pair for HS operation and the other for LP operation. An external resistor network is required. For details, refer to *TN100, MIPI Interface Matching Solutions Based on GOWINSEMI FPGA*.

5 Port Description

5.1 MIPI D-PHY RX Advance IP Ports

For the MIPI D-PHY RX Advance IP I/O port descriptions, see Table 5-1.

Table 5-1 D-PHY RX Advance I/O Ports

Signal	I/O	Clock Domain	Description
HS_CLK_P, HS_CLK_N	Input/ Bidirectional (for devices supporting bidirectional LP operation)	N/A	HS signals of the clock lane. ● HS_CLK_P = P wire; HS_CLK_N = N wire. ● Valid when the I/O type of the clock lane is configured as TLVDS or ELVDS.
HS_DATA_P<n>, HS_DATA_N<n>	Input/ Bidirectional (for devices supporting bidirectional LP operation)	N/A	HS signals of data lane <n>. ● HS_DATA_P<n> = P wire; HS_DATA_N<n> = N wire. ● Valid when the I/O type of data lane <n> is configured as TLVDS or ELVDS.
LP_CLK [1:0]	Bidirectional	N/A	LP signals of the clock lane. ● LP_CLK[0] = N wire; LP_CLK[1] = P wire. ● Valid when the I/O type of the clock lane is configured as TLVDS or ELVDS and LP mode is enabled for the clock lane.
LP_DATA<N> [1:0]	Bidirectional	N/A	LP signals of data lane <N>. ● LP_DATA[0] = N wire; LP_DATA[1] = P wire. ● Valid when the I/O type of data lane <N> is configured as TLVDS or ELVDS and LP mode is enabled for the data lane.
MIPI_CLK_P,	Bidirectional	N/A	Signals of the clock lane.

Signal	I/O	Clock Domain	Description
MIPI_CLK_N			● MIPI_CLK_P = P wire; MIPI_CLK_N = N wire. ● Valid when the I/O type of the clock lane is configured as MIPI I/O.
MIPI_LANE<N>_P, MIPI_LANE<N>_N	Bidirectional	N/A	Signals of data lane <N>. ● MIPI_LANE<N>_P = P wire; MIPI_LANE<N>_N = N wire. ● Valid when the I/O type of data lane <N> is configured as MIPI I/O.
reset_n	Input	Async	Reset signal
clk_hs_en	Input	clk_out	Enables HS reception on the clock lane
data_hs_en	Input	clk_out	Enables HS reception on the data lane
data_out<n>	Output	clk_out	HS reception data from data lane <n>. ● The data width is 8 bits when the MIPI D-PHY mode is 1:8. ● The data width is 16 bits when the MIPI D-PHY mode is 1:16.
ready[3:0]	Output	clk_out	Indicates that the parallel data outputs of the data lanes are aligned, active high; ready[n] corresponds to data lane <n>.
clk_term_en	Input	Async	Controls the termination resistor on the clock lane. ● 1: Enables the termination resistor. ● 0: Disables the termination resistor.
data_term_en	Input	Async	Controls the termination resistors on all data lanes. ● 1: Enables the termination resistors. ● 0: Disables the termination resistors.
lp_clk_dir	Input	Async	Controls the LP direction of the clock lane. ● '0': Receive. ● '1': Transmit.
lp_data<n>_dir	Input	Async	Controls the LP direction of data lane <n>. ● '0': Receive. ● '1': Transmit.
lp_clk_out [1:0]	Output	Async	LP receive data from the clock lane. ● lp_clk_out[0] = N wire. ● lp_clk_out[1] = P wire.
lp_data<n>_out [1:0]	Output	Async	LP receive data from data lane <n>. ● lp_data<n>_out[0] = N wire. ● lp_data<n>_out[1] = P wire.

Signal	I/O	Clock Domain	Description
lp_clk_in [1:0]	Input	Async	LP transmit data for the clock lane. ● lp_clk_in[0] = N wire; ● lp_clk_in[1] = P wire.
lp_data<n>_in [1:0]	Input	Async	LP transmit data for data lane <n>. ● lp_data<n>_in[0] = N wire; ● lp_data<n>_in[1] = P wire.
lane<n>_iodelay	Output	clk_byte_out	I/O Delay scan value for data lane <n>.
lane<n>_iodelay_lock	Output	clk_byte_out	Indicates that the I/O Delay scan value for data lane <n> is locked, active high.
data_bf_lane<n>	Output	clk_byte_out	HS reception data from data lane <n> before byte alignment. Used to observe the raw HS data sampled by the OSER when "Data<n> Before Alignment" is enabled.

Note!

The value of <n> ranges from 0 to 3.

5.2 MIPI D-PHY TX Advance IP Ports

For MIPI D-PHY TX Advance IP I/O ports descriptions, see Table 5-2.

Table 5-2 D-PHY TX Advance I/O Ports

Signal	I/O	Clock Domain	Description
HS_CLK_P, HS_CLK_N	Output	N/A	HS signals of the clock lane. ● HS_CLK_P = P wire; HS_CLK_N = N wire. ● Valid when the I/O type of the clock lane is configured as TLVDS or ELVDS.
HS_DATA_P<n>, HS_DATA_N<n>	Output	N/A	HS signals of data lane <n>. ● HS_DATA_P = P wire; HS_DATA_N = N wire. ● Valid when the I/O type of data lane <n> is configured as TLVDS or ELVDS.
LP_CLK [1:0]	Bidirectional	N/A	LP signals of the clock lane. ● LP_CLK[0] = N wire; LP_CLK[1] = P wire. ● Valid when the I/O type of the

Signal	I/O	Clock Domain	Description
			clock lane is configured as TLVDS or ELVDS and LP mode is enabled for the clock lane.
LP_DATA<N>[1:0]	Bidirectional	N/A	LP signals of the data lane. ● LP_DATA<N>[0] = N wire; LP_DATA<N>[1] = P wire. ● Valid when the I/O type of the data lane is configured as TLVDS or ELVDS and LP mode is enabled for the data lane.
MIPI_CLK_P, MIPI_CLK_N	Output/ Bidirectional (for devices supporting bidirectional LP operation)	N/A	Signals of the clock lane. ● MIPI_CLK_P = P wire; MIPI_CLK_N = N wire. ● Valid when the I/O type of the clock lane is configured as MIPI I/O.
MIPI_LANE<N>_P, MIPI_LANE<N>_N	Bidirectional	N/A	Signals of data lane <N>. ● MIPI_LANE<N>_P = P wire; MIPI_LANE<N>_N = N wire. ● Valid when the I/O type of the data lane is configured as MIPI I/O.
reset_n	Input	Async	Reset signal, active low.
sclk_in	Input	N/A	HS parallel clock input. ● In 8:1 mode, the frequency is the lane rate divided by 8. In 16:1 mode, the frequency is the lane rate divided by 16. ● When the embedded PLL is disabled, this signal must be connected to sclk_out of a MIPI TX IP with the embedded PLL enabled.
sclk_out	Output	N/A	● HS parallel clock output. Can be connected to sclk_in of a MIPI TX IP with the embedded PLL disabled. ● Valid when the embedded PLL is enabled.
clk_bit_out	Output	N/A	● HS serial clock output, in phase

Signal	I/O	Clock Domain	Description
			with sclk_out. Can be connected to clk_bit_in of a MIPI TX IP with the embedded PLL disabled. ● Valid when the embedded PLL is enabled.
clk_bit_90_out	Output	N/A	● HS serial clock output, with a 90° phase difference relative to clk_bit_out. Can be connected to clk_bit_90_in of a MIPI TX IP with the embedded PLL disabled. ● Valid when the embedded PLL is enabled.
clk_bit_in	Input	N/A	● HS serial clock input. Must be connected to clk_bit_out of a MIPI TX IP with the embedded PLL enabled. ● Valid when the embedded PLL is disabled.
clk_bit_90_in	Input	N/A	● HS serial clock input. Must be connected to clk_bit_90_out of a MIPI TX IP with the embedded PLL enabled. ● Valid when the embedded PLL is disabled.
init_clk	Input	N/A	When the embedded PLL is enabled, this signal serves as the MDCLK input to the embedded PLL. This signal is supported only on Arora V devices.
hs_clk_en	Input	sclk	Enables HS transmission on the clock lane.
hs_data_en	Input	sclk	Enables HS transmission on all data lanes.
lp_clk_dir	Input	Async	Controls the LP direction of the clock lane. ● '0': Receive ● '1': Transmit
lp_clk_out [1:0]	Input	Async	LP transmit data for the clock lane. ● lp_clk_out[0] = N wire;

Signal	I/O	Clock Domain	Description
			lp_clk_out[1] = P wire.
lp_clk_in [1:0]	Output	Async	LP receive data from the clock lane. ● lp_clk_in[0] = N wire; ● lp_clk_in[1] = P wire.
lp_data<n>_dir	Input	Async	Controls the LP direction of data lane <n>. ● '0': Receive ● '1': Transmit
lp_data<n>_out [1:0]	Input	Async	LP transmit data for data lane <n>. ● lp_data<n>_out[0] = N wire; ● lp_data<n>_out[1] = P wire.
lp_data<n>_in[1:0]	Output	Async	LP receive data from data lane <n>. ● lp_data<n>_in[0] = N wire; ● lp_data<n>_in[1] = P wire.
clk_data	Input	sclk	HS data for the clock lane. ● In MIPI D-PHY 8:1 mode, the data width is 8 bits, for example, 8'b01010101. ● In MIPI D-PHY 16:1 mode, the data width is 16 bits, for example, 16'b0101010101010101.
data_in<n>	Input	sclk	HS transmit data for data lane <n>. ● In MIPI D-PHY 8:1 mode, the data width is 8 bits. ● In MIPI D-PHY 16:1 mode, the data width is 16 bits.

Note!

- The value of <n> ranges from 0 to 3.
- When the embedded PLL is enabled, sclk refers to sclk_out; otherwise, sclk refers to sclk_in.

6 Timing Description

This section describes the input signal timing of MIPI D-PHY RX Advance and TX Advance in HS mode.

6.1 MIPI D-PHY RX Advance User Interface Timing

6.1.1 Reset

MIPI D-PHY RX Advance uses reset_n as the reset signal, active-low.

6.1.2 LP Reception

Figure 6-1 shows the LP reception timing diagram for the RX Advance Clock Lane. During LP reception, the user must set lp_clk_dir, clk_term_en, and clk_hs_en to 0. The lp_clk_out signal is an output from the IP and indicates the current Clock Lane State.

Figure 6-1 Clock Lane LP Reception for RX Advance

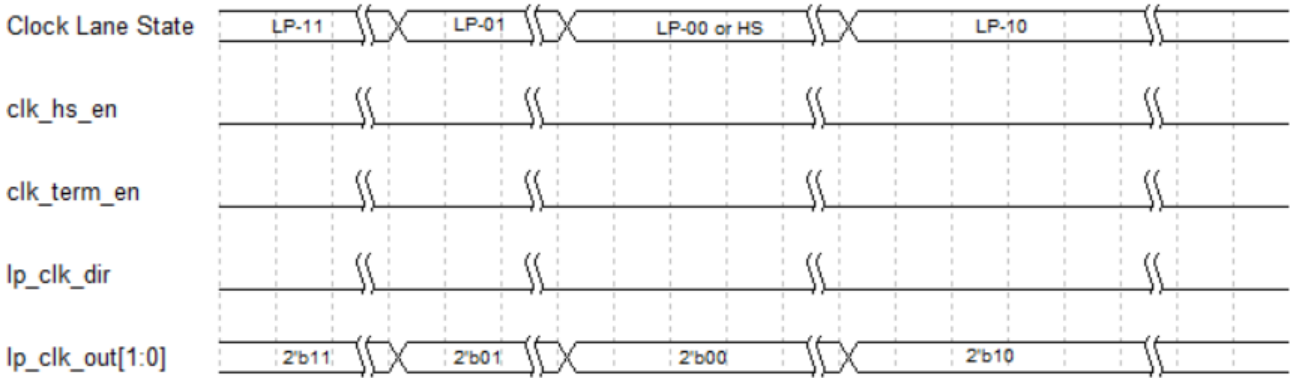
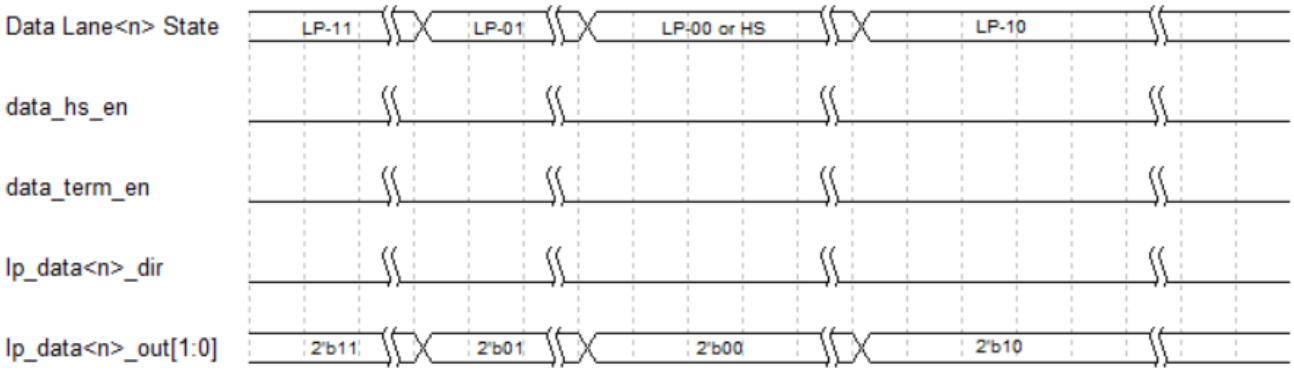


Figure 6-2 shows the LP reception timing diagram for the RX Advance Data Lane. During LP reception, the user must set lp_data<n>_dir, data_term_en, and data_hs_en to 0. The lp_data<n>_out signal is an output from the IP and indicates the current State of Data Lane <n>.

Figure 6-2 Data Lane LP Reception for RX Advance



6.1.3 LP Transmission

Figure 6-3 shows the LP transmission timing diagram for the RX Advance Clock Lane. During LP transmission, the user must set lp_clk_dir to 1, set lp_clk_in to the Lane State to be transmitted, and set clk_term_en and clk_hs_en to 0. RX Advance drives the Clock Lane to the corresponding Clock Lane State according to the value of lp_clk_in.

Figure 6-3 Clock Lane LP Transmission for RX Advance

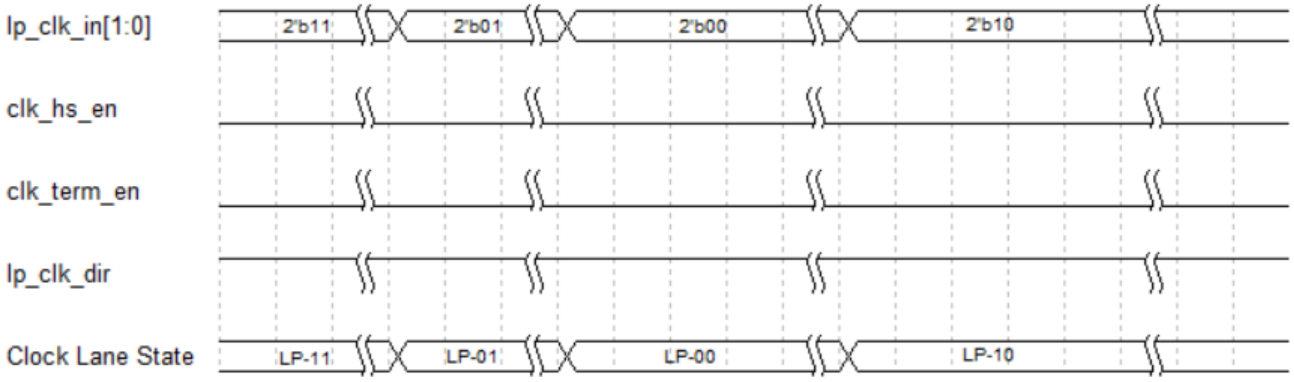
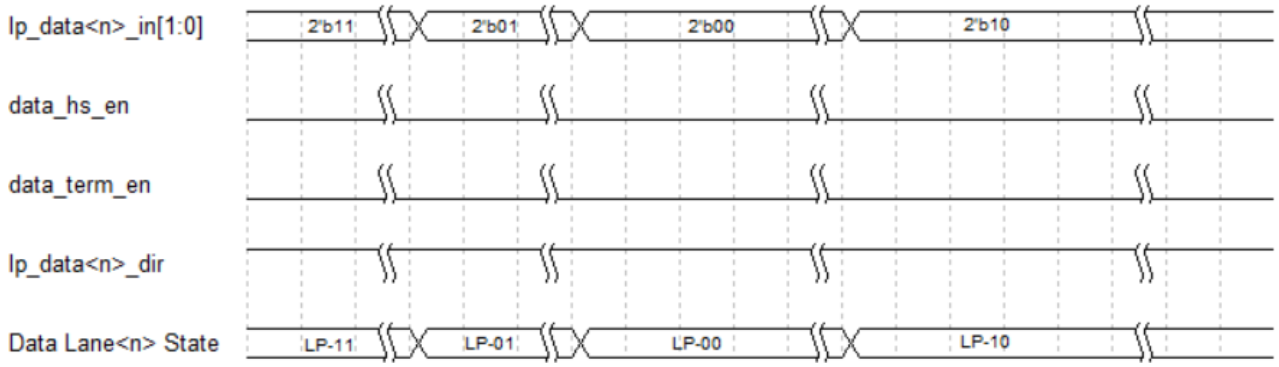


Figure 6-4 shows the LP transmission timing diagram for the RX Advance Data Lane. During LP transmission, the user must set lp_data<n>_dir to 1, set lp_data<n>_in to the Lane State to be transmitted, and set data_term_en and data_hs_en to 0. RX Advance drives Data Lane <n> to the corresponding Data Lane State according to the value of lp_data<n>_in.

Figure 6-4 Data Lane LP Transmission for RX Advance



6.1.4 HS Reception

Figure 6-5 shows the HS reception timing diagram for the RX Advance Clock Lane. During HS reception, the user must set clk_hs_en and clk_term_en to 1.

Figure 6-5 Clock Lane HS Reception for RX Advance

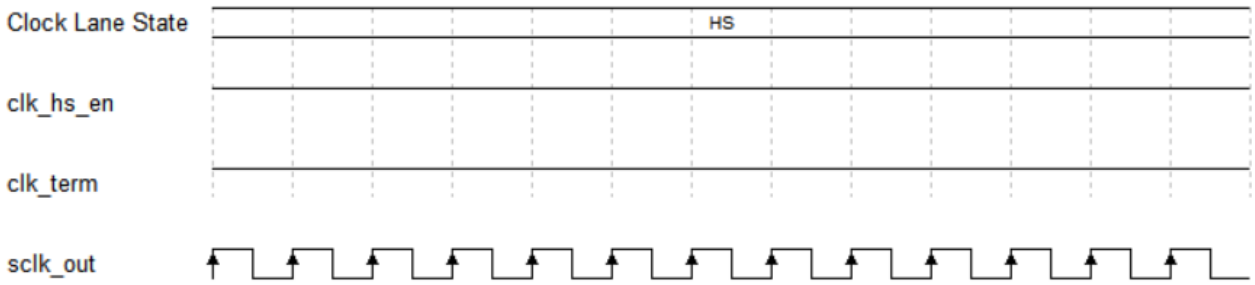
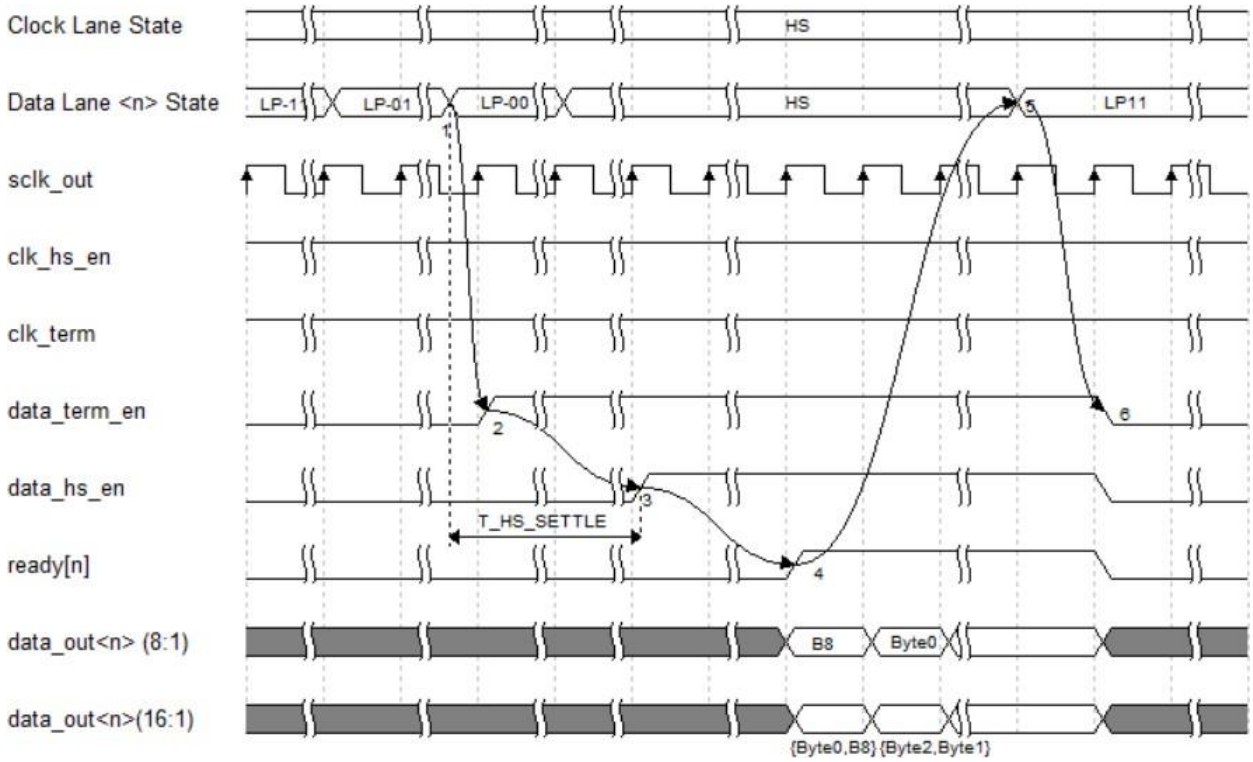


Figure 6-6 shows the HS reception timing diagram for the MIPI D-PHY RX Advance Data Lane.

1. The transmitter drives Data Lane <n> to LP-00.
2. The user sets data_term_en to 1.
3. After waiting for T_HS_SETTLE period, the user sets data_hs_en to 1.
4. If Byte Alignment is enabled, RX Advance sets ready[n] to 1 and outputs the aligned data on data_out_<n>. Otherwise, RX Advance outputs the unaligned data on data_out_<n>.
5. The transmitter drives Data Lane <n> to LP-11.
6. The user sets data_term_en and data_hs_en to 0.

Figure 6-6 Data Lane HS Reception for RX Advance



6.1.5 Byte Alignment

If Byte Alignment is enabled, RX Advance searches for B8 during the HS phase. Once B8 is successfully detected, the data is aligned, ready[n] is set to 1, and the aligned data is output on data_out_<n>. If B8 is not detected, ready[n] remains 0 and no data is output.

If Byte Alignment is disabled, RX Advance outputs the received HS data directly on data_out_<n> without alignment.

6.1.6 Lane Alignment

If Lane Alignment is enabled, RX Advance waits until all data lanes have completed alignment. It then sets the ready signals for all lanes to 1 simultaneously and outputs the aligned data. If alignment fails on any data lane, no data is output on any data lane.

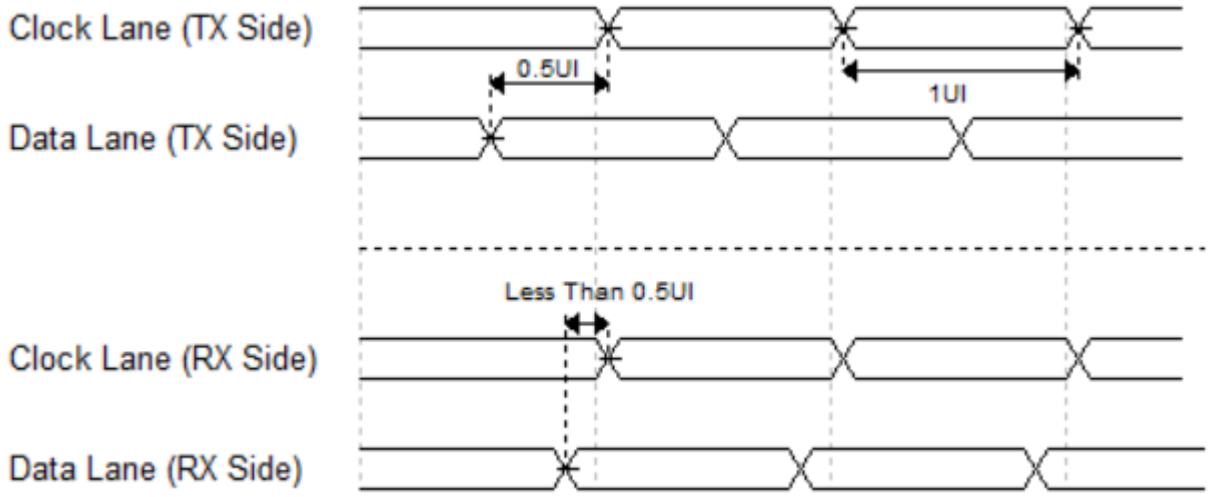
RX Advance provides two Lane Alignment modes: Standard and Lite. Standard is the commonly used Lane Alignment mode, while Lite is suitable for scenarios with limited logic resources.

6.1.7 Phase Calibration

According to the protocol, the TX Clock Lane and Data Lanes maintain a 90° phase relationship. On the RX side, differences in PCB trace lengths,

internal RX delays, and other factors can cause phase offsets between the Clock Lane and Data Lanes. Without phase calibration, these offsets may result in reception errors, as shown in Figure 6-7.

Figure 6-7 Clock Phase Offset

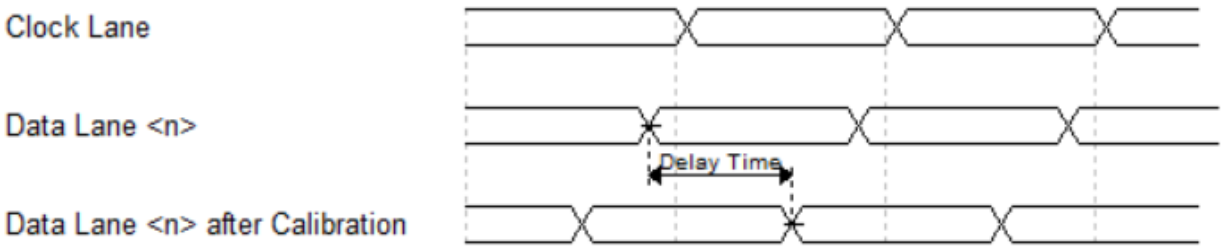


RX Advance provides two phase calibration methods: static IO Delay adjustment and IO Delay Scan. For static IO Delay adjustment, the user calibrates the phase by modifying "Calibration > HS Data <n> IO Delay Value" in the GUI. The relationship between HS Data <n> IO Delay Value and the actual delay is shown in Table 6-1. The clock-to-data phase relationship after calibration is shown in Figure 6-8.

Table 6-1 Relationship Between HS Data <n> IO Delay Value and Actual Delay

Device Family	Data Lane <n> Delay Time (ps)
GW1N	HS Data <n> IO Delay Value * 30
GW2AN-18	HS Data <n> IO Delay Value * 18
GW2AN-55	HS Data <n> IO Delay Value * 22
Arora V	HS Data <n> IO Delay Value * 12.5
Arora III	HS Data <n> IO Delay Value * 12.5

Figure 6-8 Clock-to-Data Phase Relationship After Calibration



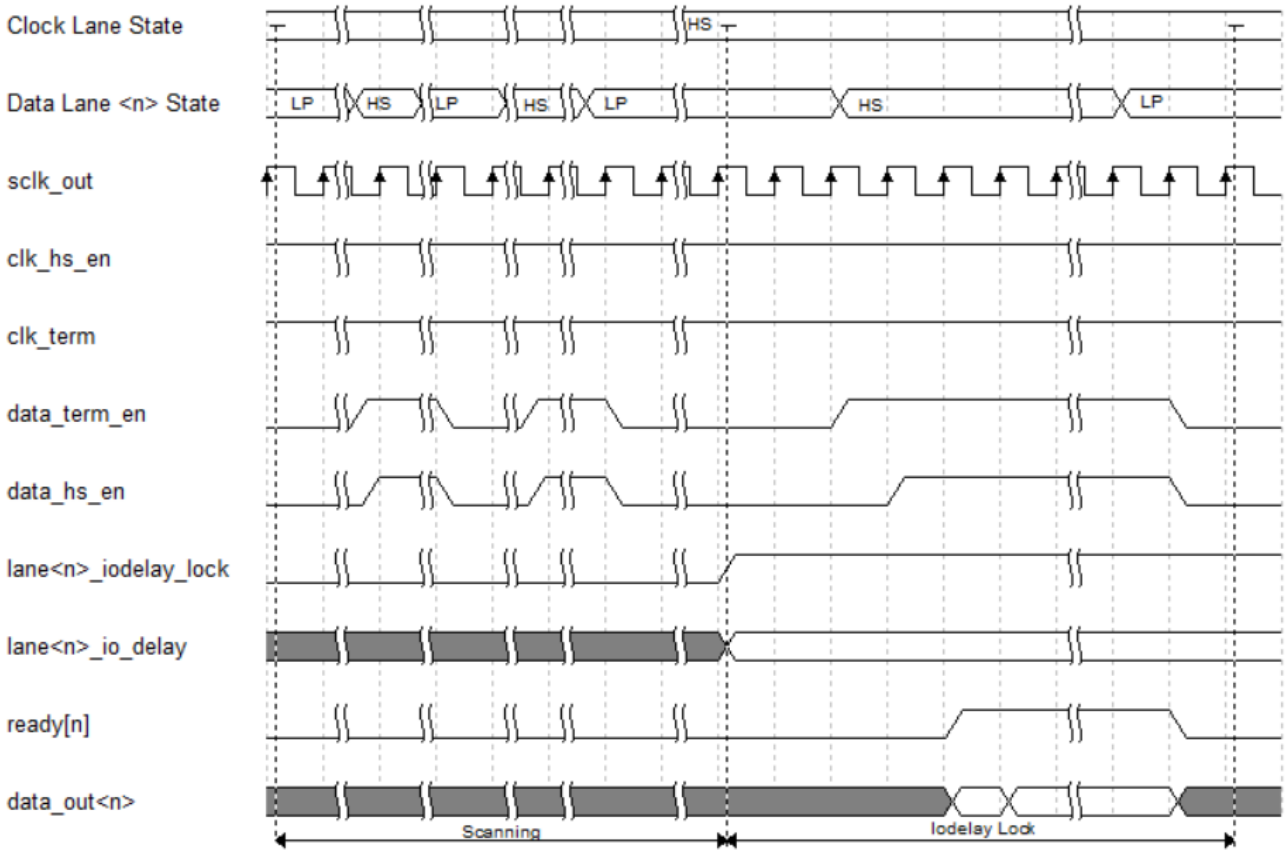
RX Advance also provides IO Delay Scan for automatic phase calibration. When IO Delay Scan is enabled, the timing is as shown in Figure 6-9. During the scan, the user must control the relevant signals to perform HS reception. For details, see section 6.1.4 HS Reception.

RX Advance automatically performs phase calibration once after each reset is completed. At the start of the scan, RX Advance sets lane<n>_iodelay_lock to 0 and initializes HS Data <n> IO Delay Value to 0. It then checks whether B8 is successfully detected at the current delay value. RX Advance subsequently increments HS Data <n> IO Delay Value by 1 at each step and checks whether B8 is successfully detected at each delay value.

The first value at which B8 is successfully detected is recorded as Value_a, and the last value at which B8 is successfully detected is recorded as Value_b. After the scan is complete, RX Advance sets lane<n>_iodelay to the midpoint between Value_a and Value_b and sets lane<n>_iodelay_lock to 1.

When IO Delay Scan is enabled, ready[n] is set to 1 only after lane<n>_iodelay_lock becomes 1.

Figure 6-9 RX Advance IO Delay Scan



6.2 MIPI D-PHY TX Advance User Interface Timing

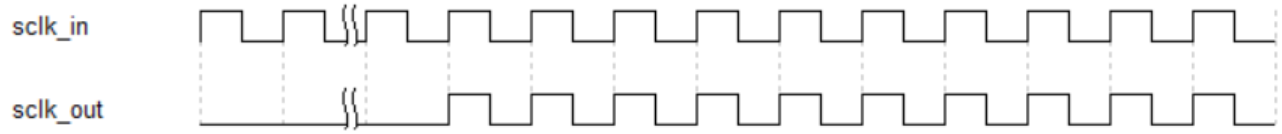
6.2.1 TX Reset

MIPI D-PHY TX Advance uses reset_n as the reset signal, active low.

6.2.2 Clock

MIPI D-PHY TX Advance can be configured to use or bypass the embedded PLL. Figure 6-10 shows the timing diagram with the embedded PLL enabled.

Figure 6-10 Embedded PLL Enabled



6.2.3 LP Transmission

Figure 6-11 shows the LP transmission timing diagram for the TX Advance Clock Lane. During LP transmission, the user sets clk_hs_en to 0

and lp_clk_dir to 1. The lp_clk_out signal is an output from the IP and indicates the current Clock Lane State. TX Advance drives the Clock Lane to the corresponding LP State according to the control signals.

Figure 6-11 Clock Lane LP Transmission for TX Advance

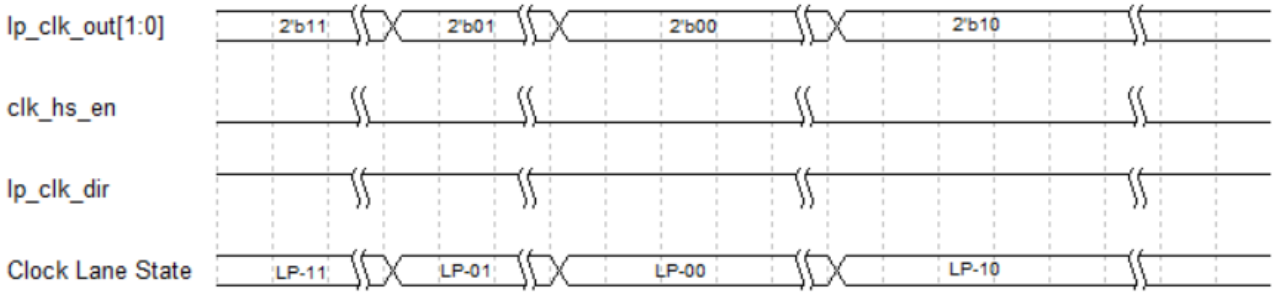
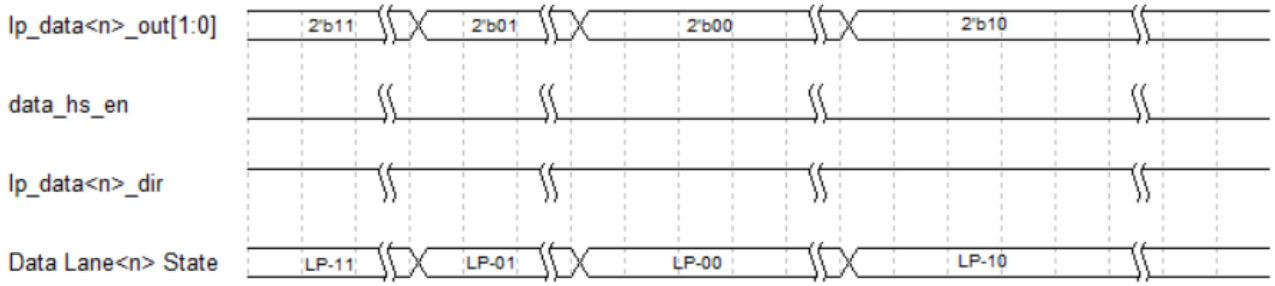


Figure 6-12 shows the LP transmission timing diagram for the TX Advance Data Lane. During LP transmission, the user sets data_hs_en to 0 and lp_data<n>_dir to 1. The lp_data<n>_out signal is an output from the IP and indicates the current State of Data Lane <n>. TX Advance drives Data Lane <n> to the corresponding LP State according to the control signals.

Figure 6-12 Data Lane LP Transmission for TX Advance



6.2.4 LP Reception

Figure 6-13 shows the LP reception timing diagram for the TX Advance Clock Lane. During LP reception, the user sets clk_hs_en and lp_clk_dir to 0. TX Advance outputs the Clock Lane State on lp_clk_in.

Figure 6-13 Clock Lane LP Reception for TX Advance

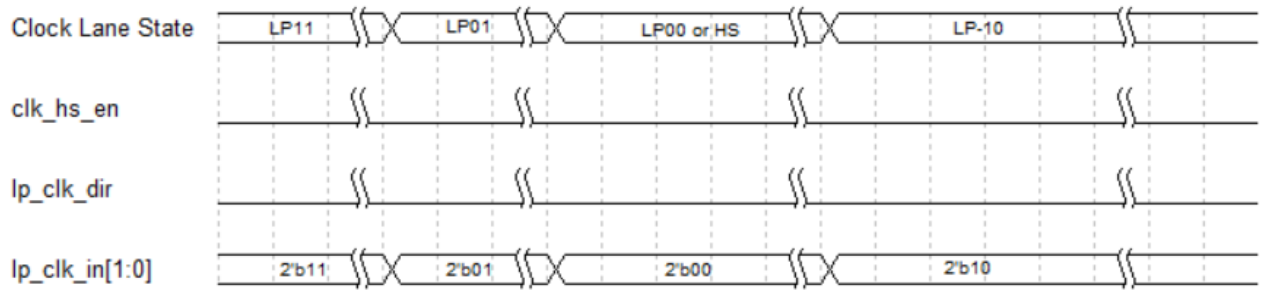
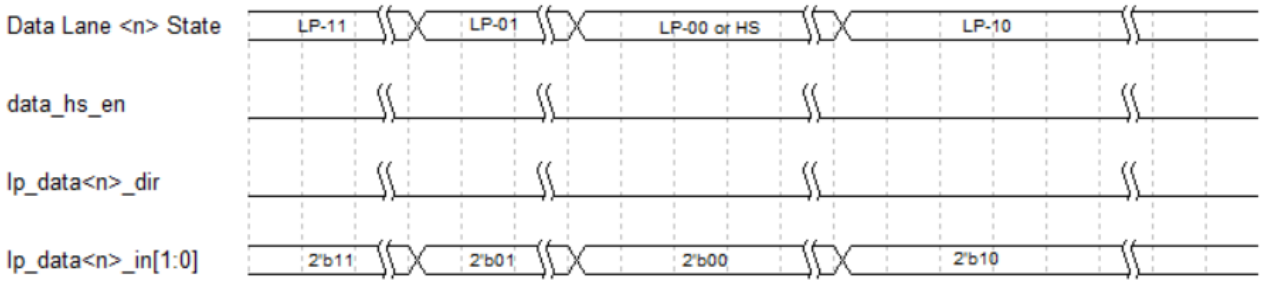


Figure 6-14 shows the LP reception timing diagram for the TX Advance Data Lane. During LP reception, the user sets data_hs_en and lp_data<n>_dir to 0. TX Advance outputs the State of Data Lane <n> on lp_data<n>_in.

Figure 6-14 Data Lane LP Reception for TX Advance

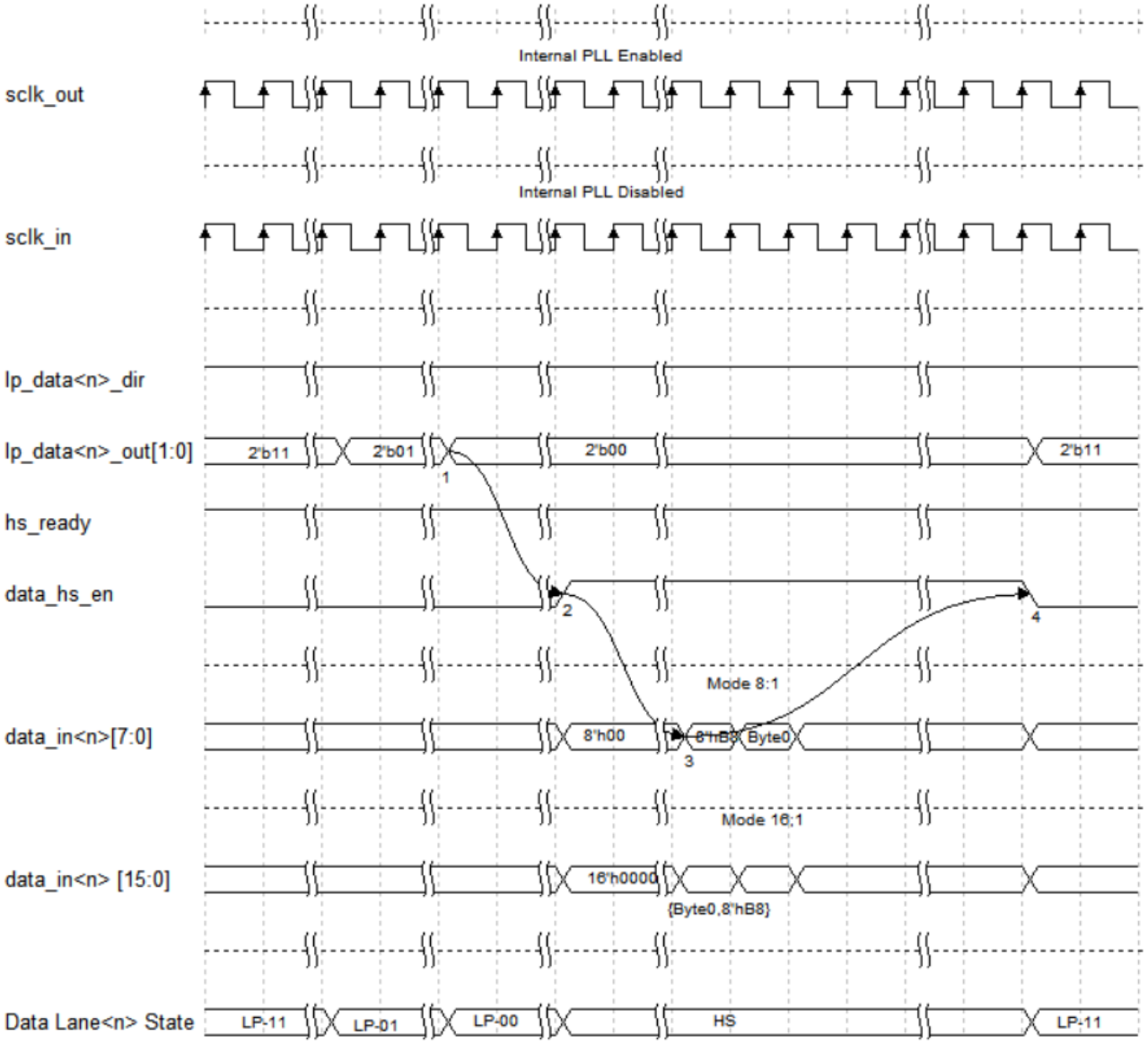


6.2.5 HS Transmission

Figure 6-15 shows the HS transmission timing diagram for the TX Advance Data Lane.

1. The user sets lp_data<n>_out to 2'b00. TX Advance drives Data Lane <n> to LP-00.
2. The user sets data_hs_en to 1 and sets data_in<n> to 8'h00 (in 8:1 mode) or 16'h0000 (in 16:1 mode). TX Advance drives Data Lane <n> to HS-0.
3. The user sets data_in<n> to the HS data to be transmitted. TX Advance outputs the HS data on Data Lane <n>.
4. The user sets data_hs_en to 0 and lp_data<n>_out to 2'b11. TX Advance drives Data Lane <n> to LP-11.

Figure 6-15 Data Lane HS Transmission for TX Advance



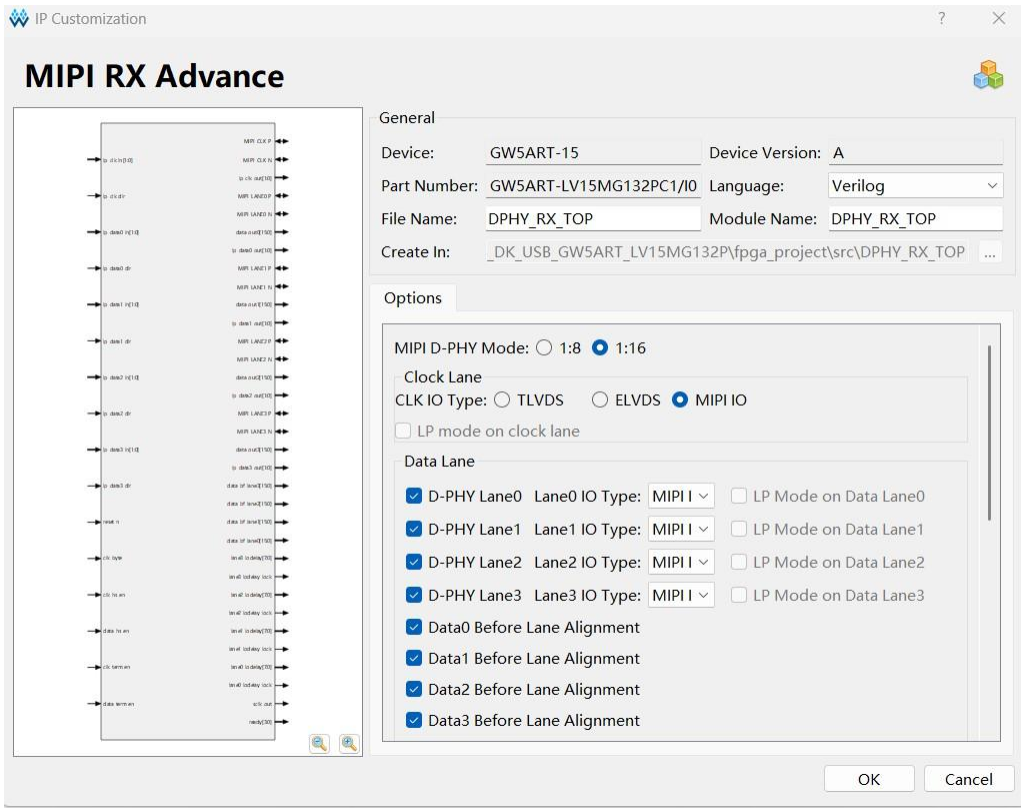
7 Configuration and Generation

Start "IP Core Generator" from the "Tools" menu in the Gowin software and then configure and generate the MIPI D-PHY RX and MIPI D-PHY TX Advance.

7.1 MIPI D-PHY RX Advance Configuration

The configuration options for MIPI D-PHY RX Advance are shown in Figure 7-1.

Figure 7-1 MIPI D-PHY RX Advance Configuration



1. Name the MIPI D-PHY RX Advance by modifying the "File Name" text

box.

2. Create the Advance top module name of MIPI D-PHY RX Advance by modifying "Module Name" text box.
3. Configure the number of HS data lane, the clock and data lane in LP mode, and the byte alignment or lane alignment through "Options". Table 7-1 lists the detailed configuration.
4. Only one HS clock lane and one HS clock lane are used by default.

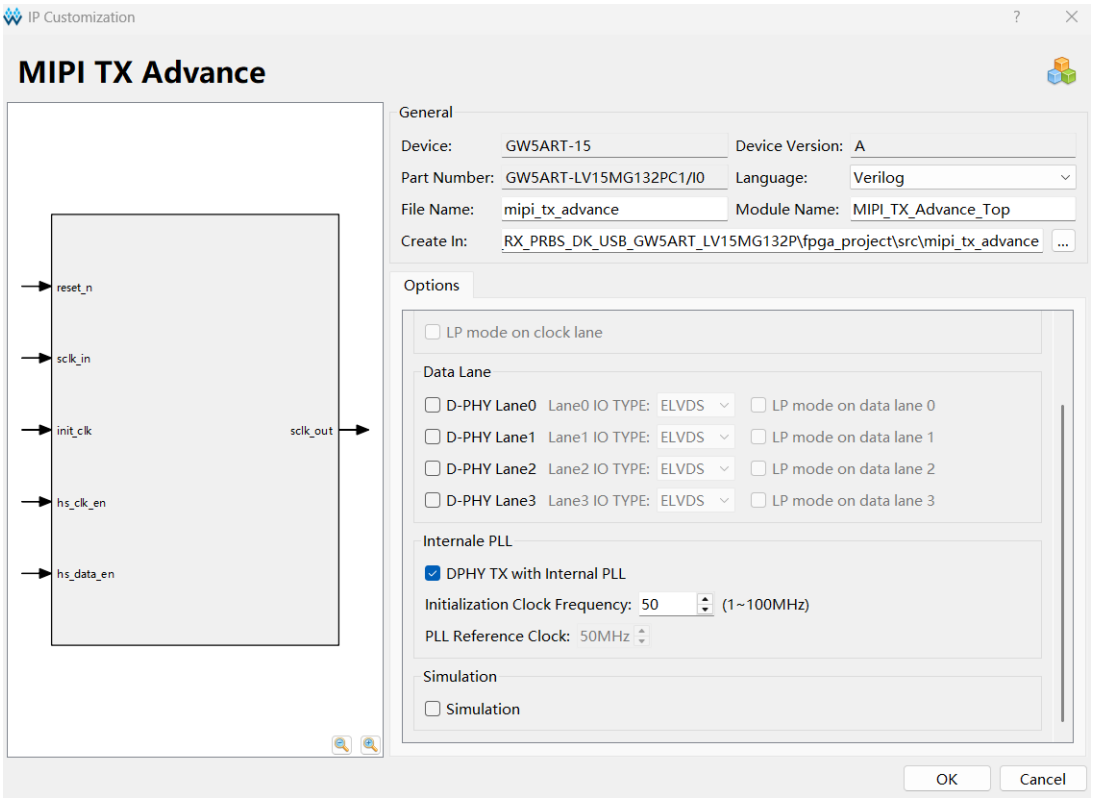
Table 7-1 MIPI D-PHY RX Advance Options

Options	Description
MIPI D-PHY Mode	Select the data mode 1:8 or 1:16.
CLK IO Type	Select the I/O type for the Clock Lane: ELVDS, TLVDS, or MIPI I/O.
D-PHY Lane[n]	Enable Data Lane [n].
Lane[n] IO Type	Select the I/O type for Data Lane [n]: ELVDS, TLVDS, or MIPI I/O.
LP Mode on Data Lane[n]	Enable LP mode on Data Lane [n]. This option is available only when the I/O type of Data Lane [n] is set to ELVDS or TLVDS.
Data[n] Before Lane Alignment	The data from Data Lane [n] before byte alignment. This option can be used to observe the raw data sampled by the IDES.
Turns On Lane Alignment	Enable Lane Alignment across data lanes. When this option is selected, byte alignment is automatically enabled for the data lanes.
Turns On Lane[n] Byte Alignment	Enable byte alignment for Data Lane [n].
Lane[n] IO Delay Scan Enable	Enable IO Delay Scan for Data Lane [n].
HS Data[n] IO Delay Value	Configure the IO delay for Data Lane [n]. This value can be configured only when IO Delay Scan for Data Lane [n] is disabled.
Simulation	Enable simulation. When this option is selected, the generated .vo file can be used for simulation. Clear this option when using the generated IP in a design project.

7.2 MIPI D-PHY TX Advance Configuration

The configuration options for MIPI D-PHY TX Advance are shown in Figure 7-2.

Figure 7-2 MIPI D-PHY TX Advance Configuration



1. Name the MIPI D-PHY TX Advance by modifying the "File Name" text box.
2. Create the Advance top module name of MIPI D-PHY TX Advance by modifying "Module Name" text box.
3. Configure the number of HS data lane, whether the clock and data lane in LP mode use the internal PLL or not through "Options". Table 7-2 lists the detailed configuration.
4. Only one HS clock lane and one HS clock lane are used by default.

Table 7-2 MIPI D-PHY TX Advance Options

Options	Description
MIPI D-PHY Mode	Select the data mode 1:8 or 1:16.
D-PHY CLK	Enable the HS Clock Lane
CLK IO Type	Select the I/O type for the Clock Lane: ELVDS, TLVDS, or MIPI I/O.

Options	Description
LP mode on clock mode	Enable LP mode on the Clock Lane. This option is available only when the Clock Lane I/O type is set to ELVDS or TLVDS.
D-PHY Lane[n]	Enable Data Lane [n].
Lane[n] IO Type	Select the I/O type for Data Lane [n]: ELVDS, TLVDS, or MIPI I/O.
LP mode on data lane [n]	Enable LP mode on Data Lane [n]. This option is available only when the I/O type of Data Lane [n] is set to ELVDS or TLVDS.
D-PHY TX with Internal PLL	Enable the internal PLL.
PLL Reference Clock	Specify the input clock frequency of the internal PLL.

Appendix A MIPI D-PHY Data Rates

Table A-1 MIPI D-PHY Data Rates (LittleBee Family)

Resolution	Frame Rate (HZ)	Bits Per Pixel (Bits)	Total Data Rate (Mbps)	Lane Number	Per Lane Bit Rate (Mbps)	Recommended Gearing Ratio (1:N)	Per Lane Fabric Clock (MHz)
FHD 1920x1080p (2200x1125)	60	8	1188	2	594.0	8	74.25
		10	1485	2	742.5	8	92.81
		16	2376	2	1188.0	16	74.25
		18	2673	4	668.3	8	83.53
		24	3564	4	891.0	8	111.38
	120	8	2376	2	1188.0	16	74.25
		10	2970	4	742.5	8	92.81
		16	4752	4	1188.0	16	74.25
		18	5346	8	668.3	8	83.53
		24	7128	8	891.0	8	111.38
UHD 3840x2160p (4400x2250)	30	8	2376	4	594.0	8	74.25
		10	2970	4	742.5	8	92.81
		16	4752	4	1188.0	16	74.25
		18	5346	8	668.3	8	83.53
		24	7128	8	891.0	8	111.38
	60	8	4752	4	1188.0	16	74.25
		10	5940	8	742.5	8	92.81
		16	9504	8	1188.0	16	74.25

Table A-2 MIPI D-PHY Data Rates (Arora Family)

Resolution	Frame Rate (HZ)	Bits Per Pixel (Bits)	Total Data Rate (Mbps)	Lane Number	Per Lane Bit Rate (Mbps)	Recommended Gearing Ratio (1:N)	Per Lane Fabric Clock (MHz)
FHD 1920x1080p (2200x1125)	60	8	1188	2	594.0	8	74.25
		10	1485	2	742.5	8	92.81
		16	2376	2	1188.0	8	148.50
		18	2673	4	668.3	8	83.53
		24	3564	4	891.0	8	111.38
	120	8	2376	2	1188.0	8	148.50
		10	2970	4	742.5	8	92.81
		16	4752	4	1188.0	8	148.50
		18	5346	8	668.3	8	83.53
		24	7128	8	891.0	8	111.38
UHD 3840x2160p (4400x2250)	30	8	2376	4	594.0	8	74.25
		10	2970	4	742.5	8	92.81
		16	4752	4	1188.0	8	148.50
		18	5346	8	668.3	8	83.53
		24	7128	8	891.0	8	111.38
	60	8	4752	4	1188.0	8	148.50
		10	5940	8	742.5	8	92.81
		16	9504	8	1188.0	8	148.50


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