



# Gowin MIPI D-PHY RX TX Advance IP User Guide

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## Revision History

Date	Version	Description
09/01/2020	1.0E	Initial version published.
04/27/2021	1.1E	The description of D-PHY RX Ports revised.
07/09/2021	1.11E	<ul style="list-style-type: none"> <li>● The supported device info. improved.</li> <li>● The Appendix A MIPI D-PHY Data Rates added.</li> </ul>
05/16/2023	1.12E	<ul style="list-style-type: none"> <li>● 3.4 Resource Utilization updated.</li> <li>● 3.5 Devices Supported updated.</li> </ul>
06/08/2023	1.13E	The range of single lane TX line rate modified.
05/22/2024	2.0E	<ul style="list-style-type: none"> <li>● Supported highest rate updated.</li> <li>● TX port descriptions updated.</li> <li>● Supported devices updated.</li> </ul>
07/18/2024	2.0.1E	<ul style="list-style-type: none"> <li>● Descriptions of 4.3 MIPI IO updated.</li> <li>● 1.2 Related Documents updated.</li> </ul>
10/25/2024	2.0.2E	3.5 Devices Supported updated.
12/13/2024	2.0.3E	3.5 Devices Supported updated.
02/28/2025	2.1E	<ul style="list-style-type: none"> <li>● 3.5 Devices Supported updated.</li> <li>● MIPI D-PHY RX Advance IP I/O ports updated.</li> <li>● 1.2 Related Documents updated.</li> </ul>
04/30/2025	2.1.1E	Figure 6-3 Input Signal Timing of MIPI D-PHY TX Advance in HS 1:16 Mode updated.
07/04/2025	2.2E	<ul style="list-style-type: none"> <li>● int_pll_lock and init_clk added in MIPI D-PHY TX Advance IP.</li> <li>● PLL Reference Clock parameter added in MIPI D-PHY TX Advance IP.</li> <li>● Descriptions of "Generation Config" option added.</li> <li>● The line rate range of the single lane TX/RX updated.</li> </ul>
08/08/2025	2.2.1E	Notes have been added below the Table 3-4 D-PHY RX Advance Mode Devices Supported and Table 3-6 D-PHY TX Advance Mode Devices Supported to indicate that some packages do not support MIPI soft IP RX/TX.
10/30/2025	2.2.2E	<ul style="list-style-type: none"> <li>● Removed the notes below the Table 3-4 D-PHY RX Advance Mode Devices Supported and Table 3-6 D-PHY TX Advance Mode Devices Supported to indicate that some packages do not support MIPI soft IP RX/TX.</li> <li>● Added the notes below the Table 3-5 D-PHY RX IO Type Devices Supported and Table 3-7 D-PHY TX IO Type Devices Supported to indicate that some packages can not support MIPI IO RX/TX.</li> </ul>
03/13/2026	2.2.3E	Added the notes describing the line rate in sections 3.1 Features and 3.2

Date	Version	Description
		Max. Frequency.

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# 1 About This Guide

## 1.1 Purpose

The purpose of Gowin MIPI D-PHY RX TX Advance IP User Guide is to help you to quickly learn the features and usage of Gowin MIPI D-PHY RX TX Advance IP by providing the descriptions of the functions, features, ports, timing, configuration, and reference design, etc.

## 1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at [www.gowinsemi.com](http://www.gowinsemi.com):

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS891, GW1NRF series of FPGA Products Data Sheet](#)
- [DS821, GW1NS series of FPGA Products Data Sheet](#)
- [DS881, GW1NER series of FPGA Products Data Sheet](#)
- [DS861, GW1NSR series of FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS961, GW2ANR series of FPGA Products Data Sheet](#)
- [DS971, GW2AN-18X and GW2AN-9X Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1239, GW5AST series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)

- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1118, GW5ART series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

## 1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
CSI	Camera Serial Interface
DSI	Display Serial Interface
GSR	Global System Reset
IP	Intellectual Property
LUT	Look-up Table
RAM	Random Access Memory

## 1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: [www.gowinsemi.com](http://www.gowinsemi.com)

E-mail: [support@gowinsemi.com](mailto:support@gowinsemi.com)

# 2 Overview

## 2.1 Introduction to Gowin MIPI D-PHY RX TX Advance IP

Gowin MIPI D-PHY TX RX Advance IP applies to the display serial interface (DSI) and the camera serial interface (CSI). It aims to receive and send images or video data. MIPI D-PHY provides a physical layer definition.

**Table 2-1 Gowin MIPI D-PHY RX Advance and TX Advance IP**

Gowin MIPI D-PHY RX Advance and TX Advance IP	
Logic Resource	Please refer to Table 3-2 and Table 3-3.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.7.05 Beta and above)

## 2.2 MIPI D-PHY

The Mobile Industry Processor Interface (MIPI) is an interface standard for mobile devices. MIPI D-PHY provides a physical definition for DSI and CSI and describes the physical layer interface protocols of source synchronous, high speed, and low power. In accordance with applications, MIPI D-PHY Advance includes RX and TX, which are used for receiving or transmitting the data in line with MIPI D-PHY. Figure 2-1 shows the diagram.

MIPI D-PHY typically includes one clock lane and 1~ 4 data lanes. You can configure the number of data lanes using IDE. The clock and data

lanes can switch between 1.2V LVCMOS signal and SLVS-200 differential signal.

MIPI D-PHY supports the following two data modes:

- High-speed (HS) mode
- Low-power (LP) mode

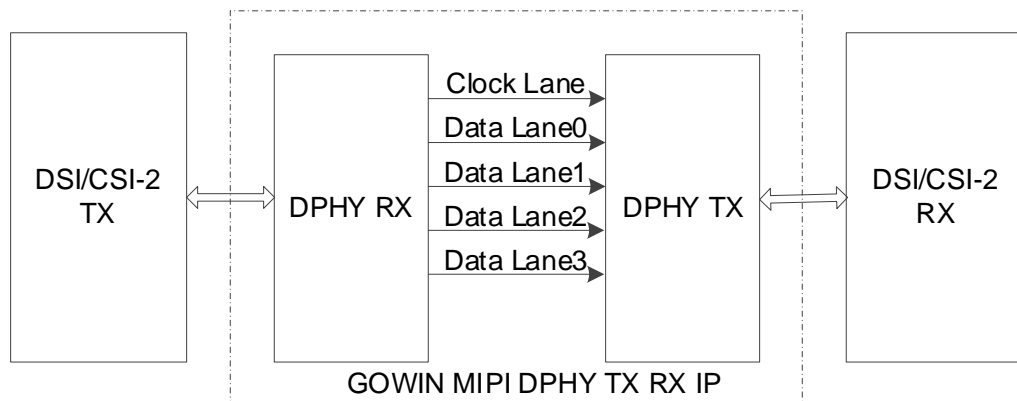
In HS mode, video data is transmitted through differential pair. Depending on the applications, the HS mode can be utilized at all times, or the D-PHY can be switched from HS differential lanes to signal ended signals.

When D-PHY is transmitting single ended signals, it enters to the LP mode.

**Note!**

- In camera and display applications, the device enters to the LP mode, which reduces power during the blanking period.
- In display applications, LP mode is used for screen configuration.

**Figure 2-1 MIPI D-PHY Structure Diagram**



# 3 Features and Performance

## 3.1 Features

- Compliant with MIPI Alliance Standard for D-PHY Specification, version 1.1
- Supports MIPI DSI and CSI-2 interfaces in both transmit and receive modes
- Supports unidirectional High-speed (HS) mode
- Supports bidirectional Low-power (LP) mode
- Supports serial HS data conversion to byte packets
- Supports MIPI D-PHY TX 8:1 mode and 16:1 mode
- Supports MIPI D-PHY RX 1:8 mode and 1:16 mode
- Supports IO types such as ELVDS, TLVDS, and MIPI IO
- The line rate of the single lane TX ranges from 80Mb/s to 2000Mb/s<sup>[1]</sup>
- The line rate of the single lane RX ranges from 80Mb/s to 1600Mb/s<sup>[1]</sup>
- Control data is transmitted in LP mode at a rate of 10Mb/s

**Note!**

<sup>[1]</sup>For the line rates supported by different devices, please refer to the [device datasheets](#) and [WP1153, Gowin MIPI Solution Capability White Paper](#).

## 3.2 Max. Frequency

The max. frequency of MIPI D-PHY is mainly determined by the line rate<sup>[1]</sup> and the speed grade of the devices.

**Note!**

<sup>[1]</sup>For the line rates supported by different devices, please refer to the [device datasheets](#) and [WP1153, Gowin MIPI Solution Capability White Paper](#).

## 3.3 Latency

D-PHY TX Latency is the time from inputting the data\_in (8-bit/16-bit parallel data) to outputting HS\_DATA.

D-PHY RX Latency is the time from inputting the HS\_DATA SOT (start-of-transmission) to outputting data\_out (8-bit/16-bit parallel data).

See Table 3-1 for the detailed Latency.

**Table 3-1 D-PHY TX RX Advance Latency**

Module	Line Rate ( Mb/s )	Lane	Latency (byteclk Latency <sup>[1]</sup> Cycle)
D-PHY TX	1200	1	3
D-PHY RX	1200	1	11

**Note!**

<sup>[1]</sup> Frequency of byteclk (MHz) = line rate in Mb/s/8

## 3.4 Resource Utilization

MIPI D-PHY RX and TX are implemented via Verilog language. Their performance and resource utilization may vary when the design is employed in a different device, or at a different density, speed, or grade.

Take the GW1N-2 series of FPGA device as an example. See Table 3-2 and Table 3-3 for the MIPI D-PHY RX and TX resource utilization. For the applications on other GOWINSEMI devices, please refer to the later release.

**Table 3-2 MIPI D-PHY RX Advance Resource Utilization**

Device Series	Speed Grade	Name	Resource Utilization	Remarks
GW1N-2	-6	LUT	477	<ul style="list-style-type: none"> <li>● 1:8 Mode</li> <li>● Four HS data lanes included</li> <li>● Word alignment and lane alignment modules included</li> <li>● clk_cross_fifo excluded</li> </ul>
		IODELAY	4	
		REG	505	
		BSRAM	0	
		IDES8	4	
		CLKDIV	1	
		DHCEN	1	

**Table 3-3 MIPI D-PHY TX Advance Resource Utilization**

Device Series	Speed Grade	Name	Resource Utilization	Remarks
GW1N-2	-6	LUT	3	1:8 Mode Internal PLL configured
		REG	0	
		CLKDIV	1	
		OSER8	5	

## 3.5 Devices Supported

**Table 3-4 D-PHY RX Advance Mode Devices Supported**

D-PHY RX Mode	Devices Supported
1:8 Mode	GW1N series, GW1NR series, GW1NS series, GW1NSR series, GW1NSER series, GW1NRF series, GW1AN series, GW2A series, GW2AR series, GW2ANR series, GW2AN series, GW5A series, GW5AT series, GW5AST series, GW5AS series, GW5AR series, GW5ART series, GW1NZ-2B, GW1NZ-2C
1:16 Mode	GW1NS series, GW1NSR series, GW1NSER series, GW5AT series, GW5AST series, GW5A series, GW5AS series, GW5AR series, GW5ART series, GW1N-1S, GW1N-2, GW1N-2B, GW1N-2C, GW1NR-2, GW1NR-2B, GW1NR-2C, GW1N-1P5, GW1N-1P5B, GW1N-1P5C, GW1NR-9, GW1NR-9C, GW1N-9, GW1N-9C, GW1NZ-2B, GW1NZ-2C

**Table 3-5 D-PHY RX IO Type Devices Supported**

D-PHY RX IO Type	Devices Supported
MIPI IO <sup>[1]</sup>	GW1NS series, GW1NSR series, GW1NSER series, GW5AT series, GW5A series, GW5AS series, GW5AST series, GW5AR series, GW5ART series, GW1N-9, GW1N-9C, GW1NR-9, GW1NR-9C, GW1N-1P5, GW1N-1P5B, GW1N-1P5C, GW1N-2, GW1N-2B, GW1NR-2, GW1NR-2B, GW1N-2C, GW1NR-2C, GW1NZ-2B, GW1NZ-2C, GW1NR-9, GW1NR-9C, GW1AN-9A, GW2AN-18X, GW2AN-9X
TLVDS IO	All Gowin devices except GW1N-1S, GW1NZ-1, and GW1NZ-1C
ELVDS IO	All Gowin devices

**Note!**

- <sup>[1]</sup>MIPI CLK requires GCLK IO when MIPI IO mode is used for GW2AN-18X and GW2AN-9X.
- GW5AT-LV15CS130 can not support MIPI IO RX.
- GW5A-LV25UG324S, GW5A-LV25PG256C, GW5A-LV25UG256C, GW5A-LV25LQ100, GW5A-LV25MG196S, GW5A-LV25PG256S, GW5A-LV25LQ144, GW5A-LV25PG196S can not support MIPI IO RX.
- GW5A-LV60UG324A can not support MIPI IO RX.
- GW5ART-LV15CM90P and GW5ART-LV15CM90PF can not support MIPI IO RX.

**Table 3-6 D-PHY TX Advance Mode Devices Supported**

D-PHY TX Mode	Devices Supported
8:1 Mode	GW1N series, GW1NR series, GW1NZ series, GW1NS series, GW1NSR series, GW1NSER series, GW1NRF series, GW1AN series, GW2A series, GW2AR series, GW2ANR series, GW2AN series, GW5AT series, GW5A series, GW5AST series, GW5AS series, GW5AR series, GW5ART series
16:1 Mode	GW1NS series, GW1NSR series, GW1NSER series, GW5AT series, GW5ART series, GW5AS series, GW5AST series, GW5A series, GW5AR series, GW1N-1S, GW1N-2, GW1N-2C, GW1N-2B, GW1NR-2, GW1NR-2C, GW1NR-2B, GW1N-1P5, GW1N-1P5B, GW1N-1P5C, GW1NZ-2B, GW1NZ-2C, GW1N-9, GW1N-9C, GW1NR-9, GW1NR-9C

**Table 3-7 D-PHY TX IO Type Devices Supported**

D-PHY TX IO Type	Devices Supported
MIPI IO	GW1NS series, GW1NSR series, GW1NSER series, GW5AR series, GW5ART series, GW1N-1P5, GW1N-1P5B, GW1N-1P5C, GW1N-2, GW1N-2B, GW1N-2C, GW1NR-2, GW1NR-2B, GW1NR-2C, GW1NR-9, GW1NR-9C, GW1N-9, GW1N-9C, GW1NZ-2B, GW1NZ-2C, GW5A-25A, GW5A-25B, GW5AS-25A, GW5AS-25B, GW5AT-60ES, GW5AT-60B, GW5A-60B, GW5AT-15A
TLVDS IO	All Gowin devices except GW1N-1S, GW1NZ-1, and GW1NZ-1C
ELVDS IO	All Gowin devices

**Note !**

- GW5AT-LV15CS130 can not support MIPI IO TX.
- GW5A-LV25UG324S, GW5A-LV25PG256C, GW5A-LV25UG256C, GW5A-LV25LQ100, GW5A-LV25MG196S, GW5A-LV25PG256S, GW5A-LV25LQ144, GW5A-LV25PG196S can not support MIPI IO TX.

- GW5A-LV60UG324A can not support MIPI IO TX.
- GW5ART-LV15CM90P and GW5ART-LV15CM90PF can not support MIPI IO TX.

# 4 Functional Description

MIPI D-PHY contains the following two D-PHY IP modules:

- D-PHY RX Advance
- D-PHY TX Advance

In D-PHY RX Advance and D-PHY TX Advance, HS data is converted to serial-parallel/parallel-serial respectively. The data in LP mode can be transmitted bi-directionally on any data lane or clock lane.

**Note!**

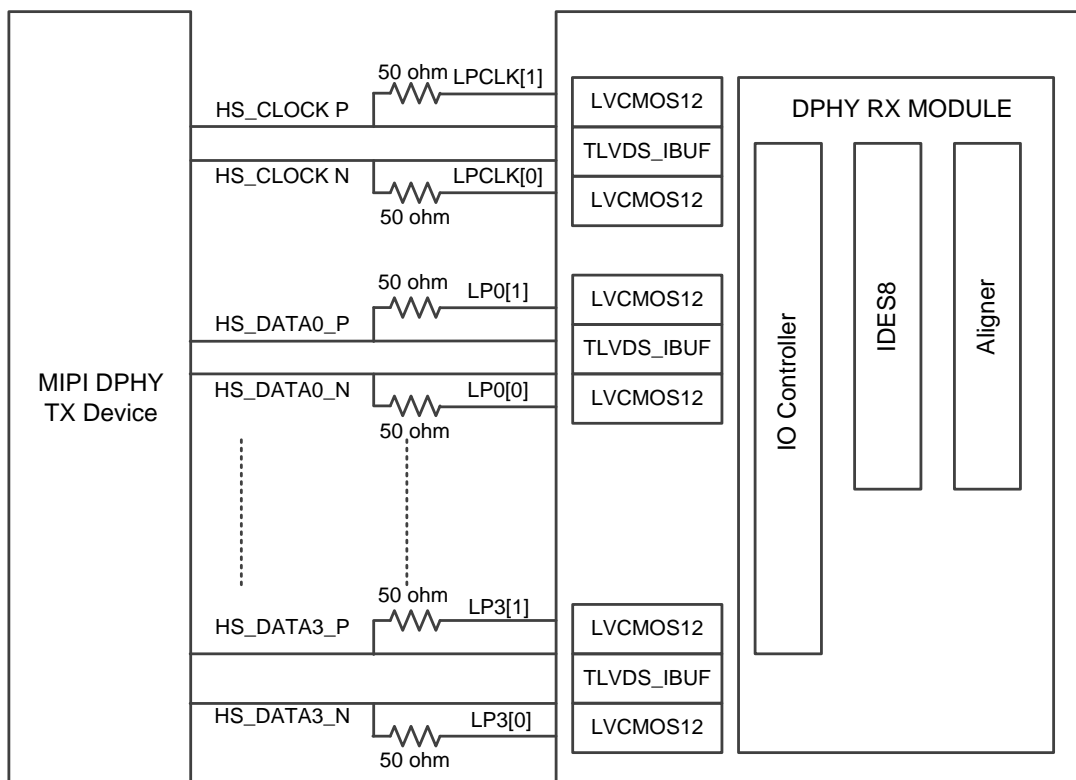
D- PHY RX Advance and D-PHY TX have different resister networks; However, both modules support bi-directional LP communication and unidirectional HS communication.

## 4.1 MIPI D-PHY RX Advance IP Structure and Function

HS data can be received on one clock lane and four clock data lanes using D-PHY RX Advance.

Each clock and data lane uses four I/Os. Two I/O pins are used to receive HS data with TLVDS differential I/O. TLVDS I/O is used to handle the common 200mV mode voltage. The other two I/Os are used as serial termination in HS mode, and can be used to transmit or receive 1.2V CMOS data in LP mode, as shown in Figure 4-1.

**Figure 4-1 Interface Implementation in HS Mode and LP Mode**



**Note!**

The resistance values in Figure 4-1 are for reference only.

In D-PHY RX module, HS data is deserialized using IDES8/IDES16. FPGA drives a divide-by-4/divide-by-8 clock and 8 bits/16 bits byte data directly using IDES8/IDES16.

**Note!**

The number of data lanes can be configured. Options are 1, 2,3, or 4 data lanes.

When the data is deserialized to 8 bits/16 bits byte data, and the lane is aligned, MIPI byte data is available in each byte clock cycle.

**Note!**

- The alignment is done by detecting of MIPI HS\_Ready sequence.
- MIPI HS\_Ready sequence is transmitted on all data lanes one clock cycle before the packet header.

hs\_en is used to reset the alignment module:

1. When hs\_en is low, the word alignment module is reset.
2. When hs\_en is high, the word alignment module looks for the next HS\_Ready sequence.
3. When HS\_Ready sequence is detected, the sync signal will increase, and the byte data at the output of the aligner will be properly aligned.

The aligner module consists of two subsidiary modules as below:

- The first module aligns the 8-bit data from the deserializer.
- The second module aligns each of the data lanes to each other.

**Note!**

- In some cases, lane alignment or lane and word alignment is not needed.
- Macro compiling commands can be used to turn the word and lane alignment on and off.

HS termination is designed to be implemented by controlling IO\_Ctrol\_RX module with term\_en signal. Although there is no direction detection mechanism, the following two ways can be used to enable HS termination:

1. The HS clock can be used to observe LP to HS data transition on one data lane.
2. In comparison to the data lane, the clock lane will enter the HS mode in advance and put off to the HS mode. Initialize the LP signals as input at startup, and then observe the clock and data lanes of LP and HS.

Once the sequence is detected, term\_en can be set to "low" by enabling HS\_termination.

The IO\_Ctrol\_RX module also controls LP signal.

Each data lane has a lp\*\_dir signal, which controls LP data direction between the FPGA and the transmitting device.

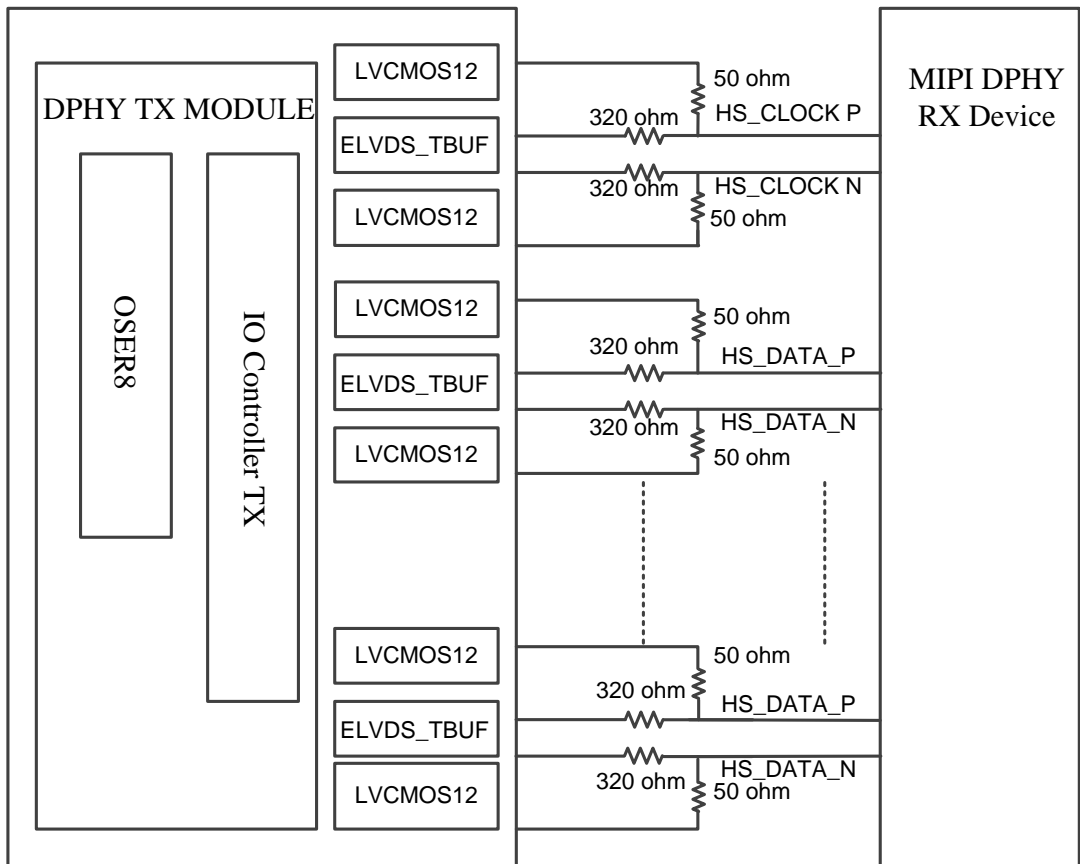
You can turn on/off LP IP for each clock and data lane individually by using Macro compiler directives. This can be convenient if you require the LP mode for one or two MIPI D-PHY data lanes.

The LP signal is defined as a 2-bit bus. Signal 1 is usually connected to the P-side, and 0 to the N-side. This maintains the consistency with the LP transition mode.

## 4.2 MIPI D-PHY TX Advance IP Structure and Function

You can use one clock lane and up to four data lanes by D-PHY TX IP. Each lane has four I/Os. Two I/O pins transmit HS data with ELVDS type or TLVDS type I/O. The other two I/O pins are used to provide voltage dividing circuit in HS mode and to transmit or receive 1.2V CMOS data in LP mode. For the circuit structure of HS data adopting ELVDS type I/O, see Figure 4-2; for the circuit structure of adopting TLVDS type I/O, see Figure 4-3.

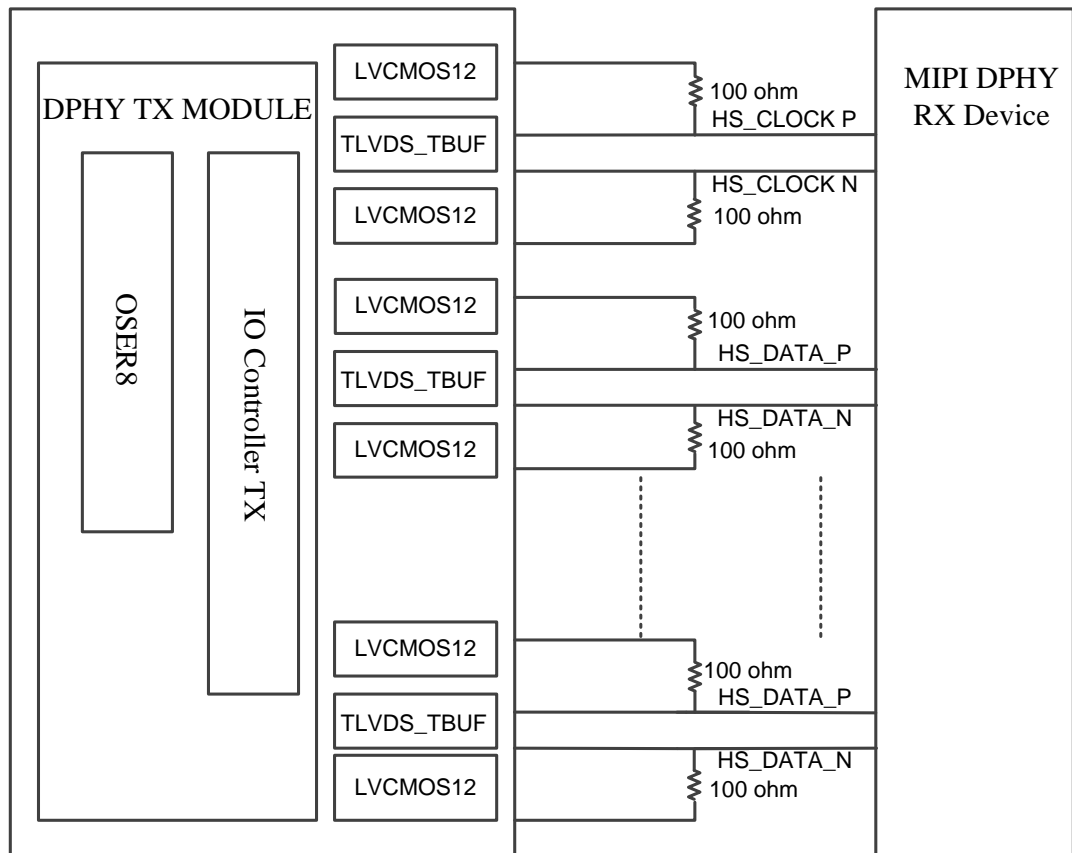
**Figure 4-2 Interface Implementation in HS Mode and LP Mode (ELVDS Used in HS Mode)**



**Note!**

The resistance values in Figure 4-2 are for reference only.

**Figure 4-3 Interface Implementation in HS Mode and LP Mode (TLVDS Used in HS Mode)**



**Note!**

The resistance values in Figure 4-3 are for reference only.

In the D-PHY TX module, HS data is serialized using OSER8/OSER16. D-PHY TX data is center aligned, so HS data lane and clock lane adopt the clock output signal with a phase shifting 0 and 90 degrees generated by the PLL respectively. You can select to use the external PLL or internal PLL to provide clock. It should be noted that it takes some time for the internal PLL in FPGA to lock.

IO\_Ctrol\_TX module controls data transmission in HS and LP modes:

- When **hs\_clk\_en** and **hs\_data\_en** signals are high, clock and data lanes are enabled in HS mode. In HS mode, IO\_Ctrol\_TX sets CMOS signals low to create a voltage divider network on LVDS output signals to achieve a 200mV common mode voltage.
- When **hs\_clk\_en** or **hs\_data\_en** is low, ELVDS I/O is set to high impedance, so it does not interfere with LP data transmissions. As MIPI specification defines clock lane going into or out of HS mode before or after the data lanes, there is an **hs\_clk\_en** control signal and an **hs\_data\_en** signal.

lp\_data\_dir signal controls the direction in LP mode:

- When hs\*\_en='1', the lp\*\_dir control signal is overwritten.
- While in LP mode, IO\_Ctrol\_TX module controls the LP data transmission.

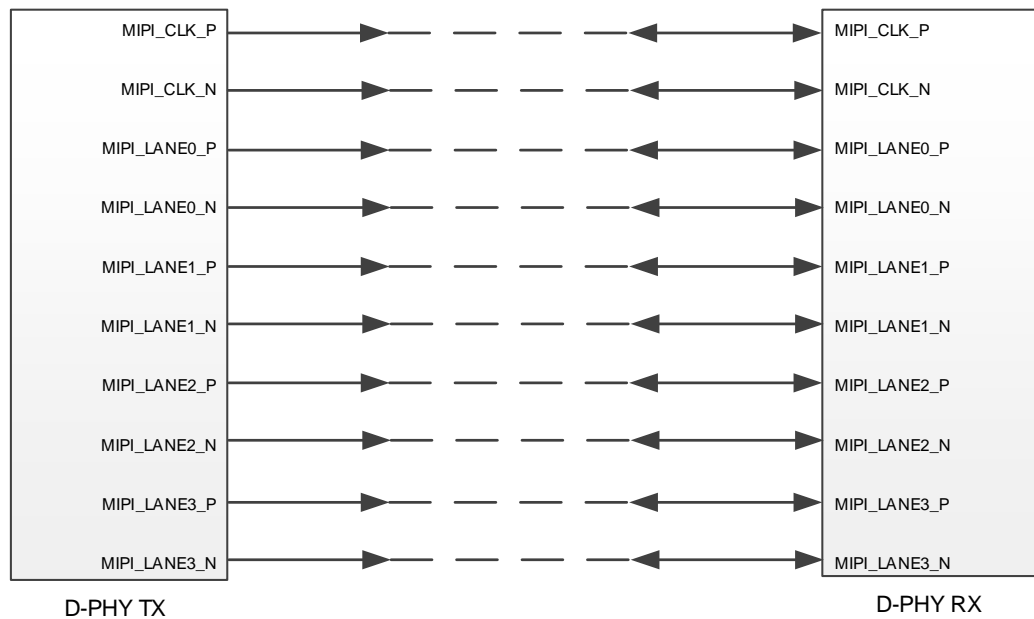
The lp\*\_dir signal controls the data direction in LP mode. The LP signals are defined as two-bit bus. Signal 1 is usually connected to the P-side, and 0 to the N-side, which maintains consistency with LP transition identification scheme.

## 4.3 MIPI IO

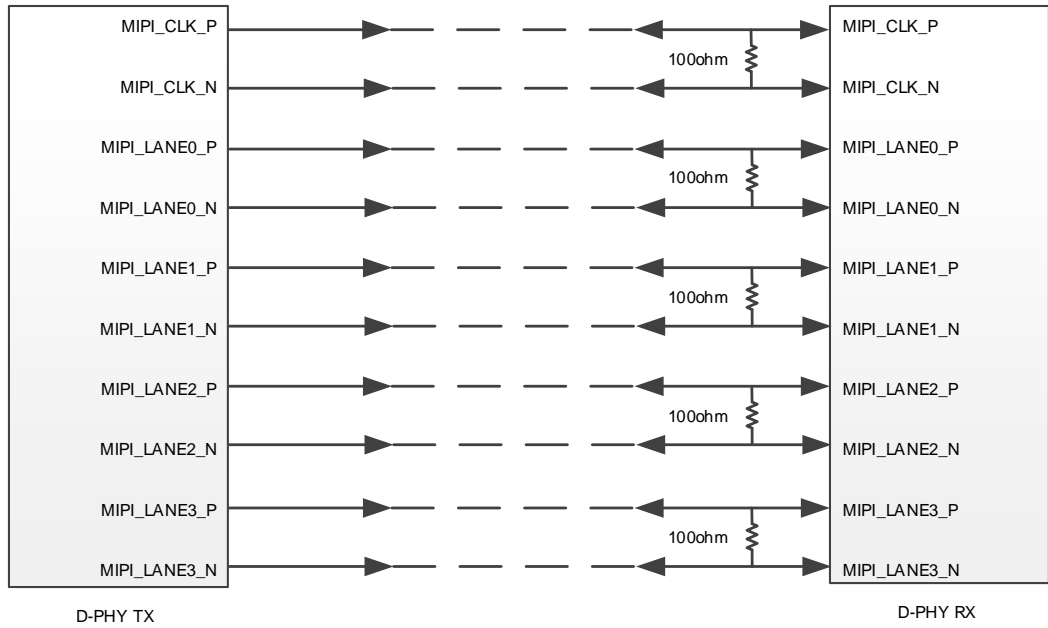
Gowin MIPI D-PHY RX/TX IP ports support MIPI IO. When you select MIPI IO TYPE, HS clock lane and LP clock lane share IO, and HS data lane and LP data lane share IO, as shown in Figure 4-4.

When using 9K and 4K series of chips, if the Bank voltage of D-PHY RX MIPI IO is 1.2V, a 100ohm matching resistor needs to be connected to the P terminal and the N terminal of the MIPI IO, as shown in Figure 4-5.

**Figure 4-4 MIPI IP Ports in MIPI IO Mode**



**Figure 4-5 MIPI IP Ports in MIPI IO Mode (External Termination Resistor Required)**



# 5 Port Description

## 5.1 MIPI D-PHY RX Advance IP Ports

For the MIPI D-PHY RX Advance IP I/O port descriptions, see Table 5-1.

Table 5-1 D-PHY RX Advance I/O Ports

Signal	I/O	Description
reset_n	Input	Reset Signal, active-low
HS_CLK	Input	<ul style="list-style-type: none"> <li>● HCLK</li> <li>● When IO TYPE is TLVDS or ELVDS</li> </ul>
HS_DATA<N>	Input	<ul style="list-style-type: none"> <li>● High-speed data lane&lt;N&gt;</li> <li>● When IO TYPE is TLVDS or ELVDS</li> </ul>
hs_en	Input	Initialize the word alignment module during the next HS-Ready sequence when non-GW5A/T series devices are selected.
clk_hs_en	Input	Clock lane receive enable, active-high, when GW5A/T series devices are selected.
data_hs_en	Input	Data lane receive enable, active-high; Initialize the word alignment module during the next HS-Ready sequence when GW5A/T series devices are selected.
clk_byte	Input	clk_cross_fifo read clock
clk_byte_out	Output	Clock Byte Out = HS_CLK/4
data_out<n>	Output	Parallel data output, data lane <n> <ul style="list-style-type: none"> <li>● When MIPI D-PHY is 1:8, the width is 8 bits.</li> <li>● When MIPI D-PHY is 1:16, the width is 16 bits.</li> </ul>
ready	Output	Active-high when parallel data is aligned
LP_CLK [1:0]	Bidirectional	LP clock lane

Signal	I/O	Description
		<ul style="list-style-type: none"> <li>● LP_CLK[0] = N wire, LP_CLK[1] = P wire;</li> <li>● When IO TYPE is TLVDS or ELVDS.</li> </ul>
LP_DATA<N> [1:0]	Bidirectional	<p>LP data lane&lt;N&gt;</p> <ul style="list-style-type: none"> <li>● LP&lt;N&gt; [0] = N wire, LP&lt;N&gt; [1] = P wire.</li> <li>● When IO TYPE is TLVDS or ELVDS.</li> </ul>
clk_term_en	Input	<p>Clock Lane terminal resistor control signal</p> <ul style="list-style-type: none"> <li>● In MIPI IO mode, 1: turn on resistor, 0: turn off resistor;</li> <li>● In other IO Type modes, 1: control LP signal to output 0; 0: lp_data_dir&lt;n&gt; controls LP signal output.</li> </ul>
data_term_en	Input	<p>Data Lane terminal resistor control signal</p> <ul style="list-style-type: none"> <li>● In MIPI IO mode, 1: turn on resistor, 0: turn off resistor.</li> <li>● In other IO Type modes, 1: control LP signal to output 0; 0: lp_data_dir&lt;n&gt; controls LP signal output.</li> </ul>
lp_clk_dir	Input	<p>Control the direction of LP clock</p> <ul style="list-style-type: none"> <li>● '0': LP clock receive</li> <li>● '1': LP clock transmit</li> </ul>
lp_data<n>_dir	Input	<p>Control the direction of LP data</p> <ul style="list-style-type: none"> <li>● '0': LP data receive</li> <li>● '1': LP data transmit</li> </ul>
lp_clk_out [1:0]	Output	<p>LP receive clock</p> <p>Available when lp_clk_dir = '0' and term_en = '0'</p>
lp_data<n>_out [1:0]	Output	<p>LP receive data</p> <p>Available when lp_data&lt;n&gt;_dir = '0' and term_en = '0'</p>
lp_clk_in [1:0]	Input	<p>LP transmit clock</p> <p>Available when lp_clk_dir = '1' and term_en = '0'.</p>
lp_data<n>_in [1:0]	Input	<p>LP transmit data</p> <p>Available when p_data&lt;n&gt;_dir = '1' and term_en = '0'</p>
MIPI_CLK	Bidirectional	When IO TYPE is MIPI IO, HS and LP mode share the same clock lane
MIPI_LANE<N>	Bidirectional	When IO TYPE is MIPI IO, HS and LP mode share the same data lane

Signal	I/O	Description
lane<n>_iodelay	Output	Data lane <n> IO delay scan result, when Lane <n> IO Delay Scan Enable is checked, and it is valid when lane <n>_iodelay_lock is high.
lane<n>_iodelay_lock	Output	Data data <n> IO delay scan result locked, active-high, when Lane <n> IO Delay Scan Enable is checked.

**Note!**

- The high and low of lp\_clk\_in and lp\_clk\_out is corresponded to the high and low of LP\_CLK.
- The high and low of lp\_data<n>\_in and lp\_data<n>\_out is corresponded to the high and low of lp\_data<n>.

## 5.2 MIPI D-PHY TX Advance IP Ports

For MIPI D-PHY TX Advance IP I/O ports descriptions, see Table 5-2.

**Table 5-2 D-PHY TX Advance I/O Ports**

Signal	I/O	Description
reset_n	Input	Reset signal, active low
HS_CLK	Output	<ul style="list-style-type: none"> <li>• High speed clock</li> <li>• When IO TYPE is TLVDS or ELVDS</li> </ul>
HS_DATA<N>	Output	<ul style="list-style-type: none"> <li>• High speed data lane&lt;N&gt;</li> <li>• When IO TYPE is TLVDS or ELVDS</li> </ul>
clk_byte	Input	Input clock when using internal PLL
clk_bit	Input	Input clock when using external PLL; clk_bit and clk_bit_90 have a phase difference of 90° with the same frequency as HS_CLK
clk_bit_90	Input	
sclk	Output/ Input	<ul style="list-style-type: none"> <li>• TX internal clock output when using an internal PLL, typically used to sample data_in.</li> <li>• TX external clock input when using an external PLL.</li> </ul>
int_pll_lock	Output	When using the internal PLL, it is the PLL lock signal.
init_clk	Input	When using the internal PLL, it is the PLL reference clock.
clk_data	Input	<ul style="list-style-type: none"> <li>• When MIPI D-PHY is 8:1, the width is 8 bits, such as 8'b01010101.</li> <li>• When MIPI D-PHY is 16:1, the width is 16</li> </ul>

Signal	I/O	Description
		bits, such as 16'b0101010101010101.
lp_clk_dir	Input	MIPI LP clock lane direction <ul style="list-style-type: none"> <li>● When set to 1, it is output</li> <li>● When set to 0, it is input</li> <li>● When IO TYPE is MIPI</li> </ul>
lp_clk_out	Input	It is MIPI LP TX clock lane, <ul style="list-style-type: none"> <li>● lp_clk_out [0] = N wire, lp_clk_out [1] = P wire</li> <li>● When lp_clk_dir is 1.</li> <li>● When IO TYPE is MIPI.</li> </ul>
lp_clk_in	Output	It is MIPI LP RX clock lane, <ul style="list-style-type: none"> <li>● lp_clk_in [0] = N wire, lp_clk_in [1] = P wire</li> <li>● When lp_clk_dir is 0</li> <li>● When IO TYPE is MIPI</li> </ul>
data_in<n>	Input	Parallel data input, data lane <n> <ul style="list-style-type: none"> <li>● When MIPI D-PHY is 8:1, the width is 8 bits.</li> <li>● When MIPI D-PHY is 16:1, the width is 16 bits.</li> </ul>
LP_CLK [1:0]	Bidirectional	LP clock lane <ul style="list-style-type: none"> <li>● LPCLK[0] = N wire, LP_CLK[1] = P wire;</li> <li>● When IO TYPE is TLVDS or ELVDS.</li> </ul>
LP_DATA<N> [1:0]	Bidirectional	LP data lane<N>; <ul style="list-style-type: none"> <li>● LP&lt;N&gt; [0] = N wire, LP&lt;N&gt; [1] = P wire;</li> <li>● When IO TYPE is TLVDS or ELVDS.</li> </ul>
hs_clk_en	Input	Enable HS clock on output, set LP_CLK signal as 0, and overwrite lp_clk_dir signal
hs_data_en	Input	Enable HS clock output, set LP_DATA<N> signals as 0, and overwrite lp_data<n>_dir signal
lp_clk_dir	Input	Control the direction of LP clock <ul style="list-style-type: none"> <li>● '0': LP clock receive</li> <li>● '1': LP clock transmit</li> </ul>
lp_data<n>_dir	Input	Control the direction of LP data <ul style="list-style-type: none"> <li>● '0': LP data receive</li> <li>● '1': LP data transmit</li> </ul>
lp_clk_out [1:0]	Input	LP transmit clock Available when lp_clk_dir = '1' and hs_clk_en = '0', no terminal resistance in TX
lp_data<n>_ou	Input	LP transmits data

Signal	I/O	Description
t [1:0]		Available when lp_data<n>_dir = '1' and hs_data_en = '0'
lp_clk_in [1:0]	Output	LP receive clock Available when lp_clk_dir = '0' and hs_clk_en = '0', no terminal resistance in TX
lp_data<n>_in [1:0]	Output	LP receive data Available when lp_data<n>_dir = '0' and hs_clk_en = '0'
MIPI_CLK	Output	When IO TYPE is MIPI IO, it is the shared clock lane for HS and LP mode.
MIPI_LANE<N>	Output	When IO TYPE is MIPI IO, it is the shared data lane for HS and LP mode.

**Note!**

- The high and low of lp\_clk\_in and lp\_clk\_out is corresponded to the high and low of LP\_CLK.
- The high and low of lp\_data<n>\_in and lp\_data<n>\_out is corresponded to the high and low of lp\_data<n>.

# 6 Timing Description

This chapter mainly describes the input signals timing of MIPI D- PHY RX Advance and TX Advance in HS mode.

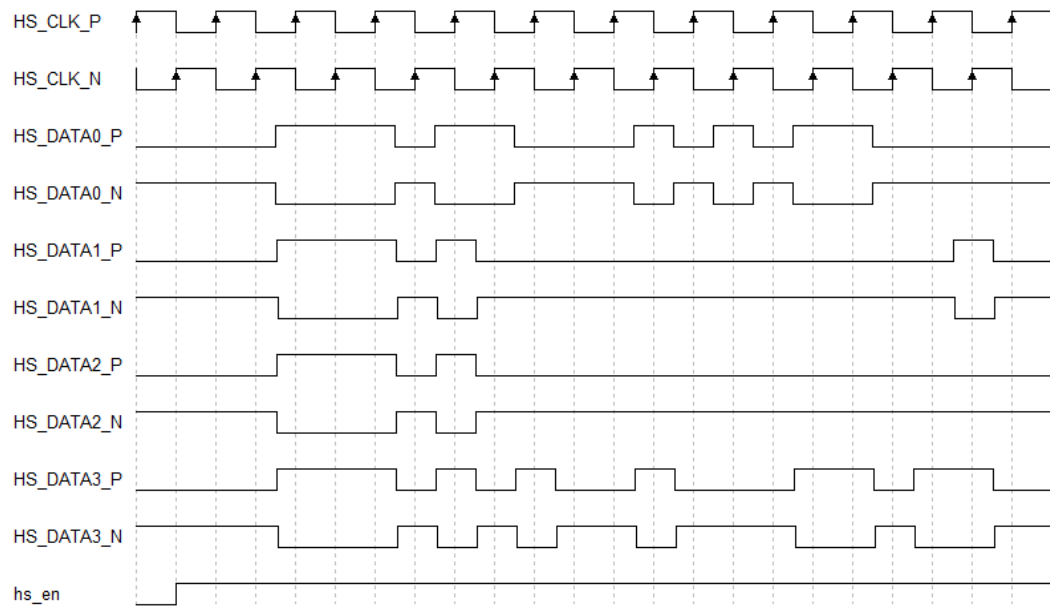
In applications, RX and TX can be connected; i.e., RX output can be TX input, and TX output can be RX input. Therefore, only the timing for RX and TX input signals is described as below.

## 6.1 RX Input Signal Timing

The clock and data lane signal timing of MIPI D-PHY RX Advance in HS 1:8 mode is as shown in Figure 6-1 .

One clock lane (HS\_CLK) and four data lanes (HS\_DATA0, HS\_DATA1, HS\_DATA2, and HS\_DATA3) are used in the diagram. Clock lane and data lane are all differential signal input. In HS mode, clock and data center is aligned when transmitting image data. The signal hs\_en needs to be set to high before receiving HS\_DATA data.

The signal timing of MIPI D- PHY RX Advance in HS 1:16 mode is similar to that of 1:8 mode. Note that the data width is 16 bits (2 byte) after RX conversion. RX will put the first received data to the lower 8 bits.

**Figure 6-1 Input Signal Timing of MIPI D-PHY RX Advance in HS 1:8 Mode**

## 6.2 TX Input Signal Timing

The clock and data lane signal timing of MIPI D-PHY TX Advance in HS mode is as shown in Figure 6-2 . When using TX:

- If internal PLL is configured, `clk_byte` needs to be provided (the frequency is 1/4 of `HS_CLK`)
- If internal PLL is not used, `CLKOP` and `CLKOS` with 90-degree phase difference need to be provided. (`CLKOP`, `CLKOS`, and `HS_CLK` have same frequency)

In Figure 6-2 , 8:1 mode is used and one clock lane (`HS_CLK`) and four data lanes (`data_in0`, `data_in1`, `data_in2`, and `data_in3`) are used. The `hs_clk_en` and `hs_data_en` signals need to be set as high before receiving `data_in` data.

In Figure 6-3 16:1 mode is used. The timing is similar to that of 8:1 mode. In 16:1 mode, 16 bits (2 bytes) data is converted in each cycle. The low 8 bits (low byte) data will be send first, so the packet header of B8 locates in the lower 8 bits of the first data.

Figure 6-2 Input Signal Timing of MIPI D-PHY TX Advance in HS 1:8 Mode

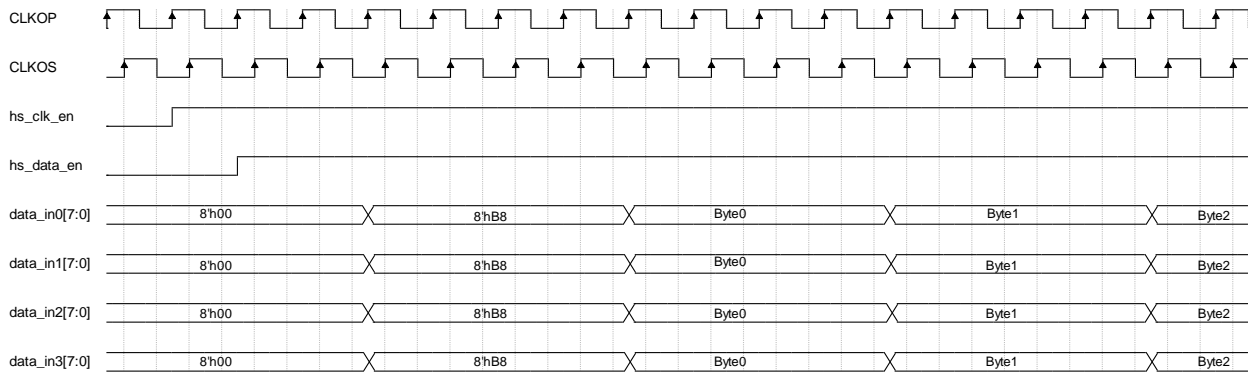
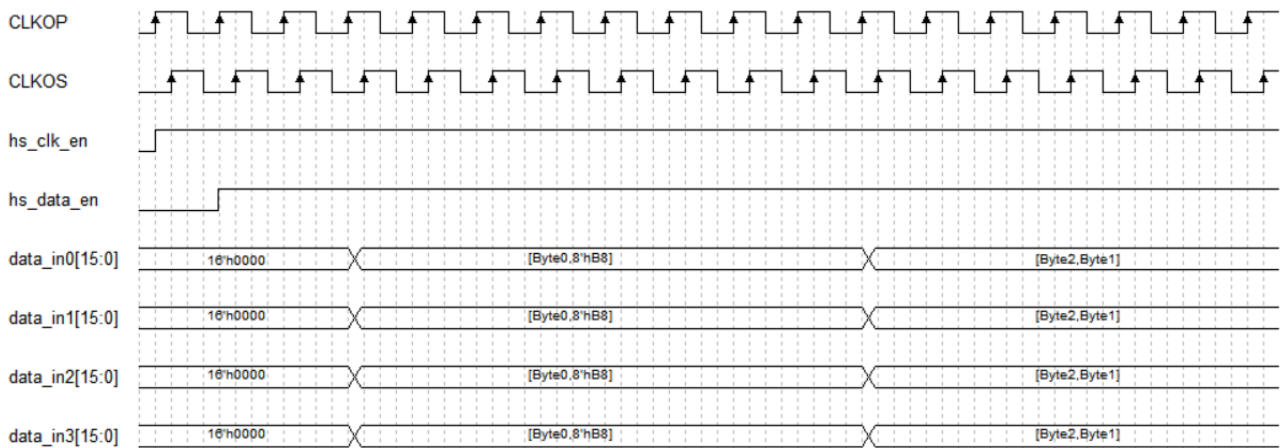


Figure 6-3 Input Signal Timing of MIPI D-PHY TX Advance in HS 1:16 Mode



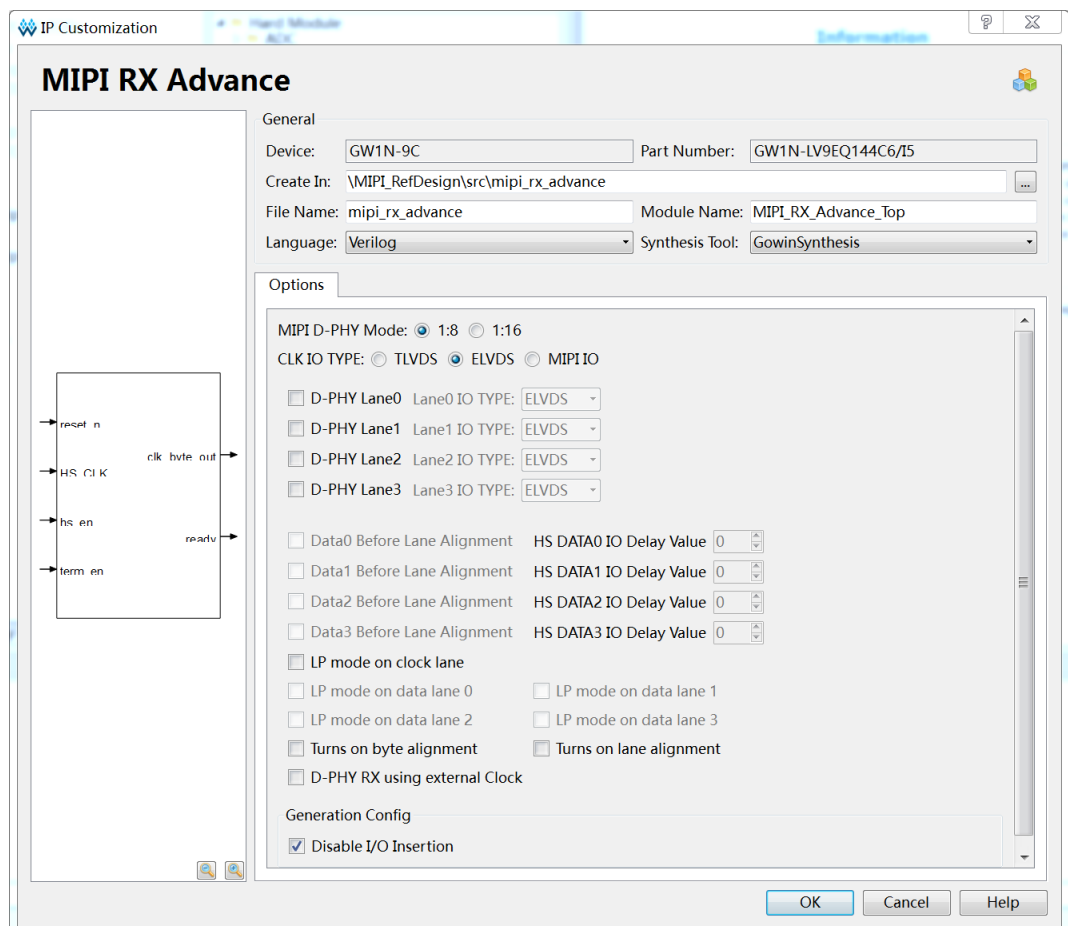
# 7 Configuration and Generation

Start "IP Core Generator" from the "Tools" menu in the Gowin software and then configure and generate the MIPI D-PHY RX and MIPI D-PHY TX Advance.

## 7.1 MIPI D-PHY RX Advance Configuration

The configuration options for MIPI D-PHY RX Advance are shown in Figure 7-1.

Figure 7-1 MIPI D-PHY RX Advance Configuration



1. Name the MIPI D-PHY RX Advance by modifying the "File Name" text box.
2. Create the Advance top module name of MIPI D-PHY RX Advance by modifying "Module Name" text box.
3. Configure the number of HS data lane, the clock and data lane in LP mode, and the byte alignment or lane alignment through "Options". Table 7-1 lists the detailed configuration.
4. Only one HS clock lane and one HS clock lane are used by default.

**Table 7-1 MIPI D-PHY RX Advance Options**

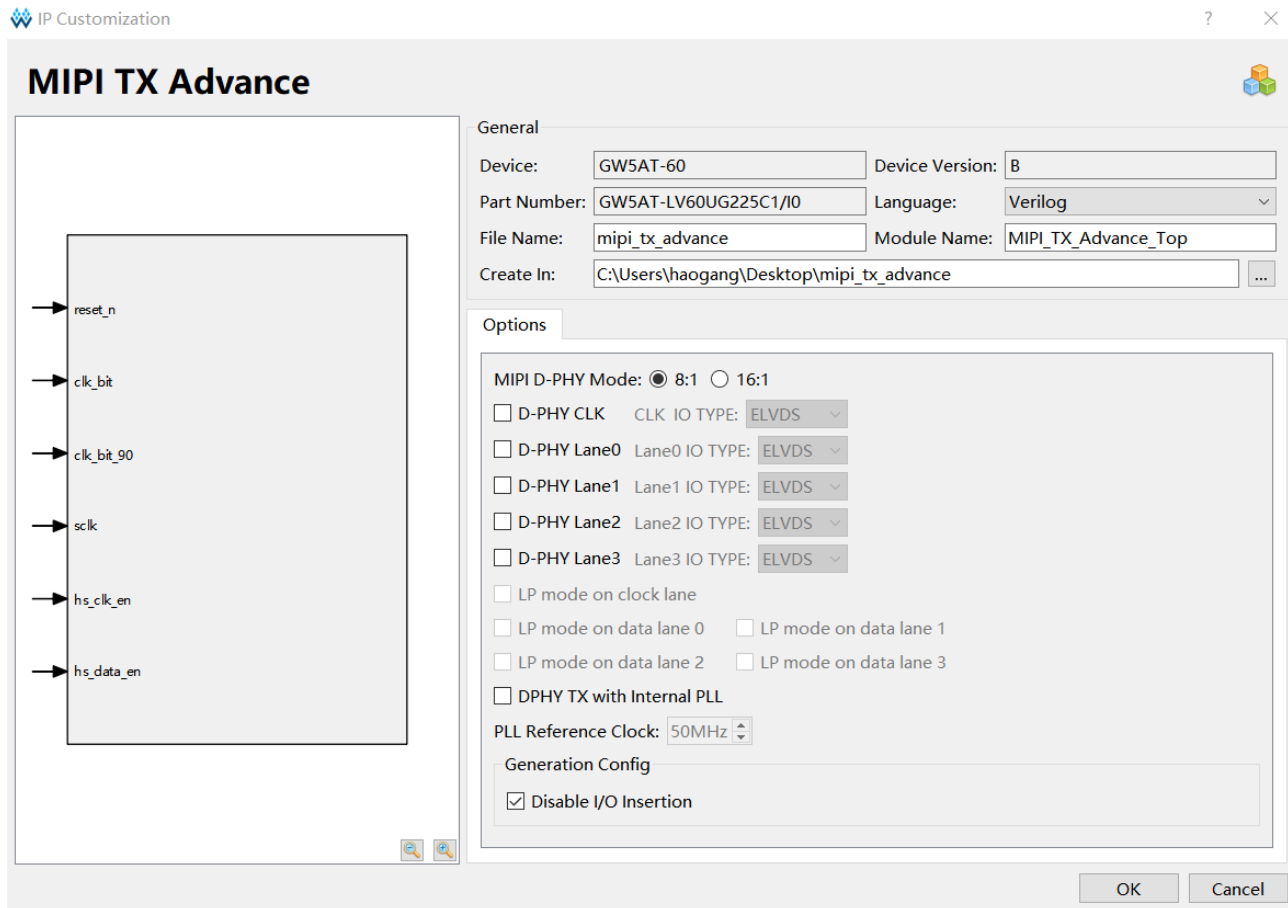
Options	Description
MIPI D-PHY Mode	Set the data mode as 1:8 or 1:16.
CLK IO Type	Set HS CLK Lane port as ELVDS, TLVDS, or MIPI IO.
D-PHY Lane0	Enable HS Lane0 to generate HS_DATA0 or MIPI_LANE0.
Lane0 IO Type	Set HS Lane0 port as ELVDS, TLVDS or MIPI IO.
D-PHY Lane1	Enable HS Lane1 to generate HS_DATA1 or MIPI_LANE1.
Lane1 IO Type	Set HS Lane1 port as ELVDS, TLVDS or MIPI IO.
D-PHY Lane2	Enable HS Lane2 to generate HS_DATA2 or MIPI_LANE2.
Lane2 IO Type	Set HS Lane2 port as ELVDS, TLVDS or MIPI IO.
D-PHY Lane3	Enable HS Lane3 to generate HS_DATA3 or MIPI_LANE3.
Lane3 IO Type	Set HS Lane3 port as ELVDS, TLVDS or MIPI IO.
Data3/2/1/0 Before Lane Alignment	<ul style="list-style-type: none"> <li>● Set whether to generate data port, output data before entering the lane alignment module;</li> <li>● HS Lanes can be set independently.</li> </ul>
HS Data3/2/1/0 IO Delay Value	<ul style="list-style-type: none"> <li>● Set the IO Delay value of HS Lane ports</li> <li>● HS Lanes can be set independently.</li> </ul>
LP mode on clock lane	Generate LP_CLK[1:0] and the other I/O ports for LP mode on clock lane.
LP mode on data lane0	Generate LP_DATA0[1:0] and the other I/O ports for LP mode on data lane0.
LP mode on data lane1	Generate LP_DATA1[1:0] and the other I/O ports for LP mode on data lane1.
LP mode on data lane2	Generate LP_DATA2[1:0] and the other I/O ports

Options	Description
	for LP mode on data lane2.
LP mode on data lane3	Generate LP_DATA3[1:0] and the other I/O ports for LP mode on data lane3.
Turns on byte alignment	Check this option to enable byte alignment, which is used to align the bytes after deserializing on one lane.
Turns on lane alignment	Check this option to enable lane alignment, which is used to align different data lanes.
D-PHY RX using external Clock	Check this option for RX module to use an external clock (clk_byte), and data_out0/1/2/3 will align at clk_byte.
Generation Config	<ul style="list-style-type: none"> <li>● If it is selected, the IP will not insert IBUF, OBUF, and IOBUF in the synthesized netlist.</li> <li>● If it is not selected, the IP will insert IBUF, OBUF, and IOBUF in the synthesized netlist.</li> <li>● The default setting is checked.</li> </ul>

## 7.2 MIPI D-PHY TX Advance Configuration

The configuration options for MIPI D-PHY TX Advance are shown in Figure 7-2.

Figure 7-2 MIPI D-PHY TX Advance Configuration



1. Name the MIPI D-PHY TX Advance by modifying the "File Name" text box.
2. Create the Advance top module name of MIPI D-PHY TX Advance by modifying "Module Name" text box.
3. Configure the number of HS data lane, whether the clock and data lane in LP mode use the internal PLL or not through "Options". Table 7-2 lists the detailed configuration.
4. Only one HS clock lane and one HS clock lane are used by default.

Table 7-2 MIPI D-PHY TX Advance Options

Options	Description
MIPI D-PHY Mode	Set the data mode as 1:8 or 1:16
D-PHY CLK	Enable HS Clock Lane to generate HS_CLK or

Options	Description
	MIPI_CLK
CLK IO Type	Set HS CLK Lane port as ELVDS, TLVDS, or MIPI IO
D-PHY Lane0	Enable HS Lane0 to generate HS_DATA0 or MIPI_LANE0
Lane0 IO Type	Set HS Lane0 port as ELVDS, TLVDS or MIPI IO
D-PHY Lane1	Enable HS Lane1 to generate HS_DATA1 or MIPI_LANE1
Lane1 IO Type	Set HS Lane1 port as ELVDS, TLVDS or MIPI IO
D-PHY Lane2	Enable HS Lane2 to generate HS_DATA2 or MIPI_LANE2
Lane2 IO Type	Set HS Lane2 port as ELVDS, TLVDS or MIPI IO
D-PHY Lane3	Enable HS Lane3 to generate HS_DATA3 or MIPI_LANE3
Lane3 IO Type	Set HS Lane3 port as ELVDS, TLVDS or MIPI IO
LP mode on clock lane	Generate LP_CLK[1:0] and the other I/O ports for LP mode on clock lane
LP mode on data lane0	Generate LP_DATA0[1:0] and the other I/O ports for LP mode on data lane0
LP mode on data lane1	Generate LP_DATA1[1:0] and the other I/O ports for LP mode on data lane1
LP mode on data lane2	Generate LP_DATA2[1:0] and the other I/O ports for LP mode on data lane2
LP mode on data lane3	Generate LP_DATA3[1:0] and the other I/O ports for LP mode on data lane3
D-PHY TX with Internal PLL	In this mode, TX module will use an internal PLL. The internal PLL will generate a pair of clock with 90-degree phase difference and sclk is the output clock signal.
PLL Reference Clock	If the TX module uses the internal PLL, this parameter must be set to the frequency of init_clk.
Generation Config	<ul style="list-style-type: none"> <li>● If it is selected, the IP will not insert IBUF, OBUF, and IOBUF in the synthesized netlist.</li> <li>● If it is not selected, the IP will insert IBUF, OBUF, and IOBUF in the synthesized netlist.</li> <li>● The default setting is checked.</li> </ul>

# Appendix **A** MIPI D-PHY Data Rates

Table A-1 MIPI D-PHY Data Rates (LittleBee Family)

Resolution	Frame Rate (HZ)	Bits Per Pixel (Bits)	Total Data Rate (Mbps)	Lane Number	Per Lane Bit Rate (Mbps)	Recommended Gearing Ratio (1:N)	Per Lane Fabric Clock (MHz)
FHD 1920x1080p (2200x1125)	60	8	1188	2	594.0	8	74.25
		10	1485	2	742.5	8	92.81
		16	2376	2	1188.0	16	74.25
		18	2673	4	668.3	8	83.53
		24	3564	4	891.0	8	111.38
	120	8	2376	2	1188.0	16	74.25
		10	2970	4	742.5	8	92.81
		16	4752	4	1188.0	16	74.25
		18	5346	8	668.3	8	83.53
		24	7128	8	891.0	8	111.38
UHD 3840x2160p (4400x2250)	30	8	2376	4	594.0	8	74.25
		10	2970	4	742.5	8	92.81
		16	4752	4	1188.0	16	74.25
		18	5346	8	668.3	8	83.53
		24	7128	8	891.0	8	111.38
	60	8	4752	4	1188.0	16	74.25
		10	5940	8	742.5	8	92.81
		16	9504	8	1188.0	16	74.25

Table A-2 MIPI D-PHY Data Rates (Arora Family)

Resolution	Frame Rate (HZ)	Bits Per Pixel (Bits)	Total Data Rate (Mbps)	Lane Number	Per Lane Bit Rate (Mbps)	Recommended Gearing Ratio (1:N)	Per Lane Fabric Clock (MHz)
FHD 1920x1080p (2200x1125)	60	8	1188	2	594.0	8	74.25
		10	1485	2	742.5	8	92.81
		16	2376	2	1188.0	8	148.50
		18	2673	4	668.3	8	83.53
		24	3564	4	891.0	8	111.38
	120	8	2376	2	1188.0	8	148.50
		10	2970	4	742.5	8	92.81
		16	4752	4	1188.0	8	148.50
		18	5346	8	668.3	8	83.53
		24	7128	8	891.0	8	111.38
UHD 3840x2160p (4400x2250)	30	8	2376	4	594.0	8	74.25
		10	2970	4	742.5	8	92.81
		16	4752	4	1188.0	8	148.50
		18	5346	8	668.3	8	83.53
		24	7128	8	891.0	8	111.38
	60	8	4752	4	1188.0	8	148.50
		10	5940	8	742.5	8	92.81
		16	9504	8	1188.0	8	148.50

