



Gowin LVDS 7to1 TX RX Reference Design **User Manual**

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Revision History

Date	Version	Description
03/28/2025	1.0E	Initial version published.
05/23/2025	1.1E	AUTO_PHASE mode removed from the RX reference design.

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1 About This Guide

1.1 Purpose

The purpose of Gowin LVDS 7to1 TX RX reference design user manual is to help you learn the features and usage of Gowin LVDS 7to1 TX RX reference design by providing the descriptions of features, functions, parameters, and reference design examples, etc.

1.2 Related Documents

You can find the related documents at www.gowinsemi.com:

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS821, GW1NS series of FPGA Products Data Sheet](#)
- [DS861, GW1NSR series of FPGA Products Data Sheet](#)
- [DS881, GW1NSER Series of SecureFPGA Products Datasheet](#)
- [DS891, GW1NRF series of Bluetooth FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)
- [DS961, GW2ANR series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
DE	Data Enable
FPGA	Field Programmable Gate Array
HS	Horizontal Sync
JEIDA	Japan Electronic Industry Development Association
LVDS	Low-Voltage Differential Signaling
VESA	Video Electronics Standards Association
VS	Vertical Sync

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Overview

Low-Voltage Differential Signaling (LVDS) 7:1 video interface is mainly used in LCD panel driver products. The LVDS 7to1 TX is used to receive parallel video signals and then convert them to LVDS signals for output. LVDS 7to1 RX is used to receive LVDS signals and then convert them into parallel video signals.

Table 2-1 Gowin LVDS 7to1 TX RX Overview

Gowin LVDS 7to1 TX RX	
Logic Resource	Please refer to Table 2-2 and Table 2-3.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.5.02beta and above)

2.2 Features

- Supports VESA and JEIDA standards
- Supports RGB888 and RGB666
- Supports one channel, two channels and 4 lanes/channel
- The data rate of single lane supports 80Mb/s~700Mb/s

2.3 Resource Utilization

Gowin 7to1 DVI 7to1 TX RX can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades. Take GW1N-4 as an instance, and the resource utilization is as shown in Table 2-2 and Table 2-3.

Table 2-2 LVDS 7to1 TX Resource Utilization

Device Series	Speed Grade	Name	Resource Utilization	Remarks
GW1N-4	-6	LUT	1	Configure internal PLL, RGB888, and One Channel.
		REG	0	
		PLL	1	
		OVIDEO	5	

Table 2-3 LVDS 7to1 RX Resource Utilization

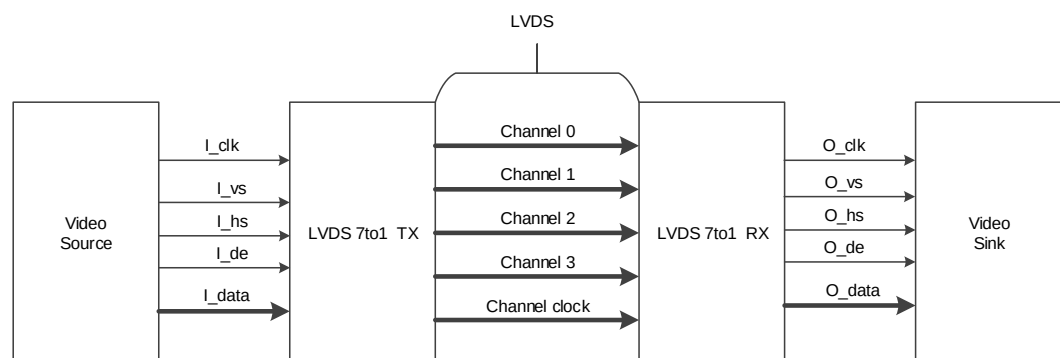
Device Series	Speed Grade	Name	Resource Utilization	Remarks
GW1N-4	-6	LUT	291	Configure internal PLL, RGB888, and One Channel.
		REG	158	
		PLL	1	
		CLKDIV	1	
		IODELAY	4	
		IVIDEO	5	

3 Functional Description

3.1 System Block Diagram

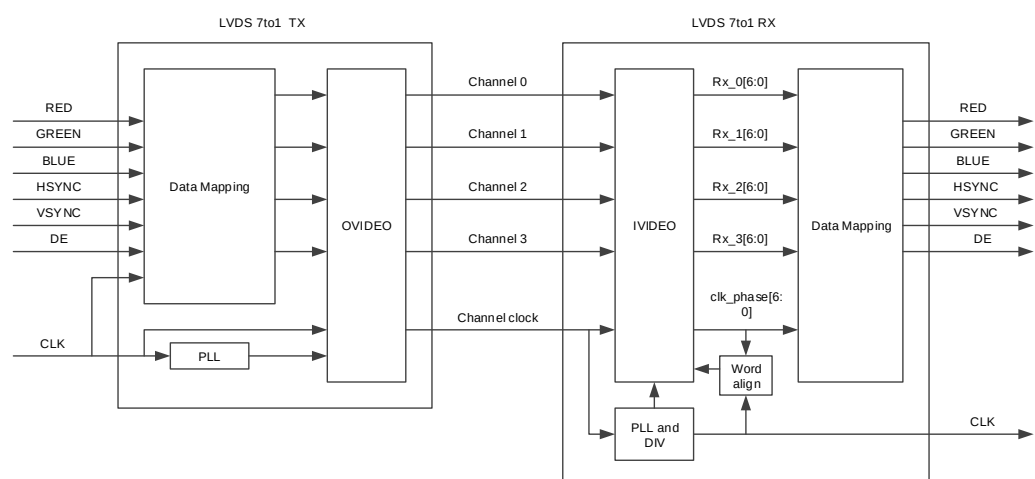
Gowin LVDS 7to1 TX RX includes LVDS 7to1 TX and LVDS 7to1 RX, and its block diagram is as shown in Figure 3-1.

Figure 3-1 Block Diagram



3.2 Implementation Diagram

Figure 3-2 Implementation Diagram



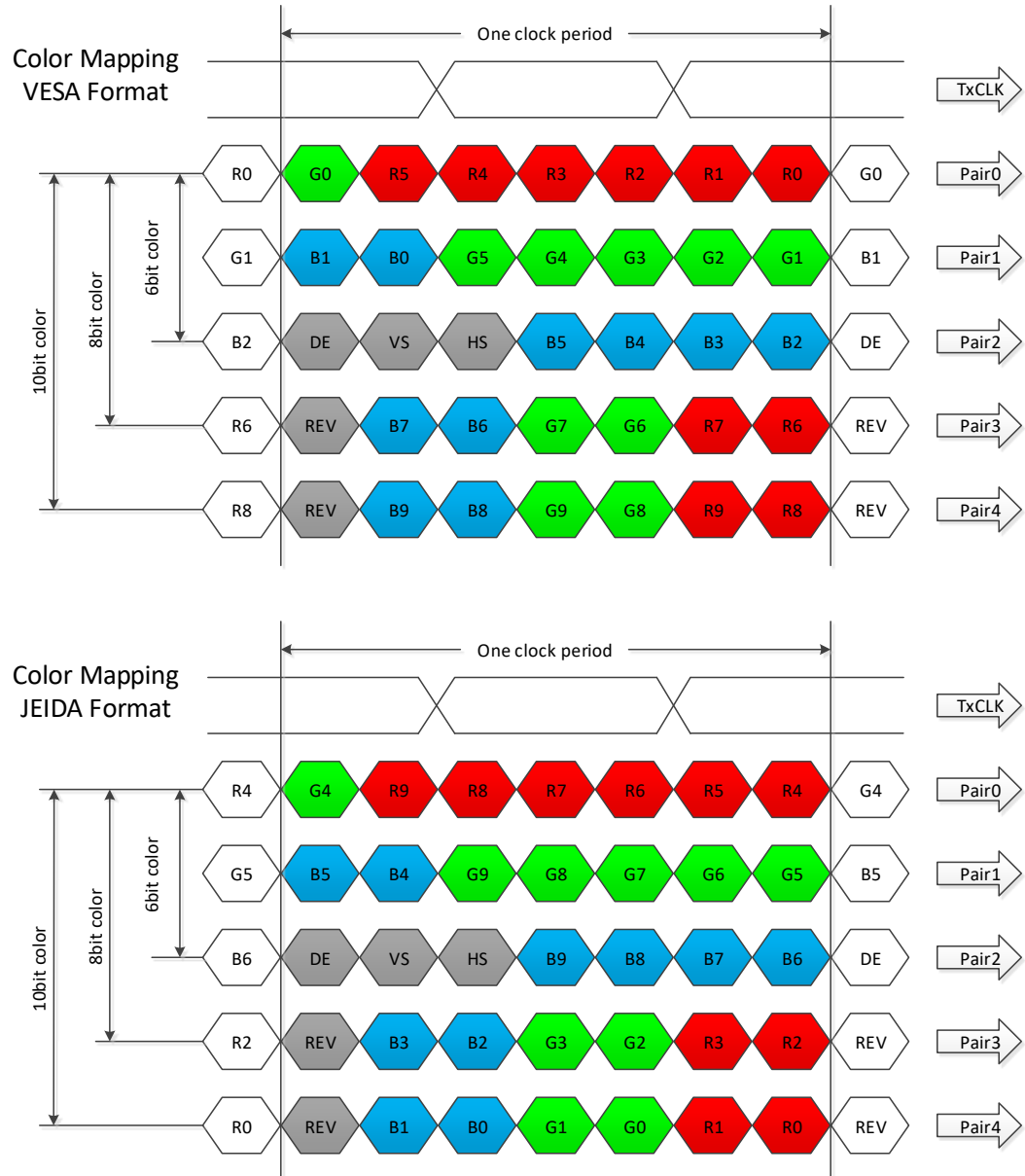
LVDS 7to1 TX mainly includes Data Mapping and Serialization (OVIDEO) modules. LVDS 7to1 RX mainly includes Deserialization (IVIDEO), Word align and Data Mapping modules.

3.2.1 LVDS 7to1 TX

The LVDS 7to1 TX is used to perform video data mapping and serial-to-parallel conversion, and it includes Data Mapping and OVIDEO.

- Data Mapping Module: Maps the video RGB data and HS/VS signals according to VESA or JEIDA standards, and the data mapping standard diagram is shown in Figure 3-3.

Figure 3-3 Data Mapping Standard Diagram



- OVIDEO Module: Converts 7-bit parallel data to serial data for output.

3.2.2 LVDS 7to1 RX

The LVDS 7to1 RX is used to perform the deserialization and data mapping of the LVDS signals, and it mainly consists of IVIDEO, Word align and Data Mapping, and finally it outputs RGB data and HS/VS signals.

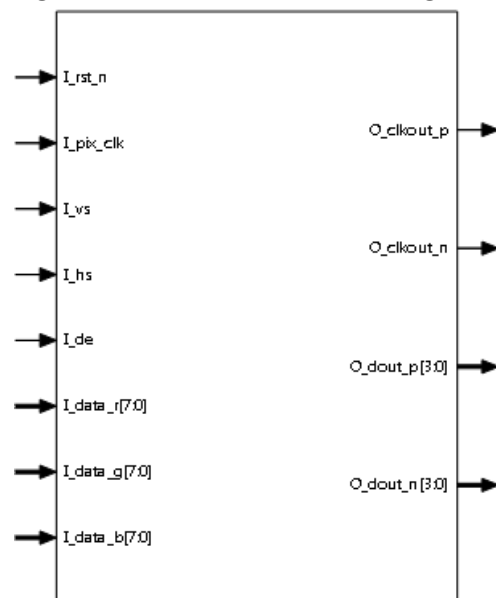
- IVIDEO Module: Converts LVDS serial data into 7-bit parallel data.
- Word align Module: Generates slip signal, and controls the IVIDEO bit shifting until clk_phase[6:0] contains 7'b1100011 or 7'b1100001.
- Data Mapping Module: Remaps the 7-bit parallel data of each channel and converts it into RGB data and HS/VS signals.

3.3 Port List

3.3.1 LVDS 7to1 TX Port

The I/O ports of the Gowin LVDS 7to1 TX are shown in Figure 3-4.

Figure 3-4 LVDS 7to1 TX IO Diagram



Ports vary slightly depending on the parameters.

The details of I/O ports of Gowin LVDS 7to1 TX are shown in Table 3-1.

Table 3-1 I/O List of Gowin LVDS 7to1 TX

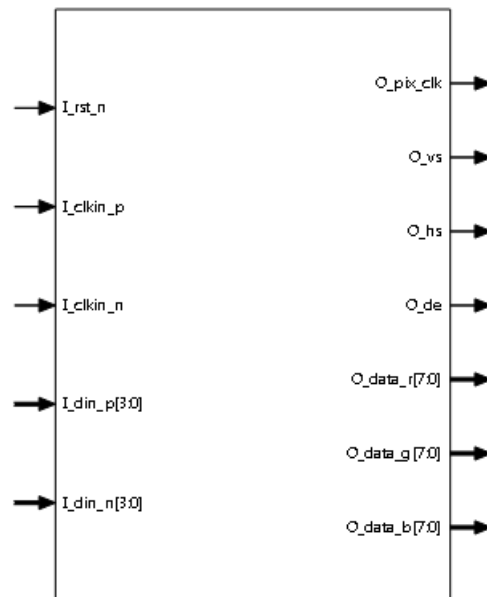
No.	Signal Name	I/O	Description	Remarks
1	I_rst_n	I	Reset signal, active-low	The I/O of all the signals takes LVDS 7to1 TX as reference.
2	I_serial_clk	I	This signal is valid when using external clock. $I_serial_clk = I_pix_clk * 3.5$	
3	I_pix_clk	I	Video input pixel clock	
4	I_vs	I	Video input vs signal	
5	I_hs	I	Video input hs signal	
6	I_de	I	Video input data enable signal	

No.	Signal Name	I/O	Description	Remarks
One Channel				
7	I_data_r	I	Video input R component	
8	I_data_g	I	Video input G component	
9	I_data_b	I	Video input B component	
10	O_clkout_p	O	LVDS differential output clock positive	
11	O_clkout_n	O	LVDS differential output clock negative	
12	O_dout_p	O	LVDS differential output data positive	
13	O_dout_n	O	LVDS differential output data negative	
Two Channel				
14	I_data_ro	I	Video input data odd pixel R component	
15	I_data_go	I	Video input data odd pixel G component	
16	I_data_bo	I	Video input data odd pixel B component	
17	I_data_re	I	Video input data even pixel R component	
18	I_data_ge	I	Video input data even pixel G component	
19	I_data_be	I	Video input data even pixel B component	
20	O_clkouto_p	O	LVDS differential output clock odd channel positive	
21	O_clkouto_n	O	LVDS differential output clock odd channel negative	
22	O_clkoute_p	O	LVDS differential output clock even channel positive	
23	O_clkoute_n	O	LVDS differential output clock even channel negative	
24	O_douto_p	O	LVDS differential output data odd channel positive	
25	O_douto_n	O	LVDS differential output data odd channel negative	
26	O_doute_p	O	LVDS differential output data even channel positive	
27	O_doute_n	O	LVDS differential output data even channel negative	

3.3.2 LVDS 7to1 RX Port

The I/O ports of Gowin LVDS 7to1 RX are shown in Figure 3-5.

Figure 3-5 LVDS 7to1 RX I/O Diagram



Ports vary slightly depending on the parameters.

The details of I/O ports of Gowin LVDS 7to1 RX are shown in Table 3-2.

Table 3-2 I/O List of Gowin LVDS 7to1 RX

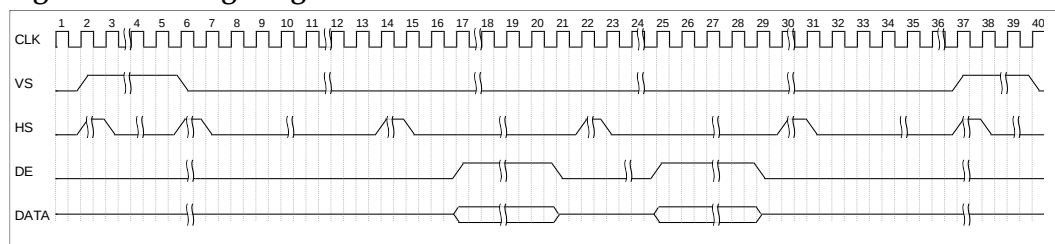
No.	Signal Name	I/O	Description	Remarks
1	I_rst_n	I	Reset signal, active-low	The I/O of all the signals takes LVDS 7to1 TX as reference.
2	O_pix_clk	O	Video output pixel clock	
3	O_vs	O	Video output vertical sync signal	
4	O_hs	O	Video output horizontal sync signal	
5	O_de	O	Video output data enable signal	
6	O_clkpat_lock	O	Clock pattern lock signal	
7	I_clkln_p	I	Input LVDS differential clock positive terminal	
8	I_clkln_n	I	Input LVDS differential clock negative terminal	
One Channel				
9	I_din_p	I	Input LVDS differential data positive terminal	
10	I_din_n	I	Input LVDS differential data negative terminal	
11	O_data_r	O	Video output data-red component	
12	O_data_g	O	Video output data-green component	

No.	Signal Name	I/O	Description	Remarks
13	O_data_b	O	Video output data-blue component	
Two Channel				
14	I_dino_p	I	Input LVDS differential data odd-channel positive terminal	
15	I_dino_n	I	Input LVDS differential data odd-channel negative terminal	
16	I_dine_p	I	Input LVDS differential data even-channel positive terminal	
17	I_dine_n	I	Input LVDS differential data even-channel negative terminal	
18	O_data_ro	O	Video output data-odd pixel red component	
19	O_data_go	O	Video output data-odd pixel green component	
20	O_data_bo	O	Video output data-odd pixel blue component	
21	O_data_re	O	Video output data-even pixel red component	
22	O_data_ge	O	Video output data-even pixel green component	
23	O_data_be	O	Video output data-even pixel blue component	

3.4 Timing Description

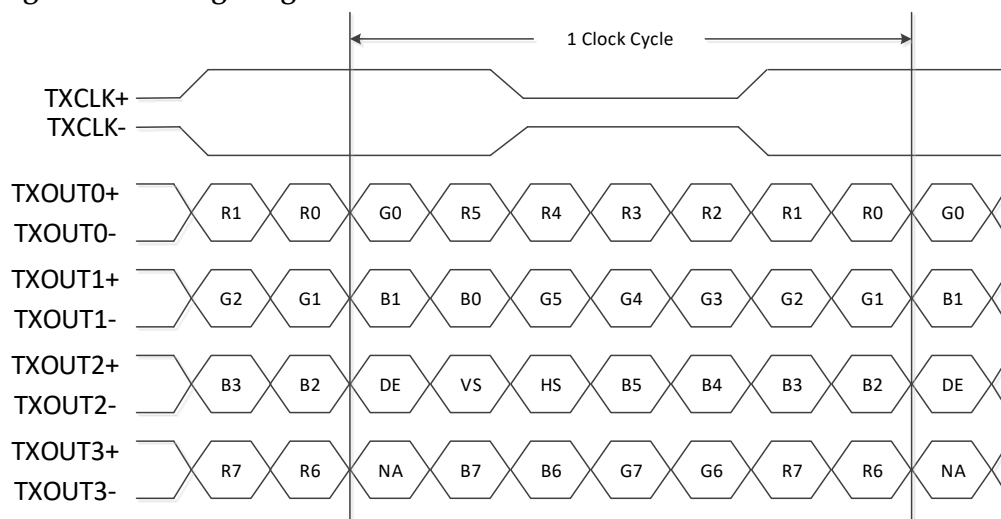
This section describes the timing of Gowin LVDS 7to1 TX RX. The video interface timing diagram of is as shown in Figure 3-6.

Figure 3-6 Timing Diagram of Video Interface



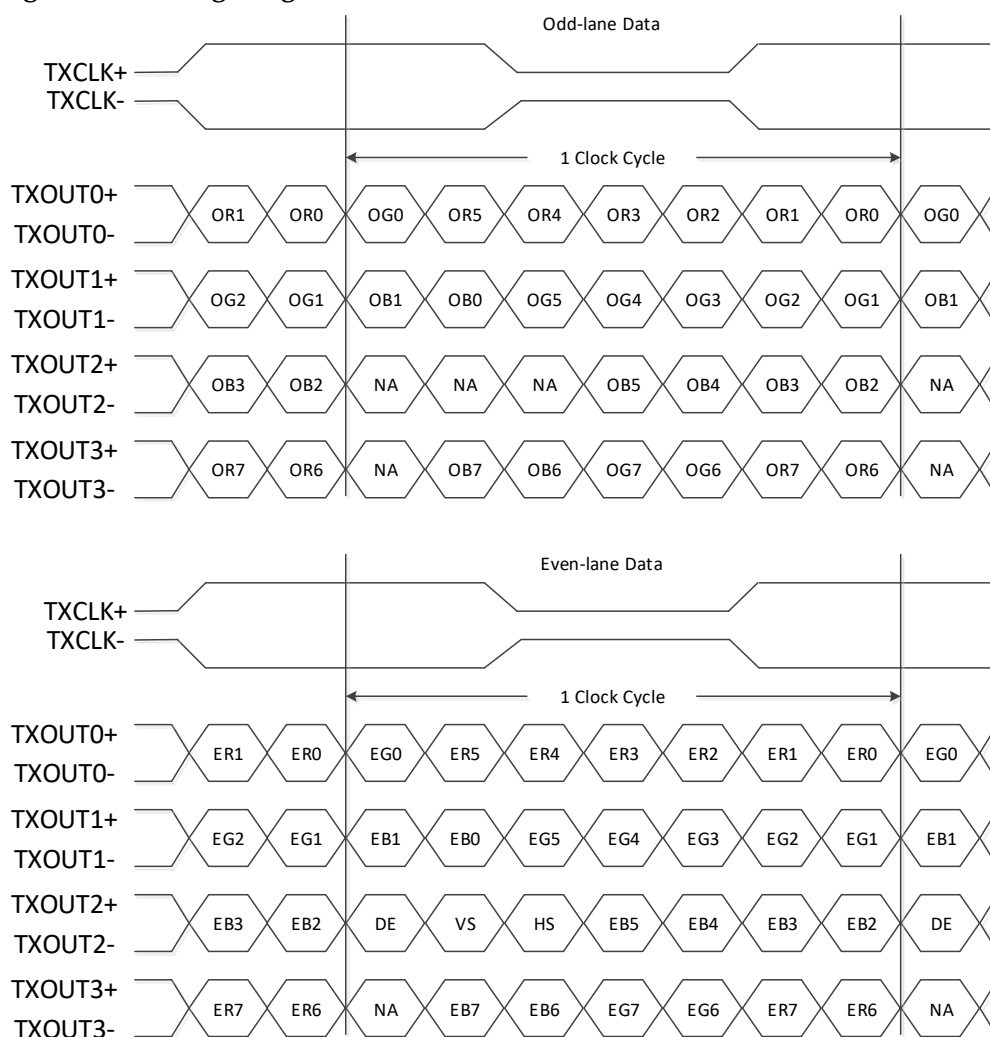
The timing diagram of one channel LVDS interface is as shown in Figure 3-7.

Figure 3-7 Timing Diagram of One Channel LVDS Interface



The timing diagram of two-channel LVDS interface is as shown in Figure 3-8.

Figure 3-8 Timing Diagram of Two-channel LVDS Interface



4 Parameter Configuration

Users can configure Gowin LVDS 7to1 TX and RX parameters using macro definitions. The parameters are located in the macro definition file.

4.1 LVDS 7to1 TX Parameters

1. LVDS_OBUF Selection: Depending on the IO locations, users can select the LVDS_OBUF type.
 - Select TLVDS type: ``define USE_TLVDS_OBUF` (default)
 - Select ELVDS type: ``define USE_ELVDS_OBUF`
2. Whether to use external clock:
 - Use external clock: ``define TX_USE_EXTERNAL_CLK` (default)
 - If not using an external clock, select the PLL type according to the device part number.
 - rPLL type: ``define TX_USE_RPLL`
 - PLLVR type: ``define TX_USE_PLLVR`
3. Channel Selection
 - Single channel: ``define TX_ONE_CHANNEL` (default)
 - Dual channel: ``define TX_TWO_CHANNEL`. If dual channel is selected, users can also configure the number of output clocks:
 - One output clock: ``define TX_TWO_CHANNEL_ONE_CLOCK`
 - Two output clocks: ``define TX_TWO_CHANNEL_TWO_CLOCK`
4. Data Mapping Method:
 - VESA data mapping: ``define TX_VESA` (default)
 - JEIDA data mapping: ``define TX_JEIDA`
5. Data Format:
 - RGB888 format: ``define TX_RGB888` (default)
 - RGB666 format: ``define TX_RGB666`
6. Clock Pattern Type:
 - 1100011 type: ``define TX_CLK_PATTERN_1100011` (default)

- 1100001 type: ``define TX_CLK_PATTERN_1100001`
7. CLKDIV Usage Selection:
- Use CLKDIV with 3.5 frequency division: ``define RX_USE_CLKDIV_3_5` (default)
 - If CLKDIV with 3.5 frequency division is not used, this macro definition is not used.

4.2 LVDS 7to1 RX Configuration

1. PLL Phase Search Mode:
 - Manual phase mode: ``define MANUAL_PHASE`
 - PLL output clock phase value: ``define RX_CLKOUTP_PHASE 4'd3` with the range 0~15
2. PLL Type Selection: Select the PLL type based on the device part number.
 - rPLL type: ``define RX_USE_RPLL` (default)
 - PLLVR type: ``define RX_USE_PLLVR`
3. Channel Selection:
 - Select single channel: ``define RX_ONE_CHANNEL` (default).
 - IODelay value for Data 0 channel: ``define D0_IODELAY 0` with range 0~127
 - IODelay value for Data 1 channel: ``define D1_IODELAY 0` with range 0~127
 - IODelay value for Data 2 channel: ``define D2_IODELAY 0` with range 0~127
 - IODelay value for Data 3 channel: ``define D3_IODELAY 0` with range 0~127
 - Dual channel: ``define RX_TWO_CHANNEL`
 - IODelay value for Odd Data 0 channel: ``define DO0_IODELAY 0` with range 0~127
 - IODelay value for Odd Data 1 channel: ``define DO1_IODELAY 0` with range 0~127
 - IODelay value for Odd Data 2 channel: ``define DO2_IODELAY 0` with range 0~127
 - IODelay value for Odd Data 3 channel: ``define DO3_IODELAY 0` with range 0~127
 - IODelay value for Even Data 0 channel: ``define DE0_IODELAY 0` with range 0~127
 - IODelay value for Even Data 1 channel: ``define DE1_IODELAY 0` with range 0~127
 - IODelay value for Even Data 2 channel: ``define DE2_IODELAY 0` with range 0~127
 - IODelay value for Even Data 3 channel: ``define DE3_IODELAY 0` with range 0~127

4. Data Mapping Method
 - VESA data mapping: ``define RX_VESA` (default)
 - JEIDA data mapping: ``define RX_JEIDA`
5. Data Format
 - RGB888 format: ``define RX_RGB888` (default)
 - RGB666 format: ``define RX_RGB666`
6. Clock Pattern Type
 - 1100011 type: ``define RX_CLK_PATTERN_1100011` (default)
 - 1100001 type: ``define RX_CLK_PATTERN_1100001`

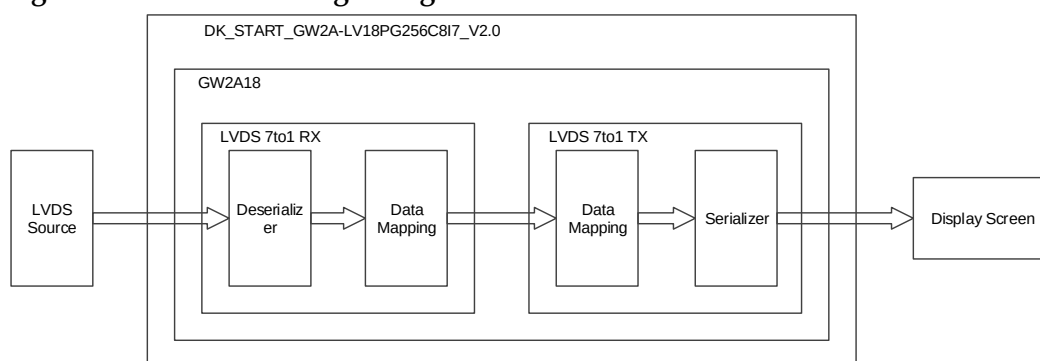
5 Reference Design

This chapter introduces the usage and structure of the reference design instance of Gowin LVDS 7to1 TX RX. Please see LVDS 7to1 TX [Reference Design](#) and RX [Reference Design](#) for details at Gowinsemi website.

5.1 Design Instance 1

Take DK_START_GW2A-LV18PG256C8I7_V2.0 as an example, and the diagram is as shown in Figure 5-1. For the details of DK_START_GW2A-LV18PG256C8I7_V2.0, you can click [here](#).

Figure 5-1 Reference Design Diagram



In this instance, there are LVDS 7to1RX and LVDS 7to1 TX, and the steps are as follows:

1. Receive LVDS 7:1 format video data with 1280x800 resolution via LVDS RX interface.
2. The LVDS 7to1 RX module is used to deserialize the LVDS signal and to map the data.
3. The LVDS 7to1 TX module is then used to map the parallel video data, serialize it, and then convert it to LVDS signals.
4. Then output the LVDS signals through the LVDS TX interface which is connected to the display screen. The input LVDS signals can be shown on the screen.

When the reference design is applied to board-level test, you can output signal to the display and also can analyze with the on-line logic

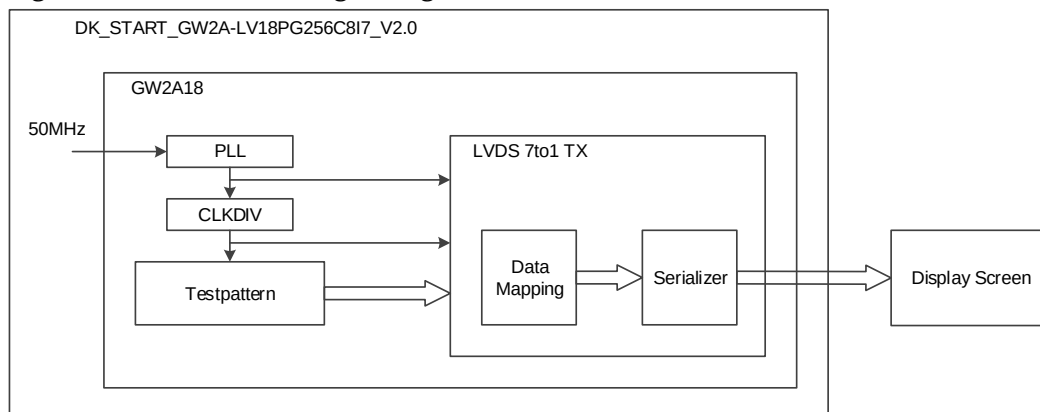
analyzer or oscilloscope.

In the simulation project provided by the reference design, bmp bitmap is used as the test excitation source, and tb is the top-level module of the simulation project. The simulation results can be compared with the output figures.

5.2 Design Instance 2

Take DK_START_GW2A-LV18PG256C8I7_V2.0 as an example, and the diagram is as shown in Figure 5-2.

Figure 5-2 Reference Design Diagram



In this reference design, there is only LVDS 7to1 TX, and its steps are as follows:

1. The pixel clock and serial clock required by LVDS 7to1 TX is generated from 50MHz reference clock.
2. Test data with 1280x800 resolution video format is output by the Testpattern module.
3. The LVDS 7to1 TX is used to map the parallel video data, serialize and convert to LVDS signals.
4. It is then output through the LVDS TX interface and connected to the display, where the test pattern can be displayed. Test pattern includes color pattern, grid pattern, grayscale pattern and pure color pattern.

In the simulation project provided by the reference design, bmp bitmap is used as the test excitation source, and tb is the top-level module of the simulation project. The simulation results can be compared with the output figures.

6 File Delivery

The delivery file of Gowin LVDS 7to1 TX RX includes file, source code and reference design.

6.1 Documents

The document mainly contains the user guide in PDF.

Table 6-1 Document List

Name	Description
TN727, Gowin LVDS 7to1 TX RX Reference Design User Manual	Gowin LVDS 7to1 TX RX reference design, namely this one.

6.2 Reference Design

The Ref. Design folder contains the netlist file, user reference design, constraints file, top-level file and the project file, etc.

Table 6-2 Gowin LVDS 7to1 RX RefDesign Flie List

Name	Description
lvds_video_top.v	The top module of reference design
lvds_video.cst	Project physical constraints file
lvds_video.sdc	Project timing constraints file
lvds_7to1_tx	LVDS 7to1 TX code folder
lvds_7to1_rx	LVDS 7to1 RX code folder

The Ref. Design folder contains the netlist file, user reference design, constraints file, top-level file and the project file, etc.

Table 6-3 File List

Name	Description
lvds_video_top.v	The top module of reference design
lvds_video.cst	Project physical constraints file
lvds_video.sdc	Project timing constraints file
testpattern.v	Reference design file
lvds_7to1_tx	LVDS 7to1 TX code folder
gowin_rpll	PLL project file

