



Gowin PCI Target IP

Release Note

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Revision History

Date	Version	Description
08/30/2019	1.0E	Initial version published.
03/30/2020	1.1E	● 1100 and 1110 description in PCI Target commands list updated; ● PCI Target pci_serr_l, pci_perr_l, tg_value description updated.

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About This Guide

This release includes Gowin PCI Target user guide and reference design.

Gowin PCI Target IP user guide and reference design are available at Gowin Website. Take specific parameters as an example for the reference design. It can be used for simulation and instantiation of the overall synthesis, placement and routing after user design.

Overview

Gowin PCI Target IP provides a solution for PCI applications and a 33M, 32bit customizable PCI Target complying with the local bus specification and PCI 2.2 protocol. It can implement PCI operations: read and write configuration, single cycle read and write, burst read and write, and so on.

Table 1 Gowin PCI Target IP Overview

Gowin PCI Target IP	
IP Core Application	
Supported Devices	GW1N series, GW1NR series GW2A series, GW2AR series GW1NS series, GW1NSR series GW1NZ series, GW1NSE series
Delivered Doc.	
Design Files	Verilog (encrypted)
TestBench	Verilog
Test and Design Flow	
Synthesis Software	Synplify_Pro
Application Software	Gowin Software

Documents

The software release file contains Gowin PCI Target IP user guide and release note, which is listed below:

Table 2 Gowin PCI Target IP Documents

Documents	Usage
Gowin PCI Target IP User Guide	PDF
Gowin PCI Target IP Release Note	PDF

IP Support

Since the requirements of user design and the highest frequency are different, the reference design does not include associated FPGA specific location (.cst) and timing constraints (.sdc) documents, which user can determine on his own as required.

For the customized IP design and support, please contact Gowin sales and support line.

Email: support@gowinsemi.com

Website: www.gowinsemi.com

